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What does the information that is listed for each connector mean? See the [tutorial](#).

## Audio/Video

### Audio

[ActionMedia 2 Audio/Video Capture](#)

[Amiga 1000 RF Monitor](#)

[Apple AudioVision](#)

[CBM 1902A](#)

[NeoGeo Audio/Video](#)

[Sony RGB Multi Input](#)

[TI-99/4A Video/Audio](#)

### Consoles

[Atari Jaguar A/V](#)

[N64 Video](#)

[PlayStation A/V](#)

[Sega Dreamcast A/V](#)

[Sega Genesis 2/32X/Nomad A/V](#)

[Sega Genesis/Master A/V](#)

[Sega Saturn A/V](#)

[SNES Video](#)

[SNES2 Video](#)

### Digital

[Digital Flat Panel \(DFP\)](#)

[Digital Visual Interface \(DVI\)](#)

[Enhanced Video Connector \(EVC\)](#)

[OpenLDI](#)

[Plug and Display Analog/Digital \(P&D-A/D\)](#)

[Plug and Display Digital \(P&D-D\)](#)

## Home Audio/Video

[3.5 mm Mono Tele](#)

[3.5 mm Stereo Tele](#)

[6.25 mm Mono Tele](#)

[6.25 mm Stereo Tele](#)

[DIN Audio](#)

[S-Video](#)

[SCART](#)

[TurboVision Turbo Express TV Tuner](#)

[VHS Video Camera](#)

## Home computers

[Amstrad CPC6128 Monitor](#)

[Amstrad CPC6128 Plus Monitor](#)

[Amstrad CPC6128 Stereo](#)

[Atari Falcon030 RGB/VGA](#)

[Atari ST Monitor Connector](#)

[C128 RGBI](#)

[C128/C64C Video](#)

[C16/C116/+4 Audio/Video](#)

[C64 Audio/Video](#)

[C65 Video](#)

[CDTV Video Slot](#)

[CM-8/CoCo RGB](#)

[Spectravideo SVI318/328 Audio/Video](#)

[ZX Spectrum 128 RGB](#)

## Video

[3b1/7300 Video](#)

[ActionMedia 2 Audio/Video Capture](#)

[Amiga 1000 RF Modulator](#)

[Amiga 1000 RF Monitor](#)

[Amiga Video](#)

[Apple AudioVision](#)

[Apple II Video Expansion](#)

[Apple Macintosh II/IIx Video](#)

[Apple Macintosh LC External Video](#)

[Apple S-Video Input](#)

[Apple S-Video Output](#)

[Apple Video Mirror](#)

[AT&T 53D410](#)

[AT&T 6300 Taxan Monitor](#)

[AT&T PC6300](#)

[CBM 1902A](#)

[CGA](#)

[Commodore 1084 & 1084S \(Analog\) Connector](#)

[Commodore 1084 & 1084S \(Digital\)](#)

[Commodore 1084d & 1084dS](#)

[ECL](#)

[EGA](#)

[IBM PCjr CGA](#)

[IBM PowerPC Video](#)

[Macintosh Video](#)

[MDA \(Hercules\)](#)

[Monochrome TTL Video](#)

[NeoGeo Audio/Video](#)

[NeXT Color Video](#)

[PGA](#)

[S-Video](#)

[SGI StereoView \(3 pin\)](#)

[SGI Video](#)

[Sony RGB Multi Input](#)

[Sun Video](#)

[TI-99/4A Video/Audio](#)

[VESA Feature](#)

[VGA \(15\)](#)

[VGA \(9\)](#)

[VGA \(VESA DDC\)](#)

[Vic 20 Video](#)

# Buses

[Accelerated Graphics Port \(AGP\)](#)

[Amiga 1200 CPU-port](#)

[Amiga Video Expansion](#)

[Apple Duo Dock](#)

[Apple Macintosh Portable Processor-Direct Slot \(PPDS\)](#)

[Apple Macintosh Processor-Direct Slot \(PDS\)](#)

[C-bus II](#)

[CardBus](#)

[CompactPCI](#)

[CompactPCI \(technical\)](#)

[ECBbus](#)

[EISA](#)

[EISA \(technical\)](#)

[Electrocoin](#)

[IEEE1394](#)

[IEEE1394 \(technical\)](#)

[ISA](#)

[ISA \(technical\)](#)

[IndustrialPCI](#)

[JAMMA](#)

[MCA](#)

[Miniature Card](#)

[Miniature Card \(technical\)](#)

[NuBus](#)

[NuBus 90](#)

[PC Card](#)

[PC/104](#)

[PCI](#)

[PCI \(technical\)](#)

[PCMCIA](#)

[SSFDC](#)

[SUN SBus](#)

[SmallPCI](#)

[Unibus](#)

[Universal Serial Bus \(USB\)](#)

[Universal Serial Bus \(USB\) \(technical\)](#)



[VESA LocalBus \(VLB\)](#)

[VESA LocalBus \(VLB\) \(technical\)](#)

[VME64x](#)

[VME64x \(technical\)](#)

[VMEbus](#)

[Zorro II](#)

[Zorro II/III](#)

## Cartridges/Expansions

### Audio

[Apple Digital Audio/Video \(DAV\)](#)

### Video

[Apple Digital Audio/Video \(DAV\)](#)

[Apple Digital Video Application \(DVA\)](#)

[+4 User Port](#)

[Amiga 1000 Ramex](#)

[Apple Communication Slot](#)

[Apple Macintosh Portable ROM Expansion](#)

[Atari 2600 Cartridge](#)

[Atari 5200 Cartridge](#)

[Atari 5200 Expansion](#)

[Atari 7800 Cartridge](#)

[Atari 7800 Expansion](#)

[Atari Cartridge Port](#)

[Atari Falcon030 DSP Port](#)

[C128 Expansion Bus](#)

[C16/+4 Expansion Bus](#)

[C64 Cartridge Expansion](#)

[C64 RS232 User Port](#)

[C64 User Port](#)

[CD32 Expansion-port](#)

[CDTV Diagnostic Slot](#)

[CDTV Expansion Slot](#)

[Commodore PET Parallel User Port](#)  
[GameBoy Cartridge](#)  
[GameBoy Cartridge](#)  
[GeekPort](#)  
[MSX Expansion](#)  
[PC-Engine Cartridge](#)  
[Psion Organiser II Connector Top Slot \(D\)](#)  
[SNES Cartridge](#)  
[SUN SROMBO](#)  
[SUN SROMBOlite](#)  
[Spectravideo SVI318/328 Expansion Bus](#)  
[Spectravideo SVI318/328 Game Cartridge](#)  
[TG-16 Cartridge](#)  
[TI-99/4A Card Slot](#)  
[TI-99/4A Cartridge Port](#)  
[TI-99/4A Side Port](#)  
[Vic 20 Memory Expansion](#)

## Cellular Phones

[Alcatel HC600/800/1000](#)  
[Ericsson 218/337/318/388](#)  
[Ericsson 628/788](#)  
[Ericsson 688/888](#)  
[Motorola 6200/7500/8200/8400/8700](#)  
[NEC P3](#)  
[Nokia 1610](#)  
[Nokia 2110](#)  
[Nokia 31xx/81xx](#)  
[Nokia 5110/6110](#)  
[Panasonic G500](#)  
[Phillips Fizz/Spark](#)  
[Siemens C25/S25](#)  
[Sony CMD 1000](#)

## Memories

## DIMM

[144 pin SO DIMM](#)

[168 pin DRAM DIMM \(Unbuffered\)](#)

[168 pin SDRAM DIMM \(Unbuffered\)](#)

## SIMM

[30 pin SIMM](#)

[72 pin ECC SIMM](#)

[72 pin SIMM](#)

## Smartcard

[SmartCard AFNOR](#)

[SmartCard ISO](#)

[SmartCard ISO 7816-2](#)

[72 pin SO DIMM](#)

[CDTV Memory Card](#)

[CompactFlash](#)

[Power Mac L2 Cache](#)

## Misc

### Harddrive

[Atari ACSI DMA](#)

### Printer

[Atari ACSI DMA](#)

## UPS

[Triplite OmniPro 675 UPS](#)

[UPS YUNTO P Series \(250/500/750/1250\)](#)

# Networks

## AUI

[Apple AUI \(AAUI\)](#)

[AUI](#)

[Media Independent Interface \(MII\)](#)

[SUN AUI](#)

## Ethernet

[Ethernet 10/100Base-T](#)

[Ethernet 1000Base-T](#)

[Ethernet 100Base-T4](#)

[Network Information](#)

# Parallel

## Parallel

[ECP Parallel](#)

[ECP Parallel \(technical\)](#)

[IEEE1284-B](#)

[IEEE1284-C](#)

[MSX Parallel](#)

[Parallel \(Amiga 1000\)](#)

[Parallel \(Amiga\)](#)

[Parallel \(Olivetti M10\)](#)

[Parallel \(PC\)](#)

[Parallel \(SUN\)](#)

## Printer

[Amstrad CPC6128 Printer Port](#)

[Centronics](#)



[Dataproducs D-Sub 50 Parallel](#)

[Dataproducs M/50 Parallel](#)

[DEC Printer](#)

## Video

[IndyCam Digital Video Port](#)

[IEEE488](#)

## PC

[3.5" Power](#)

[5.25" Power](#)

[AT Backup Battery](#)

[AT LED/Keylock](#)

[Motherboard CPU Cooling fan](#)

[Motherboard IrDA](#)

[Motherboard Power](#)

[PC Speaker](#)

[Turbo LED](#)

## Power Supply

### Amiga

[Amiga 2000 Power Supply](#)

[Amiga 3000 Power Supply](#)

[Amiga 3000T Power Supply](#)

[Amiga 500/600/1200 Power Supply](#)

### ATX

[ATX +12V Power Supply](#)

[ATX Aux Power Supply](#)

[ATX Optional Power](#)

[ATX Power Supply](#)

## SFX

[SFX Optional Power](#)

[SFX Power Supply](#)

## WTX

[WTX 12V CPU \(P3\)](#)

[WTX 12V CPU \(P4/P5\)](#)

[WTX Additional \(P2\)](#)

[WTX Main \(P1\)](#)

[Apple Macintosh Classic Internal Power](#)

[C64 Power Supply](#)

[SUN Power](#)

[Sun Aux Power](#)

## Serial

[Apple 300/1200 Modem](#)

[Apple Duo Dock Modem Adapter Card](#)

[Apple ImageWriter Serial](#)

[Apple LaserWriter AppleTalk](#)

[Apple LaserWriter Serial](#)

[Apple Macintosh XL Serial A](#)

[Apple Macintosh XL Serial B](#)

[AppleLine RS232](#)

[C64 Serial I/O](#)

[Cisco Console Port](#)

[CoCo Serial Printer](#)

[Conrad Electronics MM3610D](#)

[DEC DLV11-J Serial](#)

[DEC Dual RS-232](#)

[DEC MMJ](#)

[EIA-449 \(RS-449\)](#)

[EIA-449 \(RS-449\) Secondary](#)

[EIA530 \(RS530\)](#)

[HP 4S Scanner](#)

[HP48/HP95](#)

[ITU-TSS V.35](#)

[ITU-TSS X.21](#)

[Lowrance AirMap 100, GlobalMap 100, GlobalNav 12, GlobalNav 200, GlobalNav 212](#)

[Lowrance AirMap, AirMap 300, GlobalMap 12, GlobalMap Sport](#)

[Lowrance GlobalNav 310](#)

[MIDI In](#)

[MIDI Out](#)

[Macintosh RS-422](#)

[Macintosh Serial](#)

[Minuteman UPS](#)

[RS-232D](#)

[RS232](#)

[RS366](#)

[RS422 37pin](#)

[RS422 9pin](#)

[RocketPort Serialport](#)

[SUN LX/Classic/SS4/5/10/20 Serial Port](#)

[Serial \(15\)](#)

[Serial \(Amiga 1000\)](#)

[Serial \(Amiga\)](#)

[Serial \(MSX\)](#)

[Serial \(PC 25\)](#)

[Serial \(PC 9\)](#)

[Serial \(Printer\)](#)

[Serial \(SGI MiniDIN\)](#)

[Serial \(SUN\)](#)

## Storage

### Cassette

[Amstrad CPC6128 Tape](#)

[C16/C116/+4 Cassette](#)

[C64 Cassette](#)

[Cassette TI-99/4a](#)

[CoCo Cassette](#)

[MSX Cassette](#)

[Spectravideo SVI318/328 Cassette](#)

## CD-ROM

[Mitsumi CD-ROM](#)

[Panasonic CD-ROM](#)

[Sony CD-ROM](#)

## Floppy

[8" Floppy Diskdrive](#)

[Amiga External Diskdrive](#)

[Amstrad CPC6128 Diskdrive 2](#)

[Amstrad CPC6128 Plus External Diskdrive](#)

[Apple Macintosh External Drive](#)

[Apple Macintosh Internal Floppy disk drive](#)

[Atari Floppy Port](#)

[Internal Diskdrive](#)

[Macintosh External Drive](#)

[MSX External Diskdrive](#)

[SUN Internal Floppydrive](#)

## Harddrive

[ESDI](#)

[PC Card ATA](#)

[ST506/412](#)

## IDE/ATA

[ATA \(44\) Internal](#)

[ATA Internal](#)

[IDE Internal](#)

[Paravision SX-1 External IDE](#)

[PC Card ATA](#)

## SCSI



## Information

### [SCSI Information](#)

[Apple SCSI HDI-30](#)

[Novell and Procomp External SCSI](#)

[SCSI External Centronics 50 \(Differential\)](#)

[SCSI External Centronics 50 \(Single-ended\)](#)

[SCSI External D-Sub \(Future Domain\)](#)

[SCSI External D-Sub \(PC/Amiga/Mac\)](#)

[SCSI External IBM Burndy](#)

[SCSI Internal \(2.5"\)](#)

[SCSI Internal \(Differential\)](#)

[SCSI Internal \(Single-ended\)](#)

[SCSI-II External Hi D-Sub \(Differential\)](#)

[SCSI-II External Hi D-Sub \(Single-ended\)](#)

[SCSI-III External Hi D-Sub \(Differential\)](#)

[SCSI-III External Hi D-Sub \(Differential\)](#)

[SCSI-III External Hi D-Sub \(Single-ended\)](#)

[SCSI-III External Hi D-Sub \(Single-ended\)](#)

[Adaptec RAIDport](#)

[IEEE488](#)

## Mice/Keyboards/Joysticks

### Joystick

[Amstrad Digital Joystick](#)

[Apple IIc Joystick](#)

[Atari 2600 Controller Pinouts](#)

[Atari 2600 Joystick](#)

[Atari 5200 Joystick](#)

[Atari 7800 Joystick](#)

[Atari Enhanced Joystick](#)

[Atari Enhanced Joystick](#)

[Atari Mouse/Joy](#)

[C16/C116/+4 Joystick](#)

[C64 Control Port](#)

[MSX Joystick](#)

[NeoGeo Joystick](#)

[Nintendo SNES Controller](#)

[PC Gameport](#)

[PC Gameport+MIDI](#)

[Sega Genesis Controller](#)

[Sony Playstation Controller Port](#)

[TI-99/4A Joystick Port](#)

[Vectrex Controller](#)

## Keyboard

[AT&T 6300 Keyboard](#)

[Keyboard \(5 Amiga\)](#)

[Keyboard \(5 PC\)](#)

[Keyboard \(6 Amiga\)](#)

[Keyboard \(6 PC\)](#)

[Keyboard \(Amiga CD32\)](#)

[Keyboard \(XT\)](#)

[Macintosh Keyboard](#)

[Macintosh Keyboard Connector](#)

[SUN Keyboard/Mouse](#)

[TI-99/4A Keyboard](#)

## Mouse

[Amiga Mouse/Joy](#)

[Apple Macintosh Mouse Connector](#)

[Macintosh Mouse](#)

[Mouse \(PS/2\)](#)

[SGI Mouse \(Model 021-0004-002\) Connector](#)

[SUN Keyboard/Mouse](#)

## Serial

[Apple Desktop Bus \(ADB\)](#)

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# HARDWARE BOOK

Welcome to the Hardware Book. Internet's **largest** free collection of connector pinouts and cable descriptions.

**Newsflash!** A new version of The Hardware Book has been released as of 2001-06-08! See News for more details.

	<a href="#">Connectors</a>	Pinouts for connectors, buses etc.
	<a href="#">Cables</a>	How to build serial cables and many other cables.
	<a href="#">Adapters</a>	How to build adapters.
	<a href="#">Circuits</a>	Misc circuits (active filters etc).
	<a href="#">Tables</a>	Misc tables with info. (AWG..)
	<a href="#">WWW Links</a>	Links to other electronic resources.
	<a href="#">Download</a>	Download The Hardware Book for offline viewing.
	<a href="#">News</a>	News information about The Hardware Book.
	<a href="#">Wanted</a>	Information we are currently looking for.
	<a href="#">About</a>	Who did this? And why?
	<a href="#">Comment</a>	Send your comments to the author.

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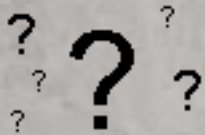
# Short tutorial

## Heading

First at each page there a short heading describing what the connector is.

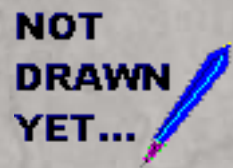
## Pictures of the connectors

After that there is at each page there is one or more pictures of the connectors. Sometimes there is some question marks only. This means that we don't know what kind of connector it is or how it looks.



(at the computer)

There may be some pictures we haven't drawn yet. We illustrate this with the following advanced picture:



(at the computer)

Normally are one or more pictures. **These are seen from the front, and NOT the soldside. Holes (female connectors usually) are darkened.** Look at the example below. The first is a female connector and the second is a male. The texts inside parentheses will tell you at which kind of the device it will look like that.



(at the videocard)



(at the monitor cable)

## Texts describing the connectors

Below the pictures there is texts that describes the connectors. Including the name of the physical connector.

5 PIN DIN 180° (DIN41524) at the computer.

## Pin table

The pin table is perhaps the information you are looking for. Should be simple to read. Contains mostly the following three columns; Pin, Name & Description.

Pin	Name	Description
1	CLOCK	Key Clock
2	GND	GND
3	DATA	Key Data
4	VCC	+5 VDC
5	n/c	Not connected

## Contributor & Source

All persons that helped us or sent us information about the connector will be listed here. The source of the information is perhaps a book or another site.

Example:

Contributor: [Joakim Ögren](#)

Source: *Amiga 4000 User's Guide from Commodore*

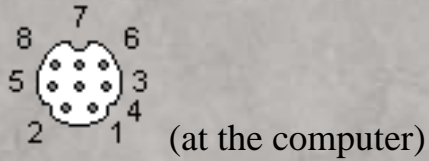
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# ActionMedia 2 Audio/Video Capture



8 PIN MINI-DIN FEMALE at the computer.

Pin	Description
1	Composite Sync Input
2	Blue Video Input
3	Red Video Input
4	Video Ground
5	Left Audio Input
6	Green Video Input
7	Right Audio Input
8	Audio Ground

Table below shows usage of inputs depending of the type:

Mode	3 (R)	6 (G)	2 (B)	1 (S)
-Composite video 1 (VCR)	Yes			
Composite video 2		Yes		
SVHS (Y/C)	Y	C		
RGB (sync-on-green)	R	G	B	
RGBS	R	G	B	S

Contributor: [Joakim Ögren](#)

Source:



[ActionMedia II legacy page](#)

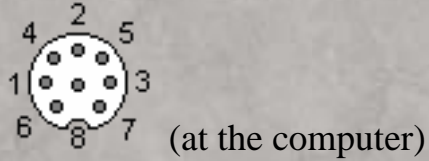
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# Amiga 1000 RF Monitor



8 PIN DIN "C" FEMALE at the computer.

Pin	Name	Dir	Description
1	n/c	-	Not connected
2	GND	—	Ground
3	AUDL	→	Audio Left
4	CVIDEO	→	Composite Video
5	GND	—	Ground
6	n/c	-	Not connected
7	+12V	→	+12 VDC
8	AUDR	→	Audio Right

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#)

Source:  
?

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# Apple AudioVision

45 PIN UNKNOWN CONNECTOR ??

Pin	Name
1	Analog audio ground
2	Audio input shield
3	Left channel audio input
4	Right channel audio input
5	Left channel audio output
6	Right channel audio output
7	Reserved
8	Monitor ID sense line 1
9	Monitor ID sense line 2
10	Green ground (shield)
11	Green video output (75 )
12	Video input power ground
13	Power for camera +5 V
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Monitor ID sense line 3
19	S-video input shield
20	S-video input luminance (Y)
21	S-video input chroma (C)
22	Reserved
24	Reserved
25	Reserved

26	Red ground (shield)
27	Red video output (75 )
28	I <sup>2</sup> C data signal
29	I <sup>2</sup> C clock signal
30	Reserved
31	Monitor ID
32	Monitor ID
33	Vertical sync signal
34	Composite sync signal
35	ADB power +5 V
36	ADB ground
37	ADB data
38	Keyboard switch
39	Reserved
40	Reserved
41	Monitor ID
42	Horizontal sync signal
43	Video sync ground
44	Blue ground (shield)
45	Blue video output (75 )

Contributor: [Joakim Ögren](#)

Source:

[Apple Tech Info Library 14703: Power Macintosh Pinouts](#) at [Apple TIL homepage](#)

[Apple Tech Info Library 12719: AudioVision 14 Display High-Density Connector Pinouts](#) at [Apple TIL homepage](#)

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# CBM 1902A

Available on the Commodore CBM 1902A monitor.



(at the Monitor)

6 PIN DIN FEMALE at the Monitor.

Pin	Name	Dir	Description
1	n/c	-	Not connected
2	AUDIO	←	Audio
3	GND	—	Ground
4	C	←	Chroma
5	n/c	-	Not connected
6	L	←	Luminance

*Note: Direction is Monitor relative Computer.*

Contributor: [Joakim Ögren](#)

Source:  
[comp.sys.cbm General FAQ v3.1 Part 7](#)

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# NeoGeo Audio/Video

Available on the NeoGeo videogame.



(at the Computer)

8 PIN DIN (DIN45326) FEMALE at the Computer.

Pin	Name	Dir	Description
1	AOUT	→	Audio out
2	GND	—	Ground
3	VIDEO	→	Composite Video Out
4	+5V	→	+5 VDC
5	GREEN	→	Green Video
6	RED	→	Red Video
7	NSYNC	→	Negative Sync
8	BLUE	→	Blue Video

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#), [Enzo](#), [Steffen Kupfer](#)

Source:  
?

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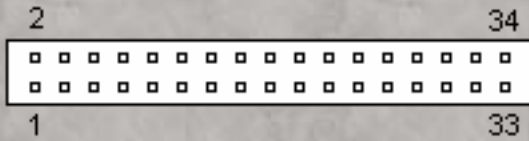
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# Sony RGB Multi Input

Available on Sony KV-25XBR TV's



(at the TV)

34 PIN IDC MALE at the TV

Pin	Description
1	+5V power supply
2	+5V power supply
3	Audio (R) input GND
4	GND
5	Remote control GND
6	Composite video output GND
7	Audio (L) input GND
8	Red Return (GND)
9	Green Return (GND)
10	Blue Return (GND)
11	GND
12	Blanking input Return (GND)
13	H.sync Return (GND)
14	N.C.
15	V.sync Return (GND)
16	GND
17	N.C.
18	N.C.

19	N.C.
20	Audio (R) Input
21	Mode Select
22	N.C.
23	Composite Video Output
24	Audio (L) Input
25	Red Input
26	Green Input
27	Blue input
28	N.C.
29	Blanking Input
30	H.sync or composite sync
31	V.sync
32	N.C.
33	RGB/NORMAL mode select
34	Audio Select

Contributor: [Joakim Ögren](#), Shawn Lin

Source:  
[Pinouts FAQ](#) at [Sci.Electronics.Repair FAQ](#)

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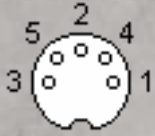
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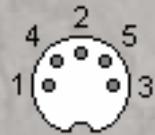




# TI-99/4A Video/Audio



(At the Computer)



at the Computer.

Pin	Name	Description
1	12V vid	
2	R-Y	color burst clock
3	AUDIO	Sound output
4	Y	
5	B-Y	external video input?
U	GND	GROUND

Contributor: [Joakim Ögren](#)

Source:

?

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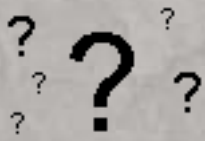


# Atari Jaguar A/V

TOP (duh)

1A 2A 3A 4A 5A 6A 7A 8A 9A 10A 11A 12A

1B 2B 3B 4B 5B 6B 7B 8B 9B 10B 11B 12B



(at the Atari)

12 PIN ?? at the Atari.

Pin	Name	Description
1A	AL	Audio Left
2A	AGND	Audio Ground
3A	GND	Ground
4A	GND (chroma)	Ground (Chroma)
5A	B	RGB Blue
6A	HSYNC	Horizontal sync
7A	G	RGB Green
8A	CHROMA	Chroma
9A	GND ???	Ground ???
10A	+5V ???	+5 VDC ???
11A	+5V ???	+5 VDC ???
12A	?	?
1B	AR	Right audio
2B	AGND	Audio GND

3B	GND	Ground
4B	R	RGB Red
5B	CSYNC	Composite (Vertical) Sync
6B	?	?
7B	LGND	Luminance Ground
8B	LUM	Luminance
9B	GND	Ground
10B	CVBSGND	Composite Video Ground
11B	CVBS	Composite Video
12B	?	?

Contributor: [Joakim Ögren](#)

Source:

Scooping out Jaguar RGB by [Duncan Brown](#) in Atari Explorer Online Vol.3 Issue 6

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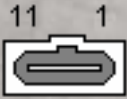
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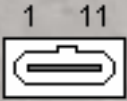


# N64 Video

Available on the Nintendo N64.



12 2 (at the SNES)



2 12 (at the video cable)

SNES A/V MALE CONNECTOR at the SNES.

SNES A/V FEMALE CONNECTOR at the video cable.

Pin	Name	Description
1	n/c	Not connected
2	n/c	Not connected
3	n/c	Not connected
4	n/c	Not connected
5	GND	Ground
6	GND	Ground
7	Y	S-Video Y
8	C	S-Video C
9	CVBS	Composite Video
10	+5V	+5 VDC
11	L+R	Left+Right Audio (Mono)
12	L-R	Left-Right Audio (Used to calculate Stereo)

Contributor: [Joakim Ögren](#)

Source:

[Video Games FAQ \(Part 3\)](#)



*Pinout from Radio Electronics April 1992*

*[SNES A/V Pinout](#) at [GamesX](#)*

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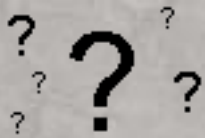
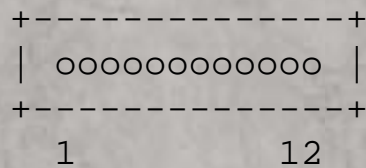
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# PlayStation A/V

Available on the Sony PlayStation Videogame.



(at the PlayStation)

12 PIN ?? at the PlayStation.

Pin	Name	Description
1	GND	Ground
2	RT	Right Audio
3	GND	Ground
4	LT	Left Audio
5	Y	S-Video Y
6	SYNC	Composite Sync
7	C	S-Video C
8	VGND	Video Ground
9	B	Blue
10	+5V	+5 VDC
11	R	Red
12	G	Green

Contributor: [Lawrence Wright](#)

*Source:*

*[Sony PlayStation A/V Pinout](#)*

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*Document last modified: 2001-06-07*



# Sega Dreamcast A/V

Pin	Description
1	Ground
2	Right Audio
3	Left Audio
4	+12v
5	+5v
6	31 kHz RGB - (VGA rate) Connect to GND with pin 7
7	15 kHz RGB - (TV rate) Connect to GND
8	Vertical Sync (for VGA)
9	Horizontal Sync (for VGA)
10	Composite Sync
11	S-video
12	S-video
13	Composite Video
14	Blue (Use 220uf cap)
15	Green (Use 220uf cap)
16	Red (use 220uf cap)

Contributor: [Joakim Ögren](#), [Marcus Hilbe](#), [Marvin](#)

Source:

?

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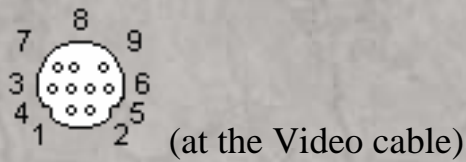
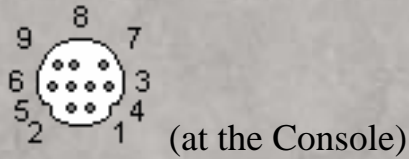
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# Sega Genesis 2/32X/Nomad A/V



9 PIN SPECIAL MINI-DIN FEMALE at the Console.

9 PIN SPECIAL MINI-DIN MALE at the Video cable.

Pin	Description
1	Blue
2	+5VDC
3	Green
4	Composite Video
5	Sync
6	Audio Mono
7	Red
8	Stereo L
9	Stereo R

Contributor: [Joakim Ögren](#), [Jerry Lynds](#)

Source:  
[SEGA Genesis A/V pinout](#) at [GamesX](#)  
[SegaDome](#)

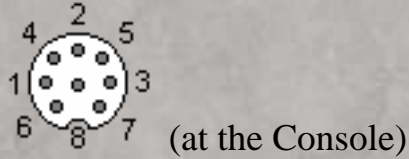
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# Sega Genesis/Master A/V



(at the Console)

8 PIN DIN 'C' FEMALE at the Console.

Pin	Description
1	Composite Video
2	Ground
3	Audio Mono
4	Green
5	+5VDC
6	Sync
7	Red
8	Blue

Contributor: [Joakim Ögren](#), [Jerry Lynds](#)

Source:  
[SEGA Genesis A/V pinout](#) at [GamesX](#)  
[SegaDome](#)

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# Sega Saturn A/V



(at the Console)

10 PIN SPECIAL MINI-DIN FEMALE at the Console.

Pin	Description
1	Sync
2	Stereo L
3	Stereo R
4	+5VDC
5	Red
6	Green
7	Blue
8	Composite Video
9	Luminance
10	Chrominance

Contributor: [Joakim Ögren](#), [Jerry Lynds](#)

Source:

[SEGA Genesis A/V pinout](#) at [GamesX](#)

[SegaDome](#)

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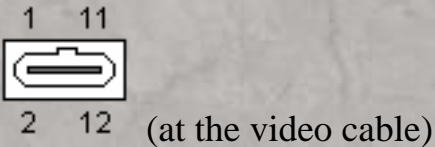
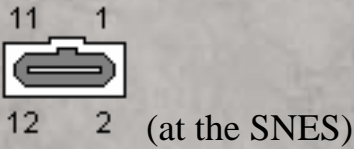
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# SNES Video

Available on the Nintendo SNES.



SNES A/V MALE CONNECTOR at the SNES.

SNES A/V FEMALE CONNECTOR at the video cable.

Pin	Name	Description
1	R	Red (Requires 200 uF in series)
2	G	Green (Requires 200 uF in series)
3	CSYNC	Composite Sync
4	B	Blue (Requires 200 uF in series)
5	GND	Ground
6	GND	Ground
7	Y	S-Video Y
8	C	S-Video C
9	CVBS	Composite Video
10	+5V	+5 VDC
11	L+R	Left+Right Audio (Mono)
12	L-R	Left-Right Audio (Used to calculate Stereo)

*Note: Pin 3 is SCART Switch voltage (+11 VDC) on PAL machines*

Contributor: [Joakim Ögren](#), [Mark K](#)



*Source:*

*[Video Games FAQ \(Part 3\)](#)*

*Pinout from Radio Electronics April 1992*

*[SNES A/V Pinout](#) at [GamesX](#)*

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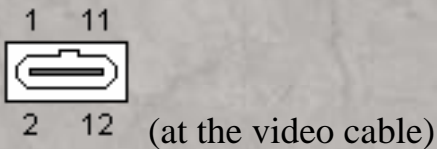
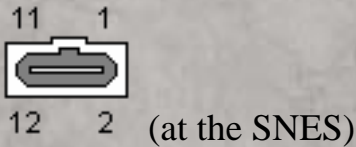
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# SNES2 Video

Available on the newer models of Nintendo SNES.



SNES A/V MALE CONNECTOR at the SNES.

SNES A/V FEMALE CONNECTOR at the video cable.

Pin	Name	Description
1	R	Red (Requires 200 uF in series)
2	G	Green (Requires 200 uF in series)
3	CSYNC	Composite Sync
4	B	Blue (Requires 200 uF in series)
5	GND	Ground
6	GND	Ground
7	n/c	Not connected
8	n/c	Not connected
9	CVBS	Composite Video
10	+5V	+5 VDC
11	L+R	Left+Right Audio (Mono)
12	L-R	Left-Right Audio (Used to calculate Stereo)

*Note: Pin 3 is SCART Switch voltage (+11 VDC) on PAL machines*

Contributor: [Joakim Ögren](#), [Mark K](#)

*Source:*

*[Video Games FAQ \(Part 3\)](#)*

*Pinout from Radio Electronics April 1992*

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# Digital Flat Panel (DFP)



MDR20 female

Used on digital flat panel monitors.

Standard by DFP Group  
Protocol: PanelLink

Pin	Name
1	TX1+
2	TX1-
3	SHLD1
4	SHLDC
5	TXC+
6	TXC-
7	GND
8	+5V
9	NC
10	NC
11	TX2+
12	TX2-
13	SHLD2
14	SHLD0
15	TX0+
16	TX0-
17	NC
18	HPD



19	DDC_DAT
20	DDC_CLK

*Contributor:* [Joakim Ögren](#)

*Source:*  
[Tech page](#) at [Network Technologies Inc](#)

*Info:* [DFP Group](#)

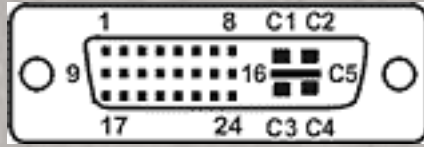
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# Digital Visual Interface (DVI)



DVI female

24 PIN DVI FEMALE at the Computer

UNKNOWN CONNECTOR

Pin	Name
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2 Shield
4	No Connection
5	No Connection
6	DDC Clock
7	DDC Data
8	No Connection
9	TMDS Data1-
10	TMDS Data2+
11	TMDS Data1 Shield
12	No Connection
13	No Connection
14	+5 V Power
15	Ground (for +5 V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDSData0+
19	TMDS Data0Shield

20	No Connection
21	No Connection
22	TMD5 Clock Shield
23	TMD5 Clock +
24	TMD5 Clock <

*Contributor:* [Joakim Ögren](#)

*Source:*

[Apple Tech Info Library 24928: Apple Studio Display 15 pinout at Apple TIL homepage](#)  
[Tech page at Network Technologies Inc](#)

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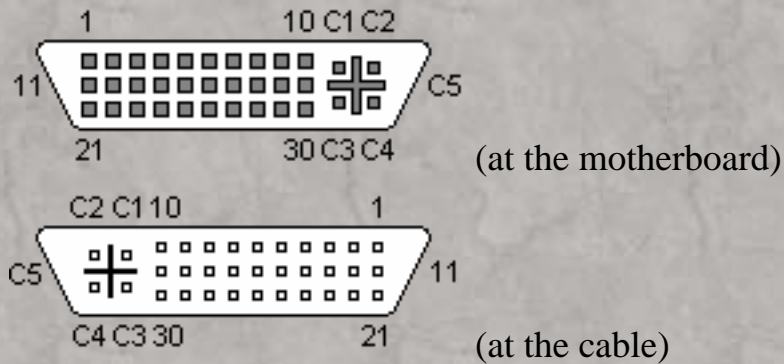
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# Enhanced Video Connector (EVC)

Defined by Video Electronic Standards Association (VESA)



35 PIN MOLEX "MicroCross" FEMALE at the videocard/monitor

35 PIN MOLEX "MicroCross" MALE at the cable

Pin	Name
1	Audio output, Right
2	Audio output, Left
3	Audio output return
4	Sync return
5	Horizontal sync (TTL)
6	Vertical sync (TTL)
7	Reserved
8	Reserved
9	1394 pair A, data -
10	1394 pair A, data +
11	Reserved
12	Reserved
13	Video input, Y or composite in
14	Video input, return



15	Video input, C in
16	USB data +
17	USB data -
18	USB/1394 common mode shield
19	1394 Vg
20	1394 Vp
21	Audio input, Left
22	Audio input, Right
23	Audio input return
24	Stereo sync (TTL)
25	DDC return
26	DDC data (SDA)
27	DDC, clock (SCL)
28	+5 VDC
29	1394 pair B, clock +
30	1394 pair B, clock -
C1	Red Video
C2	Green Video
C3	
C4	Blue Video
C5	Ground

Contributor: [Joakim Ögren](#)

Source:  
[Tech page](#) at [Network Technologies Inc](#)

Info:  
[Video Electronic Standards Association \(VESA\)](#)

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# OpenLDI



36 PIN MDR36 FEMALE

Used on SGI digital flat panel monitors.

Standard by VICI  
Protocol: LVDS

Pin	Name
1	Link2 D0-
2	Link2 D0+
3	Link2 D1-
4	Link2 D1+
5	Link2 D2-
6	Link2 D2+
7	NC NC
8	NC NC
9	GND GND
10	GND GND
11	NC NC
12	NC NC
13	Link1 D0-
14	Link1 D0+
15	Link1 D1-
16	Link1 D1+
17	Link1 D2-
18	Link1 D2+

19	Link2 D3-
20	Link2 D3+
21	Link2 CLK-
22	Link2 CLK+
23	NC NC
24	NC NC
25	NC NC
26	GND GND
27	NC NC
28	GND GND
29	NC NC
30	NC NC
31	NC NC
32	GND GND
33	Link1 CLK-
34	Link1 CLK+
35	Link1 D3-
36	Link1 D3+

Contributor: [Joakim Ögren](#)

Source:

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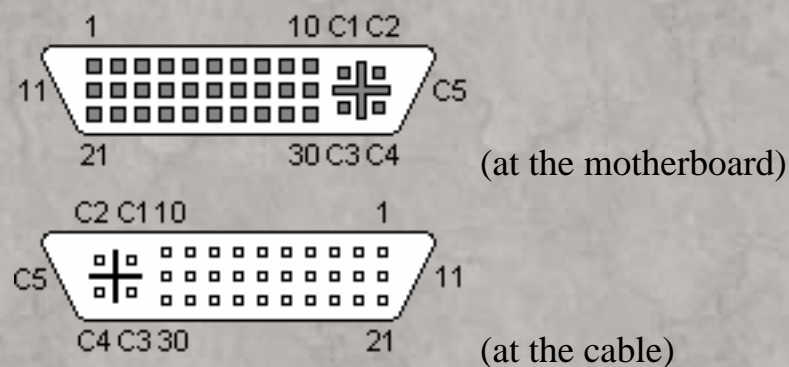
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# Plug and Display Analog/Digital (P&D-A/D)

Defined by Video Electronic Standards Association (VESA) in the Plug and Display (P&D) standard



35 PIN MOLEX "MicroCross" FEMALE at the videocard/monitor

35 PIN MOLEX "MicroCross" MALE at the cable

Pin	Name
1	TMDS Data 2 +
2	TMDS Data 2 -
3	TMDS Data return
4	Hz and Vt Sync return
5	Horizontal sync/Composite sync
6	Vertical sync
7	TMDS Clock return
8	Charge power
9	1394 pair A, data -
10	1394 pair A, data +
11	TMDS Data 1 +
12	TMDS Data 1 -
13	TMDS Data 1 return



14	TMDS Clock +
15	TMDS Clock -
16	USB data +
17	USB data -
18*	1394 outer shield (optional) & Charge Power return
19	1394 Vg
20	1394 Vp
21	TMDS Data 0 +
22	TMDS Data 0 -
23	TMDS Data 0 return
24	Stereo sync (TTL)
25	DDC return & Stereo Sync return
26	DDC data (SDA)
27	DDC clock (SCL)
28	+5 VDC
29	1394 pair B, clock +
30	1394 pair B, clock -
C1	Red Video
C2	Green Video
C3	Pixel clock (optional)
C4	Blue Video
C5	Video / Pixel Clock Ground

Contributor: [Joakim Ögren](#)

Source:

[Tech page](#) at [Network Technologies Inc](#)

Info:

[Video Electronic Standards Association \(VESA\)](#)

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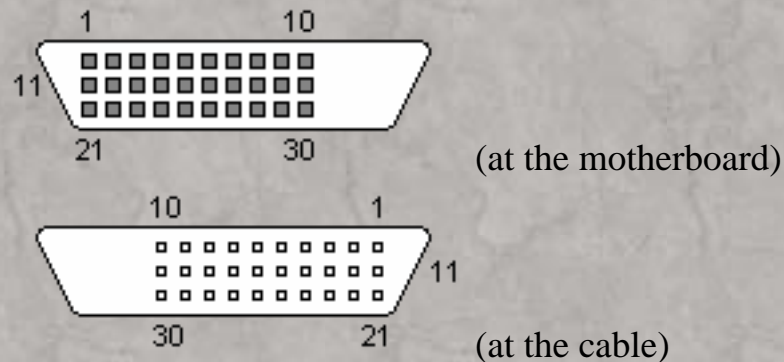
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# Plug and Display Digital (P&D-D)

Defined by Video Electronic Standards Association (VESA) in the Plug and Display (P&D) standard



30 PIN MOLEX "MicroCross" FEMALE at the videocard/monitor

30 PIN MOLEX "MicroCross" MALE at the cable

Pin	Name
1	TMDS Data 2 +
2	TMDS Data 2 -
3	TMDS Data return
4	Unused
5	Unused
6	Unused
7	TMDS Clock return
8	Charge power (optional)
9	1394 pair A, data -
10	1394 pair A, data +
11	TMDS Data 1 +
12	TMDS Data 1 -
13	TMDS Data 1 return
14	TMDS Clock +

15	TMDS Clock -
16	USB data +
17	USB data -
18	1394 outer shield (optional) & Charge Power return
19	1394 Vg
20	1394 Vp
21	TMDS Data 0 +
22	TMDS Data 0 -
23	TMDS Data 0 return
24	Unused
25	DDC return
26	DDC data (SDA)
27	DDC clock (SCL)
28	+5 VDC
29	1394 pair B, clock +
30	1394 pair B, clock -

Contributor: [Joakim Ögren](#)

Source:  
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Info:  
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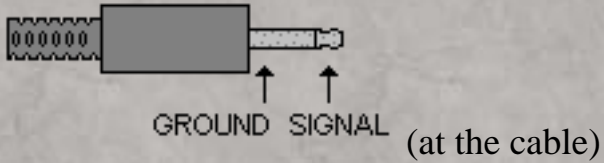
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# 3.5 mm Mono Tele



3.5 mm MONO TELEPHONE MALE at the cable.

Name	Description
SIGNAL	Signal
GROUND	Ground

Contributor: [Joakim Ögren](#)

Source:  
?

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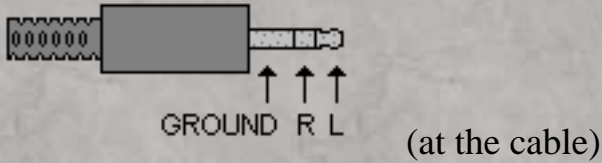
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# 3.5 mm Stereo Tele



3.5 mm STEREO TELEPHONE MALE at the cable.

Name	Description
L	Left Signal
R	Right Signal
GROUND	Ground

Contributor: [Joakim Ögren](#), [Uwe Hartmann](#)

Source:  
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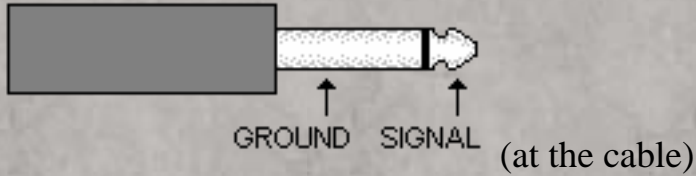
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# 6.25 mm Mono Tele



6.25 mm MONO TELEPHONE MALE at the cable.

Name	Description
SIGNAL	Signal
GROUND	Ground

Contributor: [Joakim Ögren](#)

Source:  
?

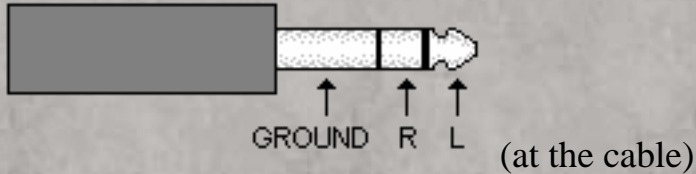
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# 6.25 mm Stereo Tele



6.25 mm STEREO TELEPHONE MALE at the cable.

Name	Description
L	Left Signal
R	Right Signal
GROUND	Ground

Contributor: [Joakim Ögren](#)

Source:  
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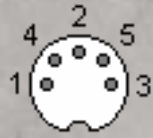
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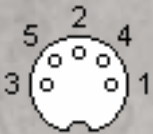
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# DIN Audio



(at the peripheral)



(at the cable)

5 PIN DIN 180° (DIN41524) FEMALE at the peripheral.

5 PIN DIN 180° (DIN41524) MALE at the cable.

Peripheral	Connected	In L	In R	Out L	Out R	Ground
Amplifier	Pickup, tuner	3	5			2
Amplifier	Taperecorder	3	5	1	4	2
Tuner	Amplifier			3	5	2
Tuner	Taperecorder			1	4	2
Recordplayer	Amplifier			3	5	2
Taperecorder	Amplifier	1	4	3	5	2
Taperecorder	Receiver	1	4	3	5	2
Taperecorder	Microphone	1	4			2

Contributor: [Joakim Ögren](#)

Source:

[ELFA's catalog Nr 44](#)

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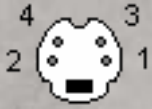
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# S-Video



(at the peripheral)

4 PIN MINI-DIN FEMALE at the peripheral.

Pin	Name	Description
1	GND	Ground (Y)
2	GND	Ground (C)
3	Y	Intensity (Luminance)
4	C	Color (Chrominance)

Contributor: [Joakim Ögren](#)

Source:

*Video Demystified at Keith Jack's pages*

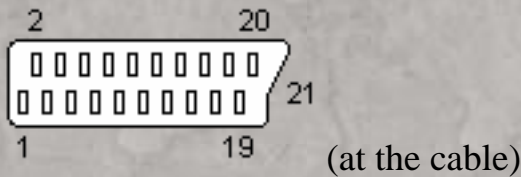
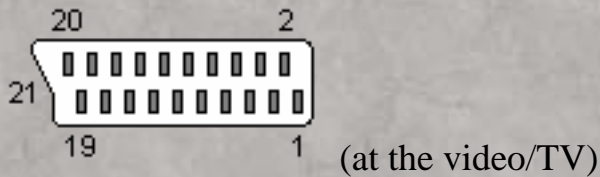
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# SCART



21 PIN SCART FEMALE at the Video/TV.

21 PIN SCART MALE at the Cable.

Pin	Name	Description	Signal Level	Impedance
1	AOR	Audio Out Right	0.5 V rms	<1k ohm
2	AIR	Audio In Right	0.5 V rms	>10k ohm
3	AOL	Audio Out Left + Mono	0.5 V rms	<1k ohm
4	AGND	Audio Ground		
5	B GND	RGB Blue Ground		
6	AIL	Audio In Left + Mono	0.5 V rms	>10k ohm
7	B	RGB Blue In	0.7 V	75 ohm
8	SWTCH	Audio/RGB switch / 16:9	0-2 V=TV, 5-8 V=WideScreen, 9.5-12 V=AV Mode	>10 kohm
9	G GND	RGB Green Ground		
10	CLKOUT	Data 2: Clockpulse Out (Unavailable ??)		
11	G	RGB Green In	0.7 V	75 ohm
12	DATA	Data 1: Data Out (Unavailable ??)		
13	R GND	RGB Red Ground		
14	DATAGND	Data Ground		

15	R	RGB Red In / Chrominance	0.7 V (Chrom.: 0.3 V burst)	75 ohm
16	BLNK	Blanking Signal	1-3 V=RGB, 0-0.4 V=Composite	75 ohm
17	VGND	Composite Video Ground		
18	BLNKGND	Blanking Signal Ground		
19	VOUT	Composite Video Out	1 V	75 ohm
20	VIN	Composite Video In / Luminance	1 V	75 ohm
21	SHIELD	Ground/Shield (Chassis)		

Contributor: [Joakim Ögren](#)

Source:

Various sources, Video Demystified at Keith Jack's pages, [SES: The SCART Interface](#)

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Document last modified: 2001-06-08



# TurboVision Turbo Express TV Tuner

Available on the Nintendo N64.



(at the TurboVision)

TURBOVISION TV FEMALE CONNECTOR at the TurboVision.

Pin	Name	Description	Wire Colour
1	GND	Ground	brown
2	tvsnd	Sound Output	blue
3	V-5	+5v Input	yellow
4	G	Green Out	orange
5	R	Red Video	black
6	B	Blue	red
7	csync	Composite Sync	grey
8	V-30	???	white

Contributor: [Joakim Ögren](#)

Source:

[TurboVision Turbo Express TV Tuner Pinout](#) at [GamesX](#)

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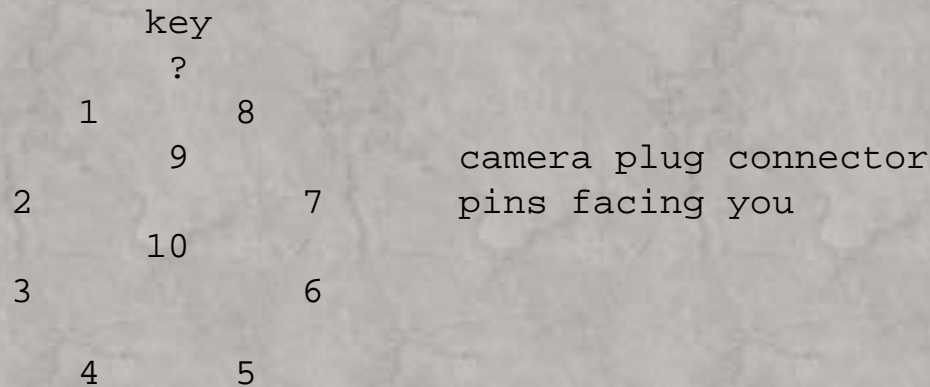
Document last modified: 2001-06-07





# VHS Video Camera

## 10 PIN UNKNOWN CONNECTOR



There seems to be no clear standard for VHS Video Cameras. Column "Name" is the most common function. Three alternative functions that could apply for some cameras is presented in columns named "Alt Name X".

Pin	Name	Alt Name 1	Alt Name 2	Alt Name 3
1	video out	video in/out		
2	video gnd			
3		serial data		
4		tally and clock	reset in	
5		audio out right	standby out	audio in
6	pause			
7	audio out	audio out left		
8	audio gnd			
9	power gnd			
10	+12V power			

Contributor: [Joakim Ögren](#), [Mike Turner](#), Mike N3EZD

Source:

*[VHS Video Camera 10 pin pinout](#) at [Baltimore Radio Amateur Television Society Pinouts FAQ](#) at [Sci.Electronics.Repair FAQ](#)*

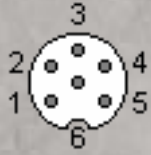
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# Amstrad CPC6128 Monitor



(at the computer)

6 PIN DIN (DIN45322) FEMALE at the computer.

Pin	Name
1	RED
2	GREEN
3	BLUE
4	SYNC
5	GND
6	LUM

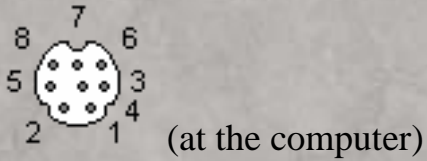
Contributor: [Joakim Ögren](#), [Agnello Guarracino](#)

Source:  
*Amstrad CPC6128 User Instructions Manual*

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*Document last modified: 2001-06-07*



# Amstrad CPC6128 Plus Monitor



8 PIN MINI-DIN FEMALE at the computer.

Pin	Name	Dir	Description
1	NSYNC	→	Sync?
2	GREEN	→	Green
3	LUM	→	Luminance
4	RED	→	Red
5	BLUE	→	Blue
6	AOL	→	Audio Output Left
7	AOR	→	Audio Output Right
8	GND	→	Ground

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#), [Colin Gaunt](#)

Source:  
Amstrad 6128 Plus Home Computer Manual


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Document last modified: 2001-06-07



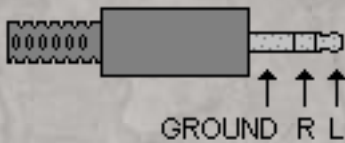


# Amstrad CPC6128 Stereo

**NOT  
DRAWN  
YET...**



(at the computer)



(at the cable)

3.5 mm STEREO TELEPHONE FEMALE at the computer.

3.5 mm STEREO TELEPHONE MALE at the cable.

Pin	Description
L	Left Channel
R	Right Channel
GND	Ground

Contributor: [Joakim Ögren](#), [Agnello Guarracino](#)

Source:  
*Amstrad CPC6128 User Instructions Manual*

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Document last modified: 2001-06-07



# Atari Falcon030 RGB/VGA

19 PIN UNKNOWN CONNECTOR (Cannon 19 pin Male?) on the Computer.

Pin	Description
1	Red
2	Green
3	Blue
4	Monochrome / Overlay
5	Ground
6	Red Ground
7	Green Ground
8	Blue Ground
9	Audio Out
10	Ground
11	Ground
12	Composite Sync
13	Horizontal Sync
14	Vertikal Sync
15	External Clock Input
16	External Sync Enable
17	+12V for Scart
18	Videomode 1
19	Videomode 2

## Settings:

M0	M1	Monitor
----	----	---------

0	0	mono
0	1	VGA
1	0	RGB
1	1	TV via CINCH

*Contributor:* [Joakim Ögren](#) Jan Krupka

*Source:*  
?

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*Document last modified:* 2000-07-11



# Atari ST Monitor Connector

**NOT  
DRAWN  
YET...**



(at the Computer)

**NOT  
DRAWN  
YET...**



(at the Devices)

13 PIN DIN FEMALE at the Computer.

13 PIN DIN MALE at the Devices.

Pin	Name	Description
1	AO	Audio Out
2	CVIDEO	Composite Video
3	CS	Clock Select
4	MD	Monochrome Detect / Clock In
5	AI	Audio In
6	G	Green
7	R	Red
8	+12V	+12 VDC (520ST has GND)
9	HSYNC	Horizontal Sync
10	B	Blue
11	MVIDEO	Monochrome Video
12	VSNC	Vertical Sync
13	GND	Ground

Contributor: [Joakim Ögren](#), [Lawrence Wright](#), [Steve & Sally Blair](#)

Source:



?

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# C128 RGBI



(at the Computer)

9 PIN D-SUB FEMALE at the Computer.

Pin	Name	Dir	Description
1	GND	—	Ground
2	GND	—	Ground
3	R	→	Red
4	G	→	Green
5	B	→	Blue
6	I	→	Intensity
7	VIDEO	→	Composite Video
8	HSYNC	→	Horizontal Sync
9	VSYNC	→	Vertical Sync

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#)

Source:

Usenet posting in comp.sys.cbm, C128 screen cables by [Marko Makela](#)

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Document last modified: 2001-06-08



# C128/C64C Video

Seems to be available on the C128 and the C64C (white color). Compatible with cables for the 5 pin D-SUB on C64's.



(at the Computer)

8 PIN DIN (DIN45326) FEMALE at the Computer.

Pin	Name	Dir	Description
1	LUM	→	Luminance (monochrome video)
2	GND	—	Ground
3	AOUT	→	Audio out
4	VOUT	→	Composite Video out
5	AIN	←	Audio in (into the SID chip)
6	n/c	-	Not connected
7	n/c	-	Not connected
8	C	→	Chroma

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#)

Source:  
CBM Memorial Page Pinouts

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# C16/C116/+4 Audio/Video

Available on Commodore C16/C116/+4 computers.



(at the Computer)

8 PIN DIN (DIN45326) FEMALE at the Computer.

Pin	Name	Dir	Description
1	LUM	→	Luminance (monochrome video)
2	GND	—	Ground
3	AOUT	→	Audio out
4	VOUT	→	Composite Video out
5	AIN	←	Audio in (into the SID chip)
6	COLOR	-	Color ?
7	n/c	-	Not connected
8	+5VDC	→	+5 VDC

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#), [Arwin Vosselman](#)

Source:

CBM Memorial Page Pinouts

SAMS Computerfacts CC8 Commodore 16

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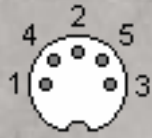
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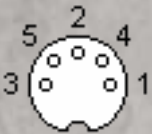




# C64 Audio/Video



(at the computer)



(at the cable)

5 PIN DIN 180° (DIN41524) FEMALE at the Computer.

5 PIN DIN 180° (DIN41524) MALE at the Cable.

Pin	Name	Dir	Description
1	LUM	→	Luminance
2	GND	—	Ground
3	AOUT	→	Audio Out
4	VOUT	→	Video Out
5	AIN	←	Audio In

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#)

Source:  
?

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# C65 Video

Available on the Commodore C65 computer.



(at the Computer)

9 PIN D-SUB MALE at the Computer.

Pin	Name	Dir	Description
1	GND	—	Ground
2	?		?
3	R	→	Red
4	G	→	Green
5	B	→	Blue
6	?		?
7	CSYNC	→	Composite Sync
8	HSYNC	→	Horizontal Sync
9	VSNC	→	Vertical Sync

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#)

Source:  
CBM Memorial Page Pinouts

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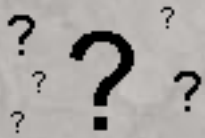


# CDTV Video Slot

```

  2   4   6   8  10  12  14  16  18  20  22  24  26  28  30
-- -- -- -- -- -- -- -- -- -- -- -- -- -- --
-- -- -- -- -- -- -- -- -- -- -- -- -- -- --
  1   3   5   7   9  11  13  15  17  19  21  24  25  27  29

```



(at the computer)

30 PIN ??? CONNECTOR at the computer.

Pin	Name	Description
1	GND	Video Ground
2	GND	Video Ground
3	XCLK	External Genlock Clock (in)
4	R	Red (in to video card)
5	/XCLKEN	Enables External Clock on XCLK.
6	BR	Buffered Red (out from video card)
7	GND	Video Ground
8	G	Green (in to video card)
9	GMS0	Genlock mode 0 (from computer, genlock button)
10	BG	Buffered Green (out from video card)
11	GMS1	Genlock mode 1 (from computer, genlock button)
12	B	Blue (in to video card)
13	/PIXELSW	Genlock signal
14	BB	Buffered Blue (out from video card)
15	VSYNC	Vertical Sync (in to video card)
16	CSYNC	Horizontal Sync (in to video card)

17	HSYNC	Composite Sync (in to video card)
18	BCSYNC	Buffered Composite Sync (out from video card)
19	GND	Video Ground
20	AUDR	Audio Right Output (from computer to RF modulator)
21	DGND	Digital Ground
22	AUDL	Audio Left Output (from computer to RF modulator)
23	-12V	-12 VDC (can be -5 VDC instead)
24	DGND	Digital Ground
25	+12V	+12 VDC
26	/CD/TV	CD/TV button. (Low=CDTV video on RF, High=Antenna)
27	VCC	+5 VDC
28	/CCK	3.58 MHz color clock (C1 clock)
29	GND	Video Ground
30	VCC	+5 VDC

*Note: Used for RF-modulator usually.*

*Contributor: [Joakim Ögren](#)*

*Source:  
Darren Ewaniuk's CDTV Technical Information*

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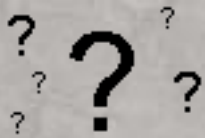




# CM-8/CoCo RGB

Available on the Tandy/Radio Shack Color Computer (CoCo).

```
+-----+
| 1 3 5 7 9 |
| 2 4     8 10|
+-----+
```



(at the CoCo)

UNKNOWN CONNECTOR at the CoCo.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	R	Red
4	G	Green
5	B	Blue
6	KEY	No Pin
7	AUDIO	Audio
8	HSYNC	Horizontal Sync
9	VSYNC	Vertical Sync
10	n/c	No Connection

Contributor: [Joakim Ögren](#)

Source:

[Tandy Color Computer FAQ](#) at [Video Game Advantage's homepage](#)

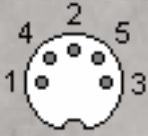
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# Spectravideo SVI318/328 Audio/Video



(at the computer)

5 PIN DIN 180° (DIN41524) FEMALE at the computer.

Pin	Name	Description
1	+5v	Power
2	GND	System ground
3	AUDIO	Audio out
4	VIDEO	Composite Video out
5	RF VID	RF Video out

Contributor: [Rob Gill](#)

Source:  
*Spectravideo SVI 328 mk II User Manual*

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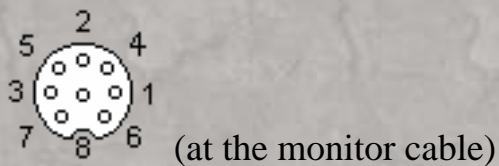
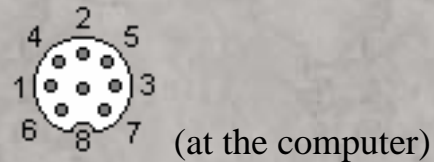
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# ZX Spectrum 128 RGB

Can be found at the Sinclair ZX Spectrum 128.



8 PIN DIN (DIN45326) FEMALE at the computer.

8 PIN DIN (DIN45326) MALE at the monitor cable.

Pin	Name	Dir	Description
1	CVBS	→	Composite Video (PAL, 75 ohms, 1.2V p-p)
2	GND	—	Ground
3	BOUT	→	Bright Output
4	CSYNC	→	Composite Sync
5	VSNC	→	Vertical Sync
6	G	→	Green
7	R	→	Red
8	B	→	Blue

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#)

Source:  
Online ZX Spectrum 128 Manual Page 3

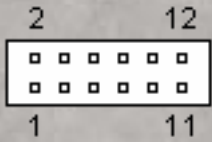
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# 3b1/7300 Video



(at the computer)

12 PIN IDC MALE at the computer.

Pin	Name	Description
1	VSYNC	Vertical Sync
2	GND	Ground
3	HSYNC	Horizontal Sync
4	GND	Ground
5	VIDEO	Video
6	GND	Ground
7	+12V	+12 VDC
8	GND	Ground
9	+12V	+12 VDC
10	SPK	Speaker
11	SPK	Speaker
12	?	?

Contributor: [Joakim Ögren](#)

Source:  
[Tommy's pinout Collection](#) by [Tommy Johnson](#)

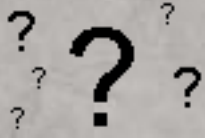
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# Amiga 1000 RF Modulator



(at the motherboard)

UNKNOWN CONNECTOR at the motherboard.

Pin	Name
1	N.C.
2	GND
3	AUDIO LEFT
4	COMP VIDEO
5	GND
6	N.C.
7	+12V
8	AUDIO RIGHT

Contributor: [Joakim Ögren](#)

Source:

[Amiga 1000 RF Modulator pinout](#) at [National Amiga](#)

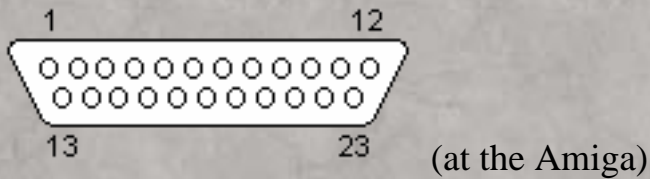
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# Amiga Video



23 PIN D-SUB MALE at the Amiga.

Pin	Name	Dir	Description
1	/XCLK	←	Extern Clock
2	/XCLKEN	←	Extern Clock Enable (47 Ohm)
3	RED	→	Analog Red (75 Ohm)
4	GREEN	→	Analog Green (75 Ohm)
5	BLUE	→	Analog Blue (75 Ohm)
6	DI	→	Digital Intensity (47 Ohm)
7	DR	→	Digital Red (47 Ohm)
8	DG	→	Digital Green (47 Ohm)
9	DB	→	Digital Blue (47 Ohm)
10	/CSYNC	→	Composite Sync (47 Ohm)
11	/HSYNC	→	Horizontal Sync (47 Ohm)
12	/VSYNC	→	Vertical Sync (47 Ohm)
13	GNDRTN	—	Digital Ground (for /XCLKEN) Don't connect with pin 16-20.
14	/PIXELSW	→	Genlock overlay (47 Ohm)
15	/C1	→	Clock out (47 Ohm)
16	GND	—	Video Ground
17	GND	—	Video Ground
18	GND	—	Video Ground
19	GND	—	Video Ground
20	GND	—	Video Ground



21	-12V		-12 Volts DC (10 mA max) (A500/A600/A1200)
	-5V		-5 Volts DC (10 mA max) (A1000/A2000/A3000/A4000)
22	+12V		+12 Volts DC (100 mA max)
23	+5V		+5 Volts DC (100 mA max)

*Note: Direction is Computer relative Monitor.*

*Contributor: [Joakim Ögren](#)*

*Source:  
Amiga 4000 User's Guide from Commodore*

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Document last modified: 2000-05-28*



# Apple II Video Expansion

## 15 PIN UNKNOWN CONNECTOR

Pin	Name	Description
1	TEXT	Video text signal from TMG; set to inverse of GR, except in double high-resolution mode.
2	14M	14M master timing signal from the system oscillator.
3	SYNC*	Displays horizontal and vertical synchronization signal from IOU pin 39.
4	SEGB	Displays vertical counter bit from IOU pin 4; in text mode, indicates second low-order vertical counter; in graphics mode, indicates low-resolution.
5	1VSOUND	One-volt sound signal from pin 5 of the audio hybrid circuit (AUD).
6	LDPS*	Video shift-register load enable from pin 12 of TMG.
7	WNDW*	Active area display blanking; includes both horizontal and vertical blanking.
8	+12V	Regulated +12 volts DC; can drive 300mA.
9	PRAS*	RAM row-address strobe from TMG pin 19.
10	GR	Graphics mode enable from IOU pin 2.
11	SEROUT*	Serialized character generator output from pin 1 of the 74LS166 shift register.
12	NTSC	Composite NTSC video signal from VID hybrid chip.
13	GND	Ground reference and supply.
14	VIDD7	From 74LS374 video latch; causes half-dot shift high.
15	CREF	Color reference signal from TMG pin 3; 3.58 MHz.

### Note:

*The signals at the DB-15 on the Apple IIc are not the same as those at the DB-15 end of the Apple III, Apple IIIGS, and Macintosh II. Do not attempt to plug a cable intended for one into the other.*

### Note:

*Several of these signals, such as the 14 MHz, must be buffered within about 4 inches of the back panel connector--preferably inside a container directly connected to the back panel.*

*Contributor:* [Joakim Ögren](#)

*Source:*

[Apple Tech Info Library 1419: Apple IIc, External Pinouts](#) at [Apple TIL homepage](#)

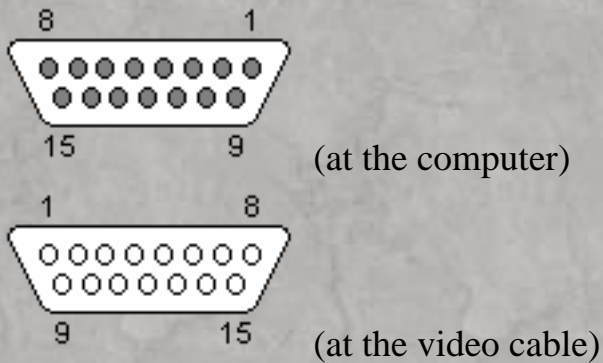
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*Document last modified:* 2000-07-08



# Apple Macintosh II/IIci Video



15 PIN D-SUB FEMALE at the computer.

15 PIN D-SUB MALE at the video cable.

Available on Macintosh II Video Cards and the Macintosh IIci built-in video

Pin	Name	Description
1	RED.GND	Red ground
2	RED.VID	Red video signal
3	/CSYNC	Composite synchronization signal
4	SENSE0	Monitor sense signal 0
5	GRN.VID	Green video signal (with sync)
6	GRN.GND	Green ground
7	SENSE1	Monitor sense signal 1
8	n/c	Not connected
9	BLU.VID	Blue video signal
10	SENSE2	Monitor sense signal 2
11	C&VSYNC.GND	Ground for CSYNC & VSYNC
12	/VSYNC	Vertical synchronization signal
13	BLU.GND	Blue ground
14	HSYNC.GND	HSYNC ground



15	/HSYNC	Horizontal synchronization signal
Shell	CHASSIS.GND	Chassis ground

Contributor: [Joakim Ögren](#)

Source:

[Technote HW08: Color Monitor Connections](#) at [Apple Technical Notes](#)

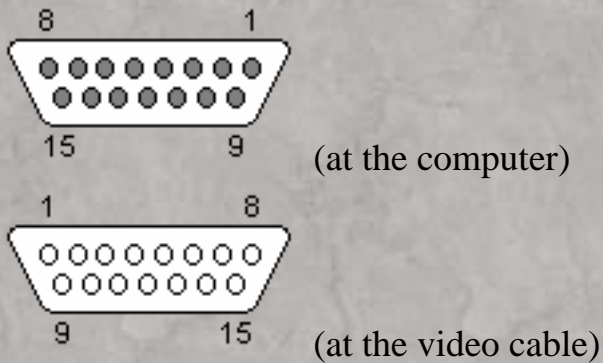
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# Apple Macintosh LC External Video



15 PIN D-SUB FEMALE at the computer.

15 PIN D-SUB MALE at the video cable.

Available on Apple Macintosh LC

Pin	Name	Description
1	RED.GND	Red ground
2	RED.VID	Red video signal
3	/CSYNC	Composite synchronization signal
4	SENSE0	Monitor sense signal 0
5	GRN.VID	Green video signal
6	GRN.GND	Green ground
7	SENSE1	Monitor sense signal 1 (grounded internally)
8	n/c	Not connected
9	BLU.VID	Blue video signal
10	SENSE2	Monitor sense signal 2
11	C&VSYNC.GND	Ground for CSYNC & VSYNC
12	/VSYNC	Vertical synchronization signal
13	BLU.GND	Blue ground
14	HSYNC.GND	HSYNC ground

15	/HSYNC	Horizontal synchronization signal
Shell	CHASSIS.GND	Chassis ground

Contributor: [Joakim Ögren](#)

Source:

[Technote HW08: Color Monitor Connections](#) at [Apple Technical Notes](#)

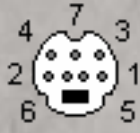
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# Apple S-Video Input



(at the computer)

7 PIN SPECIAL MINI-DIN FEMALE at the computer.

Available on Apple Power Macintosh 6100AV/7100AV/8100AV

Pin	Description
1	Analog GND
2	Analog GND
3	Video Y (Luminance)
4	Video C (Chroma)
5	I2C Clock
6	+12 VDC (max 250mA)
7	I2C Data

Contributor: [Joakim Ögren](#)

Source:

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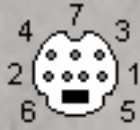
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# Apple S-Video Output



(at the computer)

7 PIN SPECIAL MINI-DIN FEMALE at the computer.

Available on Apple Power Macintosh 6100AV/7100AV/8100AV and Apple PowerBook

Pin	Description
1	Analog GND
2	Analog GND
3	Video Y (Luminance)
4	Video C (Chroma)
5	Composite Video
6	Unused
7	Unused

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# Apple Video Mirror

Available on Apple Power Macintosh 5400

Fullname: Optional Video Display Mirror Output Feature

## 22 PIN UNKNOWN CONNECTOR

Pin	Name	Description
1	VID.GND	Video ground
2	RED	Red signal
3	GREEN	Green signal
4	VID.GND	Video ground
5	VID.GND	Video ground
6	BLUE	Blue signal
7	CSYNC	C sync
8	VSYNC	Vertical sync
9	MLB.SYNC.EN.L	Not used (reserved)
10	HSYNC	Horizontal sync
11	DAC.ISET.1	Not used(reserved)
12	DAC.ISET.2	Not used (reserved)
13	SND.GND	Not used (reserved)
14	SND.RIGHT	Not used (reserved)
15	SND.LEFT	Not used (reserved)
16	+5V	+5 volts
17	GND	Ground
18	SDAT	Not used (reserved)
19	SCLK	Not used (reserved)
20	+12V	+12 volts
21	-12V	-12 volts

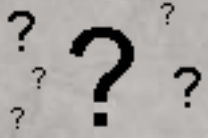
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# AT&T 53D410



(at the computer)

25 PIN D-SUB ??? at the computer.

Pin	Name	Description
1	?	?
2	VSYNC	Vertical Sync
3	HSYNC	Horizontal Sync
4	?	?
5	VIDEO	Video
6	?	?
7	?	?
8	?	?
9	?	?
10	?	?
11	?	?
12	?	?
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	?	?
17	?	?
18	?	?
19	?	?
20	?	?



21	?	?
22	?	?
23	?	?
24	?	?
25	?	?

Contributor: [Joakim Ögren](#)

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# AT&T 6300 Taxan Monitor



(at the Monitor)

8 PIN DIN (DIN45326) FEMALE at the Monitor.

Pin	Name	Description
1	TEXT	Special TEXT signal (??)
2	R	Red
3	G	Green
4	B	Blue
5	I	Intensity
6	GND	Signal Ground
7	HSYNC/CSYNC	Horizontal or Composite Sync
8	VSNC	Vertical Sync

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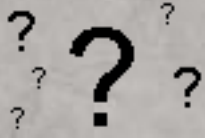
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# AT&T PC6300



(at the computer)

25 PIN D-SUB ??? at the computer.

Pin	Name	Description
1	HSYNC	Horizontal Sync
2	ID0	Monitor ID 0
3	VSYNC	Vertical Sync
4	R	Red
5	G	Green
6	B	Blue
8	n/c	Not connected
9	n/c	Not connected
10	ID1	Monitor ID 1
11	MODE0	Mode 0
12	n/c	Not connected
13	/DEGAUSS	Degauss
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground

22	n/c	Not connected
23	n/c	Not connected
24	+15V	+15 VDC
25	+15V	+15 VDC

Monochrome monitor: ID0 and ID1 are open

Color monitor: ID0 is 0, and ID1 is 1, probably 5V, not 15V

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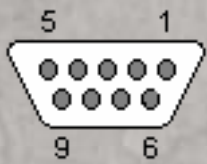


# CGA

CGA=Color Graphics Adapter.

Videotype: TTL, 16 colors.

Also known as IBM RGBI.



(at the videocard)



(at the monitor cable)

9 PIN D-SUB FEMALE at the videocard.

9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	R	Red
4	G	Green
5	B	Blue
6	I	Intensity
7	RES	Reserved
8	HSYNC	Horizontal Sync
9	VSYNC	Vertical Sync

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# Commodore 1084 & 1084S (Analog) Connector



(at the Monitor)

6 PIN DIN FEMALE at the Monitor.

Pin	Name	Description
1	G	Green
2	HSYNC	Horizontal Sync
3	GND	Ground
4	R	Red
5	B	Blue
6	VSYNC	Vertical Sync

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# Commodore 1084 & 1084S (Digital)



(at the Monitor)

8 PIN DIN 'C' FEMALE at the Monitor.

Pin	Name	Description
1	n/c	Not connected
2	R	Red
3	G	Green
4	B	Blue
5	I	Intensity
6	GND	Ground
7	HSYNC	Horizontal Sync
8	VSYNC	Vertical Sync

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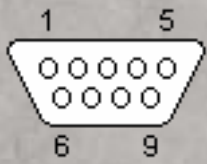
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# Commodore 1084d & 1084dS



(at the Monitor)

9 PIN D-SUB FEMALE at the Monitor.

Pin	Name	Analog Mode	Digital Mode
1	GND	Ground	Ground
2	GND	Ground	Ground
3	R	Red	Red
4	G	Green	Green
5	B	Blue	Blue
6	I	n/c	Intensity
7	CSYNC	Composite Sync	n/c
8	HSYNC	n/c	Horizontal Sync
9	VSYNC	n/c	Vertical Sync

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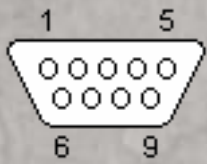
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# ECL



(at the videocard)



(at the monitor cable)

9 PIN D-SUB FEMALE at the videocard.

9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	ECL	ECL?
2	ECLGND	ECL Video Ground
3	HSYNC	Horizontal Sync
4	VSNC	Vertical Sync
5	+5V	+5 VDC
6	ECLGND	ECL Video Ground
7	ECLGND	ECL Video Ground
8	SYNCGND	Sync Ground
9	+5GND	Ground (for +5V)

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# EGA

EGA=Enhanced Graphics Adapter.

Videotype: TTL, 16/64 colors.



(at the videocard)



(at the monitor cable)

9 PIN D-SUB FEMALE at the videocard.

9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	GND	Ground
2	SR	Secondary Red
3	PR	Primary Red
4	PG	Primary Green
5	PB	Primary Blue
6	SG/I	Secondary Green / Intensity
7	SB	Secondary Blue
8	H	Horizontal Sync
9	V	Vertical Sync

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# IBM PCjr CGA

CGA=Color Graphics Adapter.

18 PIN BERG STYLE CONNECTOR ???

Pin	Description
A01	TV vertical drive (not for display)
A02	Ground
A03	TV horizontal drive (not for display)
A04	Blue (CGA pin 5)
A05	Red (CGA pin3)
A06	Intensity (CGA pin 6)
A07	Green (CGA pin 4)
A08	Comp Sync Drive (not for display)
A09	Audio
B01	+ Vertical drive (CGA pin 9)
B02	Ground
B03	+ Horizontal drive (CGA pin 8)
B04	Ground
B05	Ground
B06	Ground
B07	Ground
B08	Ground
B09	Frame ground (CGA pin 1)

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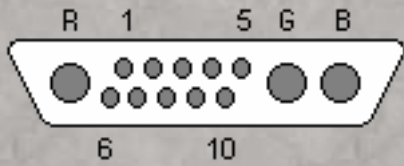
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# IBM PowerPC Video



(at the Computer)

13 PIN 13W3 FEMALE at the Computer.

Pin	Description
1	ID Bit 2
2	ID Bit 3
3	Self test
4	Digital Ground
5	Horizontal Sync
6	ID Bit 0
7	ID Bit 1
8	n/c
9	Vertical Sync
10	Digital Ground

Contributor: [Joakim Ögren](#)

Source:  
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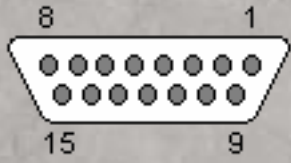
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# Macintosh Video



(at the Computer)

15 PIN D-SUB FEMALE at the Computer.

Pin	Name	Dir	Description
1	RGND	—	Red Ground
2	R	→	Red
3	CSYNC	→	Composite sync
4	SENSE0	←	Monitor Sense 0
5	G	→	Green
6	GGND	—	Green Ground
7	SENSE1	←	Monitor Sense 1
8	n/c	-	No connection
9	B	→	Blue
10	SENSE2	←	Monitor sense 2
11	SGND	—	Sync Ground
12	VSYNC	→	Vertical Sync
13	BGND	—	Blue Ground
14	HSYNCGND	—	Horizontal Sync Ground
15	HSYNC	→	Horizontal Sync

*Note: Direction is Computer relative Monitor.*

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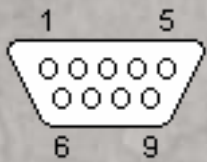
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# MDA (Hercules)



(at the videocard)



(at the monitor cable)

9 PIN D-SUB FEMALE at the videocard.

9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	n/c	
4	n/c	
5	n/c	
6	I	Intensity
7	M	Mono Video
8	H	Horizontal Sync
9	V	Vertical Sync

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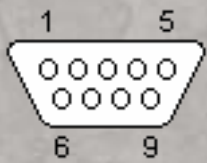


# Monochrome TTL Video

(18.43 KHz - 720x350)



(At the videocard)



(At the monitor cable)

9 PIN D-SUB FEMALE at the videocard.

9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	GND	Ground
2	-	-
3	-	-
4	-	-
5	-	-
6	I	Intensity
7	VID	Video
8	HSYNC	Horizontal Sync TTL Positive
9	VSYNC	Vertical Sync TTL Negative

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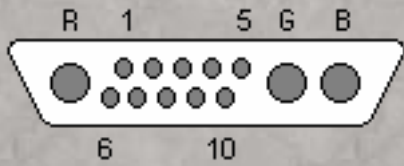
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# NeXT Color Video



(at the Computer)

13 PIN 13W3 FEMALE at the Computer.

Pin	Description
1	+12 VDC
2	Power Switch Control
3	Monitor Clock
4	Monitor Out
5	Monitor In
6	-12 VDC
7	Monitor Type 2
8	Ground
9	Ground
10	Ground

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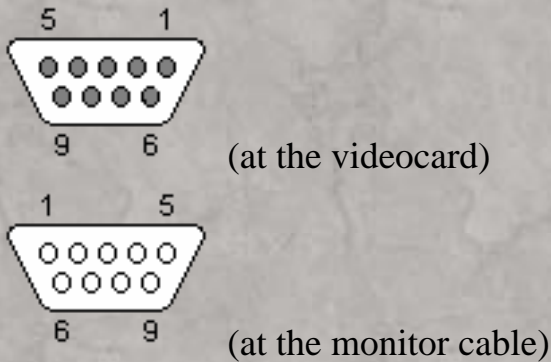
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# PGA

Videotype: Analogue.



9 PIN D-SUB FEMALE at the videocard.

9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Description
1	R	Red
2	G	Green
3	B	Blue
4	CSYNC	Composite Sync
5	MODE	Mode Control
6	RGND	Red Ground
7	GGND	Green Ground
8	BGND	Blue Ground
9	GND	Ground

Contributor: [Joakim Ögren](#)

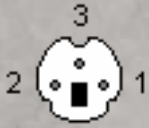
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# SGI StereoView (3 pin)



(at the computer)

3 PIN MINI-DIN FEMALE at the computer.

Pin	Description
1	STEREO POWER (+12V, 0.5A)
2	STEREO GROUND
3	VERTICAL - ODD FIELD (1=Left, 0=Right)

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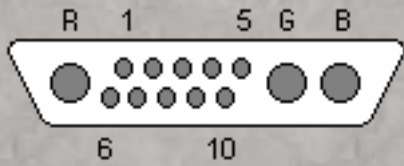
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# SGI Video



(at the Computer)

13 PIN 13W3 FEMALE at the Computer.

## Normal Monitor

Pin	Description
1	Monitor ID Bit 3, TTL
2	Monitor ID Bit 0, TTL
3	Composite Sync (Active Low), TTL
4	Horizontal Drive (Active High), TTL
5	Vertical Drive (Active High), TTL
6	Monitor ID Bit 1, TTL
7	Monitor ID Bit 2, TTL
8	Digital Ground
9	Digital Ground
10	Sync Ground

## DDC Monitor

Pin	Description
1	Data Clock (SCL)
2	Bi-directional Data (SDA)
3	Composite Sync

4	Horizontal Sync
5	Vertical Sync
6	DDC (+5VInput)
7	DDC Ground
8	Chassis Ground
9	Chassis Ground
10	Chassis Ground
R	Red
G	Green
B	Blue

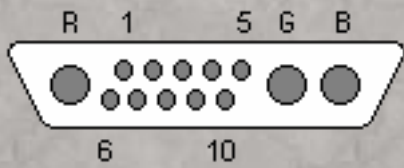
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# Sun Video



(at the Computer)

13 PIN 13W3 FEMALE at the Computer.

Pin	Name	Description
1	HSYNCGND	Horizontal Sync Ground*
2	VSYNC	Vertical Sync*
3	SENSE2	Sense #2
4	SENSEGND	Sense Ground
5	CSYNC	Composite Sync
6	HSYNC	Horizontal Sync*
7	VSYNCGND	Vertical Sync Ground*
8	SENSE1	Sense #1
9	SENSE0	Sense #0
10	CGND	Composite Ground
R	RED	Red
G	GREEN/GRAY	Green/Gray
B	BLUE	Blue

\*) Considered obsolete, may not be connected.

Monitor-sense bits defined as:

Value	Bit 2	Bit 1	Bit 0	Resolution
0	0	0	0	?
1	0	0	1	Reserved

2	0	1	0	1280 x 1024 76Hz
3	0	1	1	1152 x 900 66Hz
4	1	0	0	1152 x 900 76Hz 19"
5	1	0	1	Reserved
6	1	1	0	1152 x 900 76Hz 16-17"
7	1	1	1	No monitor connected

See <http://cvs.anu.edu.au:80/monitorconversion/> for info on attaching old workstation monitors to VGA boards.

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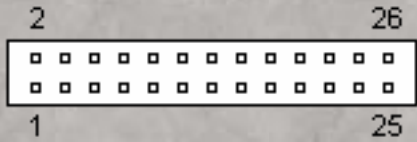
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# VESA Feature



(at the videocard)

26 PIN IDC at the Video card.

Pin	Name	Description
1	PD0	DAC Pixel Data Bit 0 (PB)
2	PD1	DAC Pixel Data Bit 1 (PG)
3	PD2	DAC Pixel Data Bit 2 (PR)
4	PD3	DAC Pixel Data Bit 3 (PI)
5	PD4	DAC Pixel Data Bit 4 (SB)
6	PD5	DAC Pixel Data Bit 5 (SG)
7	PD6	DAC Pixel Data Bit 6 (SR)
8	PD7	DAC Pixel Data Bit 7 (SI)
9	CLK	DAC Clock
10	BLK	DAC Blanking
11	HSYNC	Horizontal Sync
12	VSYNC	Vertical Sync
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17		Select Internal Video
18		Select Internal Sync
19		Select Internal Dot Clock
20	n/c	Not used

21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	n/c	Not used
26	n/c	Not used

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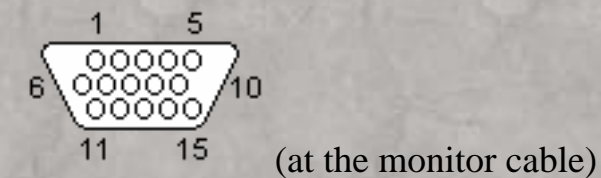
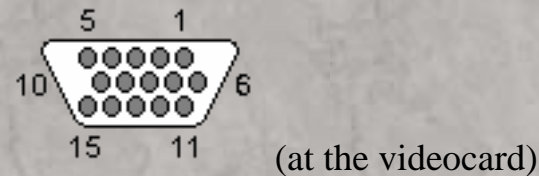
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# VGA (15)

VGA=Video Graphics Adapter or Video Graphics Array.

Videotype: Analogue.



15 PIN HIGHDENSITY D-SUB FEMALE at the videocard.

15 PIN HIGHDENSITY D-SUB MALE at the monitor cable.

Pin	Name	Dir	Description
1	RED		Red Video (75 ohm, 0.7 V p-p)
2	GREEN		Green Video (75 ohm, 0.7 V p-p)
3	BLUE		Blue Video (75 ohm, 0.7 V p-p)
4	ID2		Monitor ID Bit 2
5	GND		Ground
6	RGND		Red Ground
7	GGND		Green Ground
8	BGND		Blue Ground
9	KEY	-	Key (No pin)
10	SGND		Sync Ground
11	ID0		Monitor ID Bit 0
12	ID1 or SDA		Monitor ID Bit 1
13	HSYNC or CSYNC		Horizontal Sync (or Composite Sync)
14	VSYNC		Vertical Sync

15 ID3 or SCL



Monitor ID Bit 3

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# VGA (9)

VGA=Video Graphics Adapter or Video Graphics Array.

Videotype: Analogue.



(at the videocard)



(at the monitor cable)

9 PIN D-SUB FEMALE at the videocard.

9 PIN D-SUB MALE at the monitor cable.

Pin	Name	Dir	Description
1	RED		Red Video
2	GREEN		Green Video
3	BLUE		Blue Video
4	HSYNC		Horizontal Sync
5	VSYNC		Vertical Sync
6	RGND		Red Ground
7	GGND		Green Ground
8	BGND		Blue Ground
9	SGND		Sync Ground

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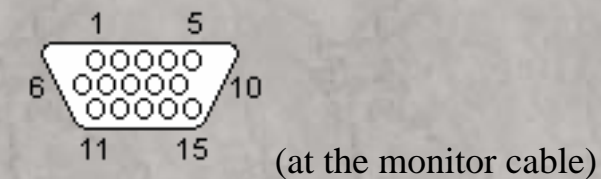
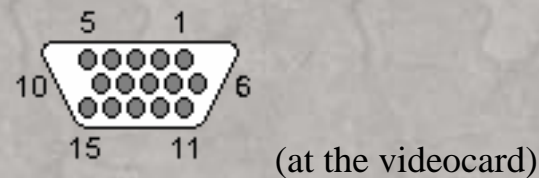
# VGA (VESA DDC)

VGA=Video Graphics Adapter or Video Graphics Array.

VESA=Video Electronics Standards Association.

DDC=Display Data Channel.





Videotype: Analogue.



15 PIN HIGHDENSITY D-SUB FEMALE at the videocard.

15 PIN HIGHDENSITY D-SUB MALE at the monitor cable.

Pin	Name	Dir	Description
1	RED		Red Video (75 ohm, 0.7 V p-p)
2	GREEN		Green Video (75 ohm, 0.7 V p-p)
3	BLUE		Blue Video (75 ohm, 0.7 V p-p)
4	RES	-	Reserved
5	GND		Ground
6	RGND		Red Ground
7	GGND		Green Ground
8	BGND		Blue Ground
9	+5V		+5 VDC
10	SGND		Sync Ground
11	ID0		Monitor ID Bit 0 (optional)

12	SDA		DDC Serial Data Line
13	HSYNC or CSYNC		Horizontal Sync (or Composite Sync)
14	VSYNC		Vertical Sync
15	SCL		DDC Data Clock Line

*Note: Direction is Computer relative Monitor.*

*Contributor: [Joakim Ögren](#)*

*Source:*

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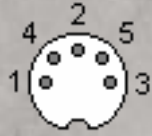
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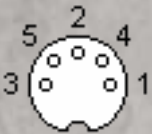




# Vic 20 Video



(at the computer)



(at the cable)

5 PIN DIN 180° (DIN41524) FEMALE at the Computer.

5 PIN DIN 180° (DIN41524) MALE at the Cable.

Pin	Name	Dir	Description
1	+6V	→	+6 VDC (10 mA max)
2	GND	→	Ground
3	AUDIO	→	Audio
4	VLOW	→	Video Low (Unconnected ?)
5	VHIGH	→	Video High

*Note: Direction is Computer relative Monitor.*

Contributor: [Joakim Ögren](#)

Source:  
CBM Memorial Page Pinouts

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# Accelerated Graphics Port (AGP)

AGP=Accelerated Graphics Port

**NOT  
DRAWN  
YET...**



(at the computer)

132 PIN EDGE CONNECTOR at the computer.

Pin	Name
A1	+12 V dc
A2	spare
A3	Reserved* Ground
A4	USB-
A5	Ground
A6	INTA#
A7	RST#
A8	GNT#
A9	VCC 3.3
A10	ST1
A11	Reserved
A12	PIPE#
A13	Ground
A14	Spare
A15	SBA1
A16	VCC 3.3
A17	SBA3
A18	Reserved

A19	Ground
A20	SBA5
A21	SBA7
A22	Key
A23	Key
A24	Key
A25	Key
A26	AD30
A27	AD28
A28	VCC 3.3
A29	AD26
A30	AD24
A31	Ground
A32	Reserved
A33	C/BE3#
A34	Vddq 3.3
A35	AD22
A36	AD20
A37	Ground
A38	AD18
A39	AD16
A40	Vddq 3.3
A41	FRAME#
A42	Spare
A43	Ground
A44	Spare
A45	VCC 3.3
A46	TRDY#
A47	STOP#
A48	Spare
A49	Ground
A50	PAR

A51	AD15
A52	Vddq 3.3
A53	AD13
A54	AD11
A55	Ground
A56	AD9
A57	C/BE0#
A58	Vddq 3.3
A59	Reserved
A60	AD6
A61	Ground
A62	AD4
A63	AD2
A64	Vddq 3.3
A65	AD0
A66	SMB1
B1	spare
B2	+5 V dc
B3	+5 V dc
B4	USB+
B5	Ground
B6	INTB#
B7	CLK
B8	REQ#
B9	VCC 3.3
B10	ST0
B11	ST2
B12	RBF#
B13	Ground
B14	Spare
B15	SBA0
B16	VCC 3.3



B17	SBA2
B18	SB_STB
B19	Ground
B20	SBA4
B21	SBA6
B22	Key
B23	Key
B24	Key
B25	Key
B26	AD31
B27	AD29
B28	VCC 3.3
B29	AD27
B30	AD25
B31	Ground
B32	AD STB1
B33	AD23
B34	Vddq 3.3
B35	AD21
B36	AD19
B37	Ground
B38	AD17
B39	C/BE2#
B40	Vddq 3.3
B41	IRDY#
B42	Spare
B43	Ground
B44	Spare
B45	VCC 3.3
B46	DEVSEL#
B47	Vddq 3.3
B48	PERR#

B49	Ground
B50	SERR#
B51	C/BE1#
B52	Vddq 3.3
B53	AD14
B54	AD12
B55	Ground
B56	AD10
B57	AD8
B58	Vddq 3.3
B59	AD STB0
B60	AD7
B61	Ground
B62	AD5
B63	AD3
B64	Vddq 3.3
B65	AD1
B66	SMB0

Contributor: [Joakim Ögren](#)

Source:

[AGP pinout](#) at [The Pin-Out directory](#)

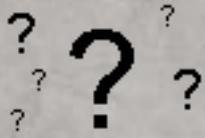
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# Amiga 1200 CPU-port



(at the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	n/c	Reserved
2	n/c	Reserved
3	n/c	Reserved
4	n/c	Reserved
5	n/c	Reserved
6	n/c	Reserved
7	n/c	Reserved
8	n/c	Reserved
9	GND	Ground
10	+5V	+5 Volts DC
11	A23	Address 23
12	A22	Address 22
13	A21	Address 21
14	A20	Address 20
15	A19	Address 19
16	A18	Address 18
17	A17	Address 17
18	A16	Address 16
19	GND	Ground
20	+5V	+5 Volts DC

21	A15	Address 15
22	A14	Address 14
23	A13	Address 13
24	A12	Address 12
25	A11	Address 11
26	A10	Address 10
27	A9	Address 9
28	A8	Address 8
29	GND	Ground
30	+5V	+5 Volts DC
31	A7	Address 7
32	A6	Address 6
33	A5	Address 5
34	A4	Address 4
35	A3	Address 3
36	A2	Address 2
37	A1	Address 1
38	A0	Address 0
39	GND	Ground
40	+5V	+5 Volts DC
41	D31	Data 31
42	D30	Data 30
43	D29	Data 29
44	D28	Data 28
45	D27	Data 27
46	D26	Data 26
47	D25	Data 25
48	D24	Data 24
49	GND	Ground
50	+5V	+5 Volts DC
51	D23	Data 23
52	D22	Data 22



53	D21	Data 21
54	D20	Data 20
55	D19	Data 19
56	D18	Data 18
57	D17	Data 17
58	D16	Data 16
59	GND	Ground
60	+5V	+5 Volts DC
61	D15	Data 15
62	D14	Data 14
63	D13	Data 13
64	D12	Data 12
65	D11	Data 11
66	D10	Data 10
67	D9	Data 9
68	D8	Data 8
69	GND	Ground
70	+5V	+5 Volts DC
71	D7	Data 7
72	D6	Data 6
73	D5	Data 5
74	D4	Data 4
75	D3	Data 3
76	D2	Data 2
77	D1	Data 1
78	D0	Data 0
79	GND	Ground
80	+5V	+5 Volts DC
81	/IPL2	
82	/IPL1	
83	/IPL0	
84	n/c	Reserved

85	/RST	Reset
86	/HLT	Halt
87	n/c	Reserved
88	n/c	Reserved
89	SIZE1	
90	SIZE0	
91	/AS	Address Strobe
92	/DS	Data Strobe
93	R/W	Read/Write
94	/BERR	Bus Error
95	n/c	Reserved
96	/AVEC	
97	/DSACK1	
98	/DSACK2	
99	CPUCKLA	
100	ECLOCK	EClock pulse
101	GND	Ground
102	+5V	+5 Volts DC
103	FC2	Processor Status 2
104	FC1	Processor Status 1
105	FC0	Processor Status 0
106	/RMC	
107	n/c	
108	n/c	
109	n/c	
110	n/c	
111	/BR	Slot specific Bus Arbitration
112	/BG	Slot specific Bus Arbitration
113	n/c	Reserved
114	/BOSS	
115	/FPUCS	
116	/FPUSENSE	

117	CCKA	
118	/RESET	Reset
119	GND	Ground
120	+5V	+5 Volts DC
121	/NETCS	
122	/SPARECS	
123	/RTCCS	Realtime Clock Chip select
124	/FLASH	
125	/REG	
126	/CCENA	
127	/WAIT	
128	/KBRESET	Keyboard reset
129	/IORD	IO Read
130	/IOWR	IO Write
131	/OE	Output enable
132	/WE	
133	/OVR	/DTACK Override
134	XRDY	External Ready
135	/ZORRO	
136	/WIDE	
137	/INT2	Interrupt level 2
138	/INT6	Interrupt level 6
139	GND	Ground
140	+5V	+5 Volts DC
141	SYSTEM1	System1 Ground
142	SYSTEM0	System0 Ground
143	/xRxD	
144	/xTxD	
145	/CONFIG OUT	
146	AGND	Audio Ground
147	ALEFT	Audio Left
148	ARIGHT	Audio Right

149	+12V	+12 Volts DC
150	-12V	-12 Volts DC

*Contributor:* [Joakim Ögren](#)

*Source:*

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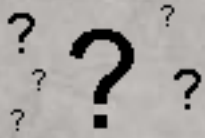
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# Amiga Video Expansion























(at the computer)

36+54 PIN EDGE CONNECTOR at the computer.

Pin	Name	Dir	Description
1	RGB16	→	Red Bit 0
2	RGB17	→	Red Bit 1
3	LINELF	→	Audio Line Out Left
4	LINERT	→	Audio Line Out Right
5	C28D	→	Pixel-Synchronous Clock
6	+5V	-	+5 Volts DC (1 A)
7	ARED	→	Analog Red
8	+5V	-	+5 Volts DC (1 A)
9	GND	-	Digital Ground
10	+12V	-	+12 Volts DC (40 mA)
11	AGREEN	→	Analog Green
12	GND	-	Digital Ground
13	GND	-	Digital Ground
14	/CSYNC	→	Composite Sync
15	ABLUE	→	Analog Blue
16	/XCLKEN	←	Genlock Clock Enable
17	GND	-	Digital Ground
18	BURST	→	Burst Gate
19	/C4	→	3.55/3.58 MHz Clock
20	GND	-	Digital Ground

21	GND	-	Digital Ground
22	/HSYNC		Horizontal Sync (47 Ohm)
23	RGB4		Blue Bit 4
24	GND	-	Digital Ground
25	RGB7		Blue Bit 7
26	/VSYNC		Vertical Sync (47 Ohm)
27	RGB15		Green Bit 7
28	BLANK		Video Blank
29	RGB23		Red 7
30	/PIXELSW		Genlock Overlay (47 Ohm)
31	-5V	-	-5 Volts DC
32	GND	-	Digital Ground
33	/XCLK		Genlock Clock
34	/C1		C1 Clock
35	+5V	-	+5 Volts DC (1 A)
36	PSTROBE		Printer Port Handshake
1	GND	-	Digital Ground
2	RGB20		Red Bit 4
3	RGB21		Red Bit 5
4	RGB22		Red Bit 6
5	GND	-	Digital Ground
6	RGB12		Green Bit 4
7	RGB13		Green Bit 5
8	RGB14		Green Bit 6
9	GND	-	Digital Ground
10	RGB5		Blue Bit 5
11	RGB6		Blue Bit 6
12	GND	-	Ground
13	SOG		Sync-On-Green Indicator
14	TBASE		50/60 Hz Software Clock Timebase
15	CDAC		7.09/7.16 MHz Clock

16	PPOUT		Printer Port Paper Out
17	/C3		3.55/3.58 MHz Clock
18	PBUSY		Printer Port Busy
19	/LPEN		Light Pen Input
20	/PACK		Printer Port Acknowledge Handshake
21	PSEL		Printer Port Select
22	GND	-	Digital Ground
23	PPD0		Printer Port Data Bit 0
24	PPD1		Printer Port Data Bit 1
25	PPD2		Printer Port Data Bit 2
26	PPD3		Printer Port Data Bit 3
27	PPD4		Printer Port Data Bit 4
28	PPD5		Printer Port Data Bit 5
29	PPD6		Printer Port Data Bit 6
30	PPD7		Printer Port Data Bit 7
31	/LED		LED (Audio filter bypass) Setting
32	GND	-	Digital Ground
33	RAWLF		Raw (Unfiltered) Audio Left
34	AGND	-	Audio Ground
35	RAWRT		Raw (Unfiltered) Audio Right
36	AGND	-	Audio Ground
37	n/c	-	Reserved for future expansion
38	n/c	-	Reserved for future expansion
39	GND	-	Digital Ground
40	GND	-	Digital Ground
41	n/c	-	Reserved for future expansion
42	n/c	-	Reserved for future expansion
43	GND	-	Digital Ground
44	GND	-	Digital Ground
45	RGB18		Red Bit 2
46	RGB19		Red Bit 3
47	RGB8		Green Bit 0

48	RGB9		Green Bit 1
49	RGB10		Green Bit 2
50	RGB11		Green Bit 3
51	RGB0		Blue Bit 0
52	RGB1		Blue Bit 1
53	RGB2		Blue Bit 2
54	RGB3		Blue Bit 3

*Note: Direction is Motherboard relative Card.*

*Note: Do not mix analog & digital grounds.*

*Contributor: [Joakim Ögren](#)*

*Source:*

*Amiga 4000 User's Guide from Commodore*

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# Apple Duo Dock

## 152 PIN UNKNOWN CONNECTOR

Available on Apple Duo Dock & Duo Dock II docking stations. For use with Apple PowerBook Duo computers.

Pin	Name	Description
1	PR +24V EXT	Raw +24 V from AC adapter
2	PR +24V EXT	Raw +24 V from AC adapter
3	/PLUG IN	Power surge control (grounded in the expansion device)
4	GND	Logic ground
7	/ON/OFF OUT	On/off button
9	/STERM	Synchronous termination
10	/DS	Data strobe
11	/AS	Address strobe
12	+5V MAIN OUT	+5 V regulated power
13	/HALT	Halt
14	/BERR	Bus error
15	/BGACK	Bus grant acknowledge
19	GND	Logic ground
20	GND	Logic ground
21	ADDR[0]	Address bit 0
22	ADDR[2]	Address bit 2
23	ADDR[4]	Address bit 4
24	ADDR[6]	Address bit 6
25	ADDR[8]	Address bit 8
26	ADDR[10]	Address bit 10
27	ADDR[12]	Address bit 12

28	ADDR[14]	Address bit 14
29	+5V MAIN OUT	+5 V regulated power
30	GND	Logic ground
31	ADDR[18]	Address bit 18
32	ADDR[20]	Address bit 20
33	ADDR[22]	Address bit 22
34	ADDR[24]	Address bit 24
35	ADDR[26]	Address bit 26
36	ADDR[28]	Address bit 28
37	ADDR[30]	Address bit 30
38	GND	Logic ground
39	GND	Logic ground
40	IOCLK	15.6672 MHz I/O clock
41	SIZ[1]	Transfer size bit 1
42	+5V MAIN OUT	+5 V regulated power
43	DATA[0]	Data bit 0
44	DATA[1]	Data bit 1
45	DATA[2]	Data bit 2
46	DATA[3]	Data bit 3
47	DATA[4]	Data bit 4
48	DATA[5]	Data bit 5
49	DATA[6]	Data bit 6
50	DATA[7]	Data bit 7
51	GND	Logic ground
52	DATA[17]	Data bit 17
53	DATA[18]	Data bit 18
54	DATA[19]	Data bit 19
56	DATA[20]	Data bit 20
57	DATA[21]	Data bit 21
58	DATA[22]	Data bit 22
59	DATA[23]	Data bit 23
61	GND	Logic ground

62	/SCC IRQ	SCC interrupt request
63	SERVEE	-5 V for SCC transceivers
65	GND	Logic ground
66	GND	Logic ground
67	+8V SOUND	Special "clean" +8 V power for sound output
68	+5V MODEM	+5 V power for modem
69	LINET/R	Modem DAA line talk/receive
70	+5V SOUND	+5 V power for sound output
72	SND OUT L	Sound output left channel
73	EXT MIC FILT R	Right input signal from external microphone
74	EXT MIC FILT L	Left input signal from external microphone
75	DAA GND	Modem ground
76	DAA GND	Modem ground
77	PR +24V EXT	Raw +24 V from AC adapter
78	PR +24V EXT	Raw +24 V from AC adapter
79	PR +24V EXT	Raw +24 V from AC adapter
80	GND	Logic ground
81	GND	Logic ground
83	ADB DATA	Apple Desktop Bus data
84	/ADBPWRON	ADB power-on key
86	/CBREQ	Cache burst request
87	/DSACK1	Data size acknowledge bit 1
88	/DSACK0	Data size acknowledge bit 0
89	/BR	Bus request
90	/BG	Bus grant
91	/SLEEP	Sleep-state signal
92	FC[1]	Function code bit 1
93	FC[0]	Function code bit 0
94	/RMC	Read-modify-write cycle
95	CPUCLK	CPU bus clock
96	/CPURESET	CPU reset (bus invalid)
97	ADDR[1]	Address bit 1



98	ADDR[3]	Address bit 3
99	ADDR[5]	Address bit 5
100	ADDR[7]	Address bit 7
101	ADDR[9]	Address bit 9
102	ADDR[11]	Address bit 11
103	ADDR[13]	Address bit 13
104	ADDR[15]	Address bit 15
105	ADDR[16]	Address bit 16
106	ADDR[17]	Address bit 17
107	ADDR[19]	Address bit 19
108	ADDR[21]	Address bit 21
109	ADDR[23]	Address bit 23
110	ADDR[25]	Address bit 25
111	ADDR[27]	Address bit 27
112	ADDR[29]	Address bit 29
113	ADDR[31]	Address bit 31
114	/SLOT IN	Expansion device plugged in grounds pin
115	GND	Logic ground
116	RD	Read/Write
117	SIZ[0]	Transfer size bit 0
118	DATA[8]	Data bit 8
119	DATA[9]	Data bit 9
120	DATA[10]	Data bit 10
121	DATA[11]	Data bit 11
122	+5VEXTSENSE	+5 V external sense
123	DATA[12]	Data bit 12
124	DATA[13]	Data bit 13
125	DATA[14]	Data bit 14
126	DATA[15]	Data bit 15
127	DATA[16]	Data bit 16
128	DATA[24]	Data bit 24
129	DATA[25]	Data bit 25



130	DATA[26]	Data bit 26
131	DATA[27]	Data bit 27
132	DATA[28]	Data bit 28
133	DATA[29]	Data bit 29
134	DATA[30]	Data bit 30
135	DATA[31]	Data bit 31
137	/SWIM CS	SWIM chip select
138	/SLOT E IRQ	Pseudo-NuBus expansion slot E interrupt
139	/PFW	Power fail warning (shutdown bit)
140	/IO RESET	Reset output to I/O systems
141	GND	Logic ground
142	GND	Logic ground
143	DAA CNTLF	Modem DAA control
144	DAA ID IN	ID input from 152-pin connector to modem card
145	/RING DET	Ring detect signal from the modem DAA
146	/RB DVR	Modem relay B driver
147	/RA DVR	Modem relay A driver
148	EXT MIC SEL	External microphone plugged in
151	DAA GND	Modem ground
152	DAA GND	Modem ground

*Note: / = Active low*

Connector: JAE part number JX20-152BA-D1LTH

Provides the interface between the PowerBook Duo computer, and the Duo Dock. It mounts directly to the Duo Dock's main logic board, and plugs into the matching connector on the PowerBook Duo rear panel, giving the Duo Dock direct access to the microprocessor's 32-bit address bus, 32-bit data bus, and control signals. It also provides access to power, control, and status signals in other parts of the computer, and allows the Duo Dock to provide power to the PowerBook Duo.

Contributor: [Joakim Ögren](#)

Source: [Apple Tech Info Library 12929: Duo Dock/Duo Dock II, External Pinouts](#) at [Apple TIL homepage](#)

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*Document last modified: 2001-06-07*



# Apple Macintosh Portable Processor-Direct Slot (PPDS)

96 PIN Euro-DIN CONNECTOR

Pin	Name
a1	GND
a2	+5V
a3	+5V
a4	+5V
a5	/DELAY.CS
a6	/VMA
a7	/BG
a8	/LDS
a9	GND
a10	A2
a11	A5
a12	A8
a13	A11
a14	A14
a15	A17
a16	reserved
a17	n/c
a18	reserved
a19	reserved
a20	D1
a21	D4
a22	D7

a23	D10
a24	D13
a25	+5/3.7V
a26	A19
a27	A22
a28	FC0
a29	/IPL0
a30	/BERR
a31	GND
a32	GND
b1	GND
b2	+5V
b3	+5V
b4	+5V
b5	/SYS.PWR
b6	/BR
b7	/DTACK
b8	/UDS
b9	+5/0V
b10	A3
b11	A6
b12	A9
b13	A12
b14	A15
b15	A18
b16	reserved
b17	reserved
b18	reserved
b19	+12V
b20	D2
b21	D5
b22	D8



b23	D11
b24	D14
b25	+5V
b26	A20
b27	A23
b28	FC1
b29	/IPL1
b30	/EXT.DTACK
b31	16M
b32	GND
c1	GND
c2	+5V
c3	+5V
c4	+5V
c5	/VPA
c6	/BGACK
c7	R/W
c8	/AS
c9	A1
c10	A4
c11	A7
c12	A10
c13	A13
c14	A16
c15	reserved
c16	n/c
c17	reserved
c18	reserved
c19	D0
c20	D3
c21	D6
c22	D9

c23	D12
c24	D15
c25	GND
c26	A21
c27	E
c28	FC2
c29	/IPL2
c30	/SYS.RST
c31	GND
c32	GND

## D0-D15

Unbuffered data bus, bits 0 through 15

## A1-A23

Unbuffered address bus, bits 1 through 23

## 16M

16 MHz clock

## /EXT.DTACK

External data transfer acknowledge. This signal is an input to the processor logic glue. Assertion delays external generation of the /DTACK signal.

## E

E(enable) clock

## /BERR

Bus error signal generated whenever /AS remains low for more than about 250 us.

## **/IPL0-/IPL2**

Input priority level lines 0 through 2.

## **/SYS.RST**

Initiates a system reset.

## **/SYS.PWR**

A signal from the Power Manager indicated that associated circuits should tri-state their outputs and go into idle state; /SYS.PWR is pulled high (deasserted) during sleep state.

## **/AS**

Address strobe

## **/UDS**

Upper data strobe

## **/LDS**

Lower data strobe

## **R/W**

Defines bus transfer as read or write signal

## **/DTACK**

Data transfer acknowledge

## **/DELAY.CS**

Indicates that a wait state is inserted into the current memory cycle and that you can delay a CS.

## **/BG**

Bus grant

## **/BGACK**

Bus grant acknowledge

## **/BR**

Bus request

## **/VMA**

Valid memory access

## **/VPA**

Valid peripheral address

## **FC0-FC2**

Function code lines 0 through 2

## **+5/0V**

Provides +5V when the system is running normally and 0V when the system is in sleep mode.

## **+5/3.7V**



Provides +5V when the system is running normally and 3.7V when the system is in sleep mode.

Contributor: [Joakim Ögren](#)

Source:

[Technote HW12: Macintosh Portable PDS Development](#) at [Apple Technical Notes](#)

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*Document last modified: 2000-07-07*



# Apple Macintosh Processor-Direct Slot (PDS)

## 120 PIN Euro-DIN CONNECTOR

Available on Apple Macintosh SE/30 & IIfx

Cards in the PDS are accessed at 20MHz. This speed should let developers create PDS cards without using expensive components while still providing access to the processor bus. There are two locations in the memory map for PDS cards. Developers should see the "Cards and Drivers Manual" for information on creating PDS cards. This manual is available from APDA.

The cache connector in the Macintosh IIfx may look like the Macintosh IIfx PDS connector, but the pinouts are vastly different.

Pin	Name	Description
A1	res	Reserved
A2	res	Reserved
A3	/BUSLOCK	Bus Clock
A4	/IRQ3	Interrupt Request 3
A5	/IPL2*	68030 IPL2
A6	/CIOUT*	68030 Cache inhibit out
A7	/STERM*	Sync.cycle termination
A8	/DSACK1*	68030 Data ack 1
A9	SIZ1	transfer size bit 1
A10	/BGACK*	68030 bus grant ack
A11	FC2	68030 function code 2
A12	/RESET*	System reset
A13	D0	Data bit 0
A14	D2	Data bit 2

A15	D5	Data bit 5
A16	D8	Data bit 8
A17	D10	Data bit 10
A18	D13	Data bit 13
A19	D16	Data bit 16
A20	D18	Data bit 18
A21	D21	Data bit 21
A22	D24	Data bit 24
A23	D26	Data bit 26
A24	D29	Data bit 29
A25	A31	address bit 31
A26	A29	address bit 29
A27	A26	address bit 26
A28	A23	address bit 23
A29	A21	address bit 21
A30	A18	address bit 18
A31	A15	address bit 15
A32	A13	address bit 13
A33	A10	address bit 10
A34	A7	address bit 7
A35	A5	address bit 5
A36	A2	address bit 2
A37	+5V	+5 VDC
A38	CPUCLOCK	CPU Clock
A39	GND	Ground
A40	-12V	-12 VDC
B1	res	Reserved
B2	GND	Ground
B3	/TM1A	?
B4	/IRQ2	Interrupt Request 2
B5	/IPL1*	68030 IPL1
B6	/DS*	68030 Data Strobe

B7	/CBACK*	cache burst ack
B8	/DSACK0*	68030 Data ack 0
B9	SIZ0	Transfer Size bit 0
B10	/BG*	68030 bus grant
B11	FC1	68030 function code 1
B12	/BERR*	Bus error
B13	+5V	+5 VDC
B14	D3	Data bit 3
B15	D6	Data bit 6
B16	GND	Ground
B17	D11	Data bit 11
B18	D14	Data bit 14
B19	+5V	+5 VDC
B20	D19	Data bit 19
B21	D22	Data bit 22
B22	GND	Ground
B23	D27	Data bit 27
B24	D30	Data bit 30
B25	+5V	+5 VDC
B26	A28	address bit 28
B27	A25	address bit 25
B28	GND	Ground
B29	A20	address bit 20
B30	A17	address bit 17
B31	+5V	+5 VDC
B32	A12	address bit 12
B33	A9	address bit 9
B34	GND	Ground
B35	A4	address bit 4
B36	A1	address bit 1
B37	+5V	+5 VDC
B38	ECLK	?



B39	GND	Ground
B40	-5V	-5 VDC
C1	PWROFF	Power Off?
C2	/NUBUS	?
C3	/TM0A	?
C4	/IRQ1	Interrupt Request 1
C5	/IPL0*	68030 IPL0
C6	/RMC*	68030 read modify cycle
C7	/CBREQ*	68030 cache burst req
C8	R/W*	68030 read write
C9	/AS*	68030 address strobe
C10	/BR*	68030 bus request
C11	FC0	68030 function code 0
C12	/HALT*	68030 Halt
C13	D1	Data bit 1
C14	D4	Data bit 4
C15	D7	Data bit 7
C16	D9	Data bit 9
C17	D12	Data bit 12
C18	D15	Data bit 15
C19	D17	Data bit 17
C20	D20	Data bit 20
C21	D23	Data bit 23
C22	D25	Data bit 25
C23	D28	Data bit 28
C24	D31	Data bit 31
C25	A30	address bit 30
C26	A27	address bit 27
C27	A24	address bit 24
C28	A22	address bit 22
C29	A19	address bit 19
C30	A16	address bit 16

C31	A14	address bit 14
C32	A11	address bit 11
C33	A8	address bit 8
C34	A6	address bit 6
C35	A3	address bit 3
C36	A0	address bit 0
C37	+5V	+5 VDC
C38	C16M	16 MHz Clock
C39	GND	Ground
C40	+12V	+12 VDC

Below a table with differences found in the Apple Macintosh IIfx computers:

Pin	Name	Description
A1	GND*	Ground
A2	/PDS.MASTER	?
A3	res	Reserved
A4	n.c.	Not connected
A38	Reserved	by Apple
B1	ECS	Early cycle start
B2	n.c.	Not connected
B3	/PDS.BG	?
B4	/IRQ15	?
B38	n.c.	Not connected
B39	/SLOT.E	68030 slot E replace in address map
C1	/PFW	Shutdown bit
C2	n.c.	Not connected
C3	/PDS.BR	Bus request
C4	/IRQ6	?
C38	CPUCLK*	20 MHz clock

Contributor: [Joakim Ögren](#)

*Source:*

*[Apple Tech Info Library 5744: Macintosh SE/30,IIx: Processor-Direct Slot \(PDS\) Pinouts](#) at [Apple TIL homepage](#)*

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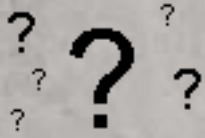
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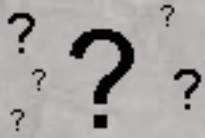
# C-bus II

Developed by Corolla

C-bus II is the successor to C-bus & Extended C-bus.



(at the backplane)



(at the device (card))

UNKNOWN CONNECTOR at the backplane.

UNKNOWN CONNECTOR at the device (card).

PA=Component side

PB=Solder side

Pin	Name
PA1	GND
PA2	AUX18
PA3	AUX16
PA4	GND
PA5	AUX14
PA6	AUX12
PA7	GND
PA8	AUX10
PA9	AUX8
PA10	GND
PA11	AUX6



PA12	AUX4
PA13	GND
PA14	AUX2
PA15	AUX0
PA16	GND
PA17	RESERVED8
PA18	RESERVED6
PA19	RESERVED4
PA20	RESERVED2
PA21	RESERVED0
PA22	GND
PA23	GND
PA24	AGND
PA25	CID1
PA26	CBCLK
PA27	GND
PA28	CRST#
PA29	LED#
PA30	GND
PA31	CARB2
PA32	CARB0
PA33	GND
PA34	TM2#
PA35	TM0#
PA36	GND
PA37	STRT#
PA38	CD31
PA39	GND
PA40	CD30
PA41	CD29
PA42	GND
PA43	CD28

PA44	CD27
PA45	GND
PA46	CD26
PA47	CD25
PA48	GND
PA49	CD24
PA50	CD23
PA51	GND
PA52	CD22
PA53	CD21
PA54	GND
PA55	CD20
PA56	CD19
PA57	GND
PA58	CD18
PA59	CD17
PA60	GND
PA61	CD16
PA62	E3
PA63	GND
PA64	E2
PA65	CD15
PA66	GND
PA67	CD14
PA68	CD13
PA69	GND
PA70	CD12
PA71	CD11
PA72	GND
PA73	CD10
PA74	CD9
PA75	GND

PA76	CD8
PA77	CD7
PA78	GND
PA79	CD6
PA80	CD5
PA81	GND
PA82	CD4
PA83	CD3
PA84	GND
PA85	CD2
PA86	CD1
PA87	GND
PA88	CD0
PA89	E1
PA90	GND
PA91	E0
PB1	+5V
PB2	AUX19
PB3	AUX17
PB4	+5V
PB5	AUX15
PB6	AUX13
PB7	+5V
PB8	AUX11
PB9	AUX9
PB10	+5V
PB11	AUX7
PB12	AUX5
PB13	+5V
PB14	AUX3
PB15	AUX1

PB16	+5V
PB17	RESERVED9
PB18	RESERVED7
PB19	RESERVED5
PB20	RESERVED3
PB21	RESERVED1
PB22	VTERM
PB23	+5V
PB24	CID3
PB25	CID2
PB26	CID0
PB27	+5V
PB28	FAULT#
PB29	LOCKCB#
PB30	+5V
PB31	CARB3
PB32	CARB1
PB33	+5V
PB34	TM3#
PB35	TM1#
PB36	+5V
PB37	ACK#
PB38	CD63
PB39	+5V
PB40	CD62
PB41	CD61
PB42	+5V
PB43	CD60
PB44	CD59
PB45	+5V
PB46	CD58
PB47	CD57



PB48	+5V
PB49	CD56
PB50	CD55
PB51	+3.3V
PB52	CD54
PB53	CD53
PB54	+3.3V
PB55	CD52
PB56	CD51
PB57	+3.3V
PB58	CD50
PB59	CD49
PB60	+3.3V
PB61	CD48
PB62	E7
PB63	+3.3V
PB64	E6
PB65	CD47
PB66	+3.3V
PB67	CD46
PB68	CD45
PB69	+3.3V
PB70	CD44
PB71	CD43
PB72	+3.3V
PB73	CD42
PB74	CD41
PB75	+3.3V
PB76	CD40
PB77	CD39
PB78	+3.3V
PB79	CD38

PB80	CD37
PB81	+3.3V
PB82	CD36
PB83	CD35
PB84	+3.3V
PB85	CD34
PB86	CD33
PB87	+3.3V
PB88	CD32
PB89	E5
PB90	+3.3V
PB91	E4

*Contributor:* [Joakim Ögren](#)

*Source:*

*C-bus II Technology architecture at Corollary's homepage*

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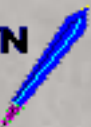
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# CardBus

32-bit bus defined by PCMCIA.

**NOT  
DRAWN  
YET...** 

(at the controller)

**NOT  
DRAWN  
YET...** 

(at the peripherals)

68 PIN ??? MALE at the controller.

68 PIN ??? FEMALE at the peripherals.

Pin	Name	Description
1	GND	Ground
2	CAD0	Address/Data 0
3	CAD1	Address/Data 1
4	CAD3	Address/Data 3
5	CAD5	Address/Data 5
6	CAD7	Address/Data 7
7	CCBE0#	Command/Byte Enable 0
8	CAD9	Address/Data 9
9	CAD11	Address/Data 11
10	CAD12	Address/Data 12
11	CAD14	Address/Data 14
12	CCBE1#	Command/Byte Enable 1
13	CPAR	Parity
14	CPERR#	Parity error

15	CGNT#	Grant
16	CINT#	Interrupt
17	Vcc	Vcc
18	Vpp1	Vpp1
19	CCLK	CCLK
20	CIRDY#	Initiator Ready
21	CCBE2#	Command/Byte Enable 2
22	CAD18	Address/Data 18
23	CAD20	Address/Data 20
24	CAD21	Address/Data 21
25	CAD22	Address/Data 22
26	CAD23	Address/Data 23
27	CAD24	Address/Data 24
28	CAD25	Address/Data 25
29	CAD26	Address/Data 26
30	CAD27	Address/Data 27
31	CAD29	Address/Data 29
32	RSRVD	Reserved
33	CCLKRUN#	CCLKRUN#
34	GND	Ground
35	GND	Ground
36	CCD1#	Card Detect 1
37	CAD2	Address/Data 2
38	CAD4	Address/Data 4
39	CAD6	Address/Data 6
40	RSRVD	Reserved
41	CAD8	Address/Data 8
42	CAD10	Address/Data 10
43	CVS1	
44	CAD13	Address/Data 13
45	CAD15	Address/Data 15
46	CAD16	Address/Data 16



47	RSRVD	Reserved
48	CBLOCK#	Block ???
49	CSTOP#	Stop transfer cycle
50	CDEVSEL#	Device Select
51	Vcc	Vcc
52	Vpp2	Vpp2
53	CTRDY#	Target Ready
54	CFRAME#	Address or Data phase
55	CAD17	Address/Data 17
56	CAD19	CAD19
57	CVS2	
58	CRST#	Reset
59	CSERR#	System Error
60	CREQ#	Request ???
61	CCBE3#	Command/Byte Enable 3
62	CAUDIO	Audio ???
63	CSTSCHG	
64	CAD28	Address/Data 28
65	CAD30	Address/Data 30
66	CAD31	Address/Data 31
67	CCD2#	Card Detect 2
68	GND	Ground

Contributor: [Joakim Ögren](#), [Marek Hostasa](#)

Source:  
PC Card Standard at PC Card's homepage

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# CompactPCI

PCI=Peripheral Component Interconnect.

CompactPCI is a version of PCI adapted for industrial and/or embedded applications.

**NOT  
DRAWN  
YET...**



(at the backplane)

**NOT  
DRAWN  
YET...**



(at the device (card))

7x47 PIN (IEC917 and IEC1076-4-101) CONNECTOR at the backplane.

7x47 PIN (IEC917 and IEC1076-4-101) CONNECTOR at the device (card).

Pin	Name	Description
Z1	GND	Ground
Z2	GND	Ground
Z3	GND	Ground
Z4	GND	Ground
Z5	GND	Ground
Z6	GND	Ground
Z7	GND	Ground
Z8	GND	Ground
Z9	GND	Ground
Z10	GND	Ground
Z11	GND	Ground
Z12	KEY	Keyed (no pin)
Z13	KEY	Keyed (no pin)
Z14	KEY	Keyed (no pin)

Z15	GND	Ground
Z16	GND	Ground
Z17	GND	Ground
Z18	GND	Ground
Z19	GND	Ground
Z20	GND	Ground
Z21	GND	Ground
Z22	GND	Ground
Z23	GND	Ground
Z24	GND	Ground
Z25	GND	Ground
Z26	GND	Ground
Z27	GND	Ground
Z28	GND	Ground
Z29	GND	Ground
Z30	GND	Ground
Z31	GND	Ground
Z32	GND	Ground
Z33	GND	Ground
Z34	GND	Ground
Z35	GND	Ground
Z36	GND	Ground
Z37	GND	Ground
Z38	GND	Ground
Z39	GND	Ground
Z40	GND	Ground
Z41	GND	Ground
Z42	GND	Ground
Z43	GND	Ground
Z44	GND	Ground
Z45	GND	Ground
Z46	GND	Ground

Z47	GND	Ground
A1	5V	+5 VDC
A2	TCK	Test Clock
A3	INTA#	Interrupt A
A4	BRSV	Bused Reserved (don't use)
A5	BRSV	Bused Reserved (don't use)
A6	REQ#	Request PCI transfer
A7	AD(30)	Address/Data 30
A8	AD(26)	Address/Data 26
A9	C/BE(3)#	Command: Byte Enable
A10	AD(21)	Address/Data 21
A11	AD(18)	Address/Data 18
A12	KEY	Keyed (no pin)
A13	KEY	Keyed (no pin)
A14	KEY	Keyed (no pin)
A15	3.3V	+3.3 VDC
A16	DEVSEL#	Device Select
A17	3.3V	+3.3 VDC
A18	SERR#	System Error
A19	3.3V	+3.3 VDC
A20	AD(12)	Address/Data 12
A21	3.3V	+3.3 VDC
A22	AD(7)	Address/Data 7)
A23	3.3V	+3.3 VDC
A24	AD(1)	Address/Data 1)
A25	5V	+5 VDC
A26	CLK1	Clock ?? MHz
A27	CLK2	Clock ?? MHz
A28	CLK4	Clock ?? MHz
A29	V(I/O)	+3.3 VDC or +5 VDC
A30	C/BE(5)#	Command: Byte Enable



A31	AD(63)	Address/Data 63
A32	AD(59)	Address/Data 59
A33	AD(56)	Address/Data 56
A34	AD(52)	Address/Data 52
A35	AD(49)	Address/Data 49
A36	AD(45)	Address/Data 45
A37	AD(42)	Address/Data 42
A38	AD(38)	Address/Data 38
A39	AD(35)	Address/Data 35
A40	BRSV	Bused Reserved (don't use)
A41	BRSV	Bused Reserved (don't use)
A42	BRSV	Bused Reserved (don't use)
A43	USR	User Defined
A44	USR	User Defined
A45	USR	User Defined
A46	USR	User Defined
A47	USR	User Defined
B1	-12V	-12 VDC
B2	5V	+5 VDC
B3	INTB#	Interrupt B
B4	GND	Ground
B5	BRSV	Bused Reserved (don't use)
B6	GND	Ground
B7	AD(29)	Address/Data 29
B8	GND	Ground
B9	IDSEL	Initialization Device Select
B10	GND	Ground
B11	AD(17)	Address/Data 17
B12	KEY	Keyed (no pin)
B13	KEY	Keyed (no pin)
B14	KEY	Keyed (no pin)

B15	FRAME#	Address or Data phase
B16	GND	Ground
B17	SDONE	Snoop Done
B18	GND	Ground
B19	AD(15)	Address/Data 15
B20	GND	Ground
B21	AD(9)	Address/Data 9)
B22	GND	Ground
B23	AD(4)	Address/Data 4)
B24	5V	+5 VDC
B25	REQ64#	
B26	GND	Ground
B27	CLK3	Clock ?? MHz
B28	GND	Ground
B29	BRSV	Bused Reserved (don't use)
B30	GND	Ground
B31	AD(62)	Address/Data 62
B32	GND	Ground
B33	AD(55)	Address/Data 55
B34	GND	Ground
B35	AD(48)	Address/Data 48
B36	GND	Ground
B37	AD(41)	Address/Data 41
B38	GND	Ground
B39	AD(34)	Address/Data 34
B40	GND	Ground
B41	BRSV	Bused Reserved (don't use)
B42	GND	Ground
B43	USR	User Defined
B44	USR	User Defined
B45	USR	User Defined
B46	USR	User Defined

B47	USR	User Defined
C1	TRST#	Test Logic Reset
C2	TMS	Test Mode Select
C3	INTC#	Interrupt C
C4	V(I/O)	+3.3 VDC or +5 VDC
C5	RST	Reset
C6	3.3V	+3.3 VDC
C7	AD(28)	Address/Data 28
C8	V(I/O)	+3.3 VDC or +5 VDC
C9	AD(23)	Address/Data 23
C10	3.3V	+3.3 VDC
C11	AD(16)	Address/Data 16
C12	KEY	Keyed (no pin)
C13	KEY	Keyed (no pin)
C14	KEY	Keyed (no pin)
C15	IRDY#	Initiator Ready
C16	V(I/O)	+3.3 VDC or +5 VDC
C17	SBO#	Snoop Backoff
C18	3.3V	+3.3 VDC
C19	AD(14)	Address/Data 14
C20	V(I/O)	+3.3 VDC or +5 VDC
C21	AD(8)	Address/Data 8)
C22	3.3V	+3.3 VDC
C23	AD(3)	Address/Data 3)
C24	V(I/O)	+3.3 VDC or +5 VDC
C25	BRSV	Bused Reserved (don't use)
C26	REQ1#	Request PCI transfer
C27	SYSEN#	
C28	GNT3#	Grant
C29	C/BE(7)	Command: Byte Enable
C30	V(I/O)	+3.3 VDC or +5 VDC

C31	AD(61)	Address/Data 61
C32	V(I/O)	+3.3 VDC or +5 VDC
C33	AD(54)	Address/Data 54
C34	V(I/O)	+3.3 VDC or +5 VDC
C35	AD(47)	Address/Data 47
C36	V(I/O)	+3.3 VDC or +5 VDC
C37	AD(40)	Address/Data 40
C38	V(I/O)	+3.3 VDC or +5 VDC
C39	AD(33)	Address/Data 33
C40	FAL#	Power Supply Status FAL (CompactPCI specific)
C41	DEG#	Power Supply Status DEG (CompactPCI specific)
C42	PRST#	Push Button Reset (CompactPCI specific)
C43	USR	User Defined
C44	USR	User Defined
C45	USR	User Defined
C46	USR	User Defined
C47	USR	User Defined
D1	+12V	+12 VDC
D2	TDO	Test Data Output
D3	5V	+5 VDC
D4	INTP	
D5	GND	Ground
D6	CLK	
D7	GND	Ground
D8	AD(25)	Address/Data 25
D9	GND	Ground
D10	AD(20)	Address/Data 20
D11	GND	Ground
D12	KEY	Keyed (no pin)
D13	KEY	Keyed (no pin)
D14	KEY	Keyed (no pin)



D15	GND	Ground
D16	STOP#	Stop transfer cycle
D17	GND	Ground
D18	PAR	Parity for AD0-31 & C/BE0-3
D19	GND	Ground
D20	AD(11)	Address/Data 11
D21	M66EN	
D22	AD(6)	Address/Data 6)
D23	5V	+5 VDC
D24	AD(0)	Address/Data 0)
D25	3.3V	+3.3 VDC
D26	GNT1#	Grant
D27	GNT2#	Grant
D28	REQ4#	Request PCI transfer
D29	GND	Ground
D30	C/BE(4)#	Command: Byte Enable
D31	GND	Ground
D32	AD(58)	Address/Data 58
D33	GND	Ground
D34	AD(51)	Address/Data 51
D35	GND	Ground
D36	AD(44)	Address/Data 44
D37	GND	Ground
D38	AD(37)	Address/Data 37
D39	GND	Ground
D40	REQ5#	Request PCI transfer
D41	GND	Ground
D42	REQ6#	Request PCI transfer
D43	USR	User Defined
D44	USR	User Defined
D45	USR	User Defined
D46	USR	User Defined

D47	USR	User Defined
E1	5V	+5 VDC
E2	TDI	Test Data Input
E3	INTD#	Interrupt D
E4	INTS	
E5	GNT#	Grant
E6	AD(31)	Address/Data 31
E7	AD(27)	Address/Data 27
E8	AD(24)	Address/Data 24
E9	AD(22)	Address/Data 22
E10	AD(19)	Address/Data 19
E11	C/BE(2)#	Command: Byte Enable
E12	KEY	Keyed (no pin)
E13	KEY	Keyed (no pin)
E14	KEY	Keyed (no pin)
E15	TRDY#	Target Ready
E16	LOCK#	Lock resource
E17	PERR#	Parity Error
E18	C/BE(1)#	Command: Byte Enable
E19	AD(13)	Address/Data 13
E20	AD(10)	Address/Data 10
E21	C/BE(0)#	Command: Byte Enable
E22	AD(5)	Address/Data 5)
E23	AD(2)	Address/Data 2)
E24	ACK64#	
E25	5V	+5 VDC
E26	REQ2#	Request PCI transfer
E27	REQ3#	Request PCI transfer
E28	GNT4#	Grant
E29	C/BE(6)#	Command: Byte Enable
E30	PAR64	

E31	AD(60)	Address/Data 60
E32	AD(57)	Address/Data 57
E33	AD(53)	Address/Data 53
E34	AD(50)	Address/Data 50
E35	AD(46)	Address/Data 46
E36	AD(43)	Address/Data 43
E37	AD(39)	Address/Data 39
E38	AD(36)	Address/Data 36
E39	AD(32)	Address/Data 32
E40	GNT5#	Grant
E41	BRSV	Bused Reserved (don't use)
E42	GNT6#	Grant
E43	USR	User Defined
E44	USR	User Defined
E45	USR	User Defined
E46	USR	User Defined
E47	USR	User Defined
F1	GND	Ground
F2	GND	Ground
F3	GND	Ground
F4	GND	Ground
F5	GND	Ground
F6	GND	Ground
F7	GND	Ground
F8	GND	Ground
F9	GND	Ground
F10	GND	Ground
F11	GND	Ground
F12	KEY	Keyed (no pin)
F13	KEY	Keyed (no pin)
F14	KEY	Keyed (no pin)

F15	GND	Ground
F16	GND	Ground
F17	GND	Ground
F18	GND	Ground
F19	GND	Ground
F20	GND	Ground
F21	GND	Ground
F22	GND	Ground
F23	GND	Ground
F24	GND	Ground
F25	GND	Ground
F26	GND	Ground
F27	GND	Ground
F28	GND	Ground
F29	GND	Ground
F30	GND	Ground
F31	GND	Ground
F32	GND	Ground
F33	GND	Ground
F34	GND	Ground
F35	GND	Ground
F36	GND	Ground
F37	GND	Ground
F38	GND	Ground
F39	GND	Ground
F40	GND	Ground
F41	GND	Ground
F42	GND	Ground
F43	GND	Ground
F44	GND	Ground
F45	GND	Ground
F46	GND	Ground



F47	GND	Ground
-----	-----	--------

Contributor: [Joakim Ögren](#)

Sources:

[CompactPCI specifications v1.0](#) at [CompactPCI's homepage](#)

[Mark Sokos PCI page](#)

*"Inside the PCI Local Bus" by Guy W. Kendall, Byte, February 1994 v 19 p. 177-180*

*"The Indispensible PC Hardware Book" by Hans-Peter Messmer, ISBN 0-201-8769-3*

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# CompactPCI (technical)

This section does not currently contain so much in depth information as I would like.

Since CompactPCI is based on PCI you should first refer to the PCI standard. This only explains the extensions CompactPCI specifies.

For a copy of the full CompactPCI standard, contact:

PCI Industrial Computer Manufacturers Group (PICMG)  
c/o Roger Communications  
301 Edgewater place  
Suite 220  
Wakewater  
MA01880  
Phone: 1-617-224-1100  
Fax: 1-617-224-1239

## Overview:

A CompactPCI system is composed of up to eight CompactPCI card locations:

- One System Slot
- Up to seven Peripheral Slots

The connector has 7 columns with 47 rows. They are divided into groups:

- Row 1-25: 32-bit PCI
- Row 26-47: Additional pins for 64-bit PCI (System Slot boards must use it).
- Row 26-28 and 40-42: Primarily implemented on System Slot boards.

The following signals must be terminated:

- AD0-31
- C/BE0#-C/BE3#
- PAR

- FRAME#
- IRDY#
- TRDY#
- STOP#
- LOCK#
- IDSEL
- DEVSEL#
- PERR#
- SERR#
- RST#

The following signals must be terminated if used:

- INTA#
- INTB#
- INTC#
- INTD#
- SB0#
- SDOBE
- AD32-AD63
- C/BE4#-C/BE7#
- REQ64#
- ACK64#
- PAR64#

The following signals do not require a stub termination:

- CLK
- REQ#
- GNT#
- TDI#
- TDO
- TCK
- TMS
- TRST#

The System Slot board must pullup the following signals (even if not used):

- REQ64#
- ACK64#

## Connector:

1	GND	5V	-12V	TRST#	12V	5V	GND
2	GND	TCK	5V	TMS	DO	TDI	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
4	GND	BRSV	GND	V(I/O)	INTP	INTS	GND
5	GND	BRSV	BRSV	RST	GND	GNT#	GND
6	GND	REQ#	GND	3.3V	CLK	AD(31)	GND
7	GND	AD(30)	AD(29)	AD(28)	GND	AD(27)	GND
8	GND	AD(26)	GND	V(I/O)	AD(25)	AD(24)	GND
9	GND	C/BE(3)#	IDSEL	AD(23)	GND	AD(22)	GND
10	GND	AD(21)	GND	3.3V	AD(20)	AD(19)	GND
11	GND	AD(18)	AS(17)	AD(16)	GND	C/BE(2)#	GND
12	KEY	KEY	KEY	KEY	KEY	KEY	KEY
13	KEY	KEY	KEY	KEY	KEY	KEY	KEY
14	KEY	KEY	KEY	KEY	KEY	KEY	KEY
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE(1)#	GND
19	GND	3.3V	AD(15)	AD(14)	GND	AD(13)	GND
20	GND	AD(12)	GND	V(I/O)	AD(11)	AD(10)	GND
21	GND	3.3V	AD(9)	AD(8)	M66EN	C/BE(0)#	GND
22	GND	AD(7)	GND	3.3V	AD(6)	AD(5)	GND
23	GND	3.3V	AD(4)	AD(3)	5V	AD(2)	GND
24	GND	AD(1)	5V	V(I/O)	AD(0)	ACK64#	GND
25	GND	5V	REQ64#	BRSV	3.3V	5V	GND
26	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
27	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
28	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
29	GND	V(I/O)	BRSV	C/BE(7 )	GND	C/BE(6)#	GND
30	GND	C/BE(5)#	GND	V(I/O)	C/BE(4)#	PAR64	GND
31	GND	AD(63)	AD(62)	AD(61)	GND	AD(60)	GND



<b>32</b>	GND	AD(59)	GND	V(I/O)	AD(58)	AD(57)	GND
<b>33</b>	GND	AD(56)	AD(55)	AD(54)	GND	AD(53)	GND
<b>34</b>	GND	AD(52)	GND	V(I/O)	AD(51)	AD(50)	GND
<b>35</b>	GND	AD(49)	AD(48)	AD(47)	GND	AD(46)	GND
<b>36</b>	GND	AD(45)	GND	V(I/O)	AD(44)	AD(43)	GND
<b>37</b>	GND	AD(42)	AD(41)	AD(40)	GND	AD(39)	GND
<b>38</b>	GND	AD(38)	GND	V(I/O)	AD(37)	AD(36)	GND
<b>39</b>	GND	AD(35)	AD(34)	AD(33)	GND	AD(32)	GND
<b>40</b>	GND	BRSV	GND	FAL#	REQ5#	GNT5#	GND
<b>41</b>	GND	BRSV	BRSV	DEG#	GND	BRSV	GND
<b>42</b>	GND	BRSV	GND	PRST#	REQ6#	GNT6#	GND
<b>43</b>	GND	USR	USR	USR	USR	USR	GND
<b>44</b>	GND	USR	USR	USR	USR	USR	GND
<b>45</b>	GND	USR	USR	USR	USR	USR	GND
<b>46</b>	GND	USR	USR	USR	USR	USR	GND
<b>47</b>	GND	USR	USR	USR	USR	USR	GND
	<b>Z</b>	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>	<b>E</b>	<b>F</b>

## Signal Descriptions:

### PRST

Push Button Reset.

### DEG

Power Supply Status DEG

### FAL

Power Supply Status FAL

### SYSEN

## System Slot Identification

*Contributor:* [Joakim Ögren](#), [Mark Sokos](#)

*Sources:*

[CompactPCI specifications v1.0](#) at [CompactPCI's homepage](#)

[Mark Sokos PCI page](#)

*"Inside the PCI Local Bus" by Guy W. Kendall, Byte, February 1994 v 19 p. 177-180*

*"The Indispensible PC Hardware Book" by Hans-Peter Messmer, ISBN 0-201-8769-3*

*Info: CompactPCI - An Open Industrial Computer Standard article by [Joseph S. Pavlat](#)*

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*Document last modified: 2001-06-08*



# ECBbus

**NOT  
DRAWN  
YET...**



(at the network device).

**NOT  
DRAWN  
YET...**



(at the transciever).

96 PIN DIN 41612 FEMALE at the backplane  
96 PIN DIN 41612 MALE at the boards.

The ECB-bus was defined in 1984 by the german company KONTRON.

It was defined for the 100x160mm-europa-card and used 2x32 pins of a 3x32-pin-connector (row a and c).

Later the third (middle) row of pins was defined for additional signals used in 16-bit-systems. This extended bus uses all 3x32pins.

## Row a & c (for 8 bit)

Pin	Name	Description
a1 +	5V +	5 volts dc
a2 D	5 D	ata line bit 5
a3	D6	Data line bit 6
a4	D3	Data line bit 3
a5	D4	Data line bit 4
a6	A2	Address 2
a7	A4	Address 4
a8	A5	Address 5

a9	A6	Address 6
a10	WAIT/	CPU wait
a11	BUSRQ/	bus request
a12		
a13		
a14		
a15		
a16		
a17		
a18	A14	address 14
a19		
a20	M1/	first cycle
a21		
a22		
a23		
a24		
a25		
a26		
a27	IORQ/	in/out request
a28	RFSH/	refresh cycle
a29	A13	address 13
a30	A9	address 9
a31	BUSAK/	bus acknowledge
a32	GND	signal ground

Pin	Name	Description
c1	+5V	+5 volts dc
c2	D0	Data line bit 0
c3	D7	Data line bit 7
c4	D2	Data line bit 2
c5	A0	Address 0
c6	A3	Address 3



c7	A1	Address 1
c8	A8	Address 8
c9	A7	Address 7
c10		
c11	IEI	interrupt enable in
c12		
c13		
c14	D1	Data line bit 1
c15		
c16	IEO	interrupt enable out
c17	A11	address 11
c18	A10	address 10
c19		
c20	NMI/	not maskable interrupt
c21	INT/	normal interrupt
c22	WR/	write cycle
c23		
c24	RD/	read cycle
c25	HALT/	cpu stopped
c26		
c27	A12	address 12
c28	A15	address 15
c29		
c30	MREQ/	memory request
c31	RESET/	cpu reset
c32	GND	signal ground

## Row b (additional for 16 bit)

Pin	Name	Description
b1	+5V	+5 volts dc

b2	A20	address 20
b3	A21	address 21
b4	A22	address 22
b5	A23	address 23
b6	D8	data line bit 8
b7	D9	data line bit 9
b8	D10	data line bit 10
b9	D11	data line bit 11
b10	D12	data line bit 12
b11	D13	data line bit 13
b12	D14	data line bit 14
b13	D15	data line bit 15
b14	IRQ7	interrupt 7
b15	IRQ6	interrupt 6
b16	IRQ5	interrupt 5
b17	IRQ4	interrupt 4
b18	IRQ3	interrupt 3
b19	IRQ2	interrupt 2
b20	IRQ1	interrupt 1
b21	IRQ0	interrupt 0
b22	IOWR	I/O write
b23	??	??
b24	IORC	I/O read
b25	MRDC	Mem read
b26	??	??
b27	MWRC	Mem write
b28	DS0	Data Select 0
b29	DS1	Data Select 1
b30	OFF	bus driver tristate
b31	LOCK	bus driver tristate disabled
b32	GND	signal ground

DS0	DS1	Description
0	0	data transfer 16-bit
0	1	only bit 0-7
1	0	only bit 8-15
1	1	no data transfer

*Note: / = Active Low*

*Contributor: [Gerd Wilken](#)*

*Source:  
One issue of the magazine computer-technik (c't) in 1984*

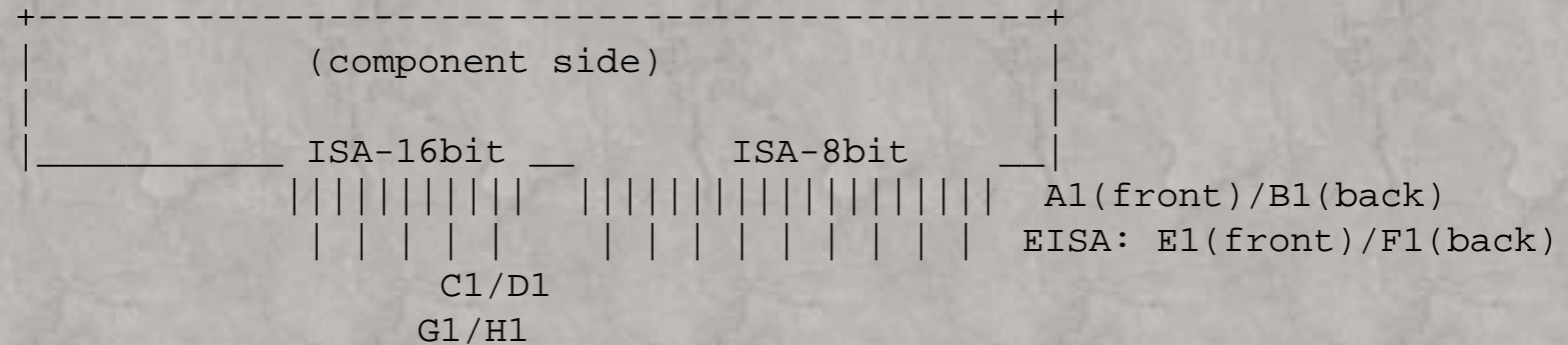
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# EISA

EISA=Extended Industry Standard Architecture.

Developed by Compaq, AST, Zenith, Tandy...



A,C,E,G=Component Side

A,B,F,H=Sold Side

**NOT  
DRAWN  
YET...**



(at the computer)

62+38 PIN EDGE CONNECTOR at the computer.

Pin	Name	Description
E1	CMD#	Command Phase
E2	START#	Start Phase
E3	EXRDY	EISA Ready
E4	EX32#	EISA Slave Size 32
E5	GND	Ground
E6	KEY	Access Key
E7	EX16#	EISA Slave Size 16
E8	SLBURST#	Slave Burst



E9	MSBURST#	Master Burst
E10	W/R#	Write/Read
E11	GND	Ground
E12	RES	Reserved
E13	RES	Reserved
E14	RES	Reserved
E15	GND	Ground
E16	KEY	Access Key
E17	BE1#	Byte Enable 1
E18	LA31#	Latchable Addressline 31
E19	GND	Ground
E20	LA30#	Latchable Addressline 30
E21	LA28#	Latchable Addressline 28
E22	LA27#	Latchable Addressline 27
E23	LA25#	Latchable Addressline 25
E24	GND	Ground
E25	KEY	Access Key
E26	LA15	Latchable Addressline 15
E27	LA13	Latchable Addressline 13
E28	LA12	Latchable Addressline 12
E29	LA11	Latchable Addressline 11
E30	GND	Ground
E31	LA9	Latchable Addressline 9
F1	GND	Ground
F2	+5V	+5 VDC
F3	+5V	+5 VDC
F4	---	
F5	---	
F6	KEY	Access Key
F7	---	
F8	---	

F9	+12V	+12 VDC
F10	M/IO#	Memory/Input-Output
F11	LOCK#	Lock bus
F12	RES	Reserved
F13	GND	Ground
F14	RES	Reserved
F15	BE3#	Byte Enable 3
F16	KEY	Access Key
F17	BE2#	Byte Enable 2
F18	BE0#	Byte Enable 0
F19	GND	Ground
F20	+5V	+5 VDC
F21	LA29#	Latchable Addressline 29
F22	GND	Ground
F23	LA26#	Latchable Addressline 26
F24	LA24#	Latchable Addressline 24
F25	KEY	Access Key
F26	LA16	Latchable Addressline 16
F27	LA14	Latchable Addressline 14
F28	+5V	+5 VDC
F29	+5V	+5 VDC
F30	GND	Ground
F31	LA10	Latchable Addressline 10
G1	LA7	Latchable Addressline 7
G2	GND	Ground
G3	LA4	Latchable Addressline 4
G4	LA3	Latchable Addressline 3
G5	GND	Ground
G6	KEY	Access Key
G7	D17	Data 17
G8	D19	Data 19

G9	D20	Data 20
G10	D22	Data 22
G11	GND	Ground
G12	D25	Data 25
G13	D26	Data 26
G14	D28	Data 28
G15	KEY	Access Key
G16	GND	Ground
G17	D30	Data 30
G18	D31	Data 31
G19	MREQx	Master Request
H1	LA8	Latchable Addressline 8
H2	LA6	Latchable Addressline 6
H3	LA5	Latchable Addressline 5
H4	+5V	+5 VDC
H5	LA2	Latchable Addressline 2
H6	KEY	Access Key
H7	D16	Data 16
H8	D18	Data 18
H9	GND	Ground
H10	D21	Data 21
H11	D23	Data 23
H12	D24	Data 24
H13	GND	Ground
H14	D27	Data 27
H15	KEY	Access Key
H16	D29	Data 29
H17	+5V	+5 VDC
H18	+5V	+5 VDC
H19	MAKx	Master Acknowledge

*Contributor:* [Joakim Ögren](#), [Mark Sokos](#)

*Sources:*

[Mark Sokos EISA page](#)

*"EISA System Architecture, 2nd Edition" by Tom Shanley and Don Anderson, ISBN 0-201-40995-X*  
[comp.sys.ibm.pc.hardware.\\* FAQ Part 4](#) - maintained by [Ralph Valentino](#)

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# EISA (technical)

This section is currently based solely on the work by Mark Sokos.

This file is intended to provide a basic functional overview of the EISA Bus, so that hobbyists and amateurs can design their own EISA compatible cards.

It is not intended to provide complete coverage of the EISA standard.

EISA is an acronym for Extended Industry Standard Architecture. It is an extension of the ISA architecture, which is a standardized version of the bus originally developed by IBM for their PC computers. EISA is upwardly compatible, which means that cards originally designed for the 8 bit IBM bus (often referred to as the XT bus) and cards designed for the 16 bit bus (referred to as the AT bus, and also as the ISA bus), will work in an EISA slot. EISA specific cards will not work in an AT or an XT slot.

The EISA connector uses multiple rows of connectors. The upper row is the same as a regular ISA slot, and the lower row contains the EISA extension. The slot is keyed so that ISA cards cannot be inserted to the point where they connect with the EISA signals.

## Signal Descriptions

### **+5, -5, +12, -12**

Power supplies. -5 is often not implemented.

### **AEN**

Address Enable. This is asserted when a DMAC has control of the bus. This prevents an I/O device from responding to the I/O command lines during a DMA transfer.

### **BALE**

Bus Address Latch Enable. The address bus is latched on the rising edge of this signal. The address on the SA bus is valid from the falling edge of BALE to the end of the bus cycle. Memory devices should

latch the LA bus on the falling edge of BALE.

## BCLK

Bus Clock, 33% Duty Cycle. Frequency Varies. 8.33 MHz is specified as the maximum, but many systems allow this clock to be set to 10 MHz and higher.

## BE(x)

Byte Enable. Indicates to the slave device which bytes on the data bus contain valid data. A 16 bit transfer would assert BE0 and BE1, for example, but not BE2 or BE3.

## CHCHK

Channel Check. A low signal generates an NMI. The NMI signal can be masked on a PC, externally to the processor (of course). Bit 7 of port 70(hex) (enable NMI interrupts) and bit 3 of port 61 (hex) (recognition of channel check) must both be set to zero for an NMI to reach the CPU.

## CHRDY

Channel Ready. Setting this low prevents the default ready timer from timing out. The slave device may then set it high again when it is ready to end the bus cycle. Holding this line low for too long can cause problems on some systems. CHRDY and NOWS should not be used simultaneously. This may cause problems with some bus controllers.

## CMD

Command Phase. This signal indicates that the current bus cycle is in the command phase. After the start phase (see START), the data is transferred during the CMD phase. CMD remains asserted from the falling edge of START until the end of the bus cycle.

## SD0-SD16

System Data lines. They are bi-directional and tri-state.

## DAKx

DMA Acknowledge.

## **DRQx**

DMA Request.

## **EX16**

EISA Slave Size 16. This is used by the slave device to inform the bus master that it is capable of 16 bit transfers.

## **EX32**

EISA Slave Size 32. This is used by the slave device to inform the bus master that it is capable of 32 bit transfers.

## **EXRDY**

EISA Ready. If this signal is asserted, the cycle will end on the next rising edge of BCLK. The slave device drives this signal low to insert wait states.

## **IO16**

I/O size 16. Generated by a 16 bit slave when addressed by a bus master.

## **IORC**

I/O Read Command line.

## **IOWC**

I/O Write Command line.

## **IRQx**

Interrupt Request. IRQ2 has the highest priority.

## **LApp**

Latchable Address lines.

## **LOCK**

Asserting this signal prevents other bus masters from requesting control of the bus.

## **MAKx**

Master Acknowledge for slot x: Indicates that the bus master request (MREQx) has been granted.

## **MASTER16**

16 bit bus master. Generated by the ISA bus master when initiating a bus cycle.

## **M/IO**

Memory/Input-Output. This is used to indicate whether the current bus cycle is a memory or an I/O operation.

## **M16**

Memory Access, 16 bit

## **MRDC**

Memory Read Command line.

## **MREQx**

Master Request for Slot x: This is a slot specific request for the device to become the bus master.

## **MSBURST**

Master Burst. The bus master asserts this signal in response to SLBURST. This tells the slave device that the bus master is also capable of burst cycles.

## **MWTC**

Memory Write Command line.



## NOWS

No Wait State. Used to shorten the number of wait states generated by the default ready timer. This causes the bus cycle to end more quickly, since wait states will not be inserted. Most systems will ignore NOWS if CHRDY is active (low). However, this may cause problems with some bus controllers, and both signals should not be active simultaneously.

## OSC

Oscillator, 14.318 MHz, 50% Duty Cycle. Frequency varies.

## REFRESH

Refresh. Generated when the refresh logic is bus master.

## RESDRV

This signal goes low when the machine is powered up. Driving it low will force a system reset.

## SA0-SA19

System Address Lines, tri-state.

## SBHE

System Bus High Enable, tri-state. Indicates a 16 bit data transfer.

## SLBURST

Slave Burst. The slave device uses this to indicate that it is capable of burst cycles. The bus master will respond with MSBURST if it is also capable of burst cycles.

## SMRDC

Standard Memory Read Command line. Indicates a memory read in the lower 1 MB area.

## SMWTC

Standard Memory Write Command line. Indicates a memory write in the lower 1 MB area.

## START

Start Phase. This signal is low when the current bus cycle is in the start phase. Address and M/IO signals are decoded during this phase. Data is transferred during the command phase (indicated by CMD).

## TC

Terminal Count. Notifies the CPU that the last DMA data transfer operation is complete.

## W/R

Write or Read. Used to indicate if the current bus cycle is a read or a write operation.

*Contributor:* [Joakim Ögren](#), [Mark Sokos](#)

*Sources:*

[Mark Sokos EISA page](#)

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# Electrocoin

The Electrocoin standard was introduced before JAMMA (Japanese Arcade Machine Manufacturers Association) to allow various games to be connected to generic cabinets such as Silverline and Goliaths. They use the same 28 way connector, but the designations are different. Pins 16 and 18 were 3 player and 4 player start buttons, and were superseded when 3 button games became popular. Pins 14 and 20 were free, but were used by us to allow for easy servicing of games.

28 PIN UNKNOWN CONNECTOR on the arcade machine

## Lower side:

Pin	Description
A	Ground
B	Ground
C	+5V
D	+5V
E	+12V
F	-5V
H	Not used
J	-12V
K	Keyway
L	Speaker 1
M	Speaker 1
N	Speaker 2
P	Player 2 Up
R	Speaker 2
S	Player 2 Right
T	Player 2 Button 1
U	Player 2

V	Player 2 Button 2
W	Player 2 Left
X	(Horizontal Sync)
Y	Player 2 Start
Z	Video Red
Aa	Video Green
Ab	Video Blue
Ac	Video Sync
Ad	Ground
Ae	Ground
Af	Ground

## Upper side:

Pin	Description
1	Ground
2	Ground
3	+5V
4	+5V
5	+12V
6	-5V
7	Not used
8	-12V
9	Keyway
10	Meter 1
11	Meter 2
12	Credit Board Meter
13	Player 1 Up
14	Test
15	Player 1 Right
16	Player 2 Button 3



17	Player 1 Down
18	Player 1 Button 3
19	Player 1 Left
20	Service
21	Player 1 Start
22	Player 1 Button 1
23	Player 1 Button 2
24	Coin 1
25	Coin 2
26	Ground
27	Ground
28	Ground

*Contributor:* [Joakim Ögren](#)

*Source:*

*Electrocoin pinout at* [Technick.net](#)

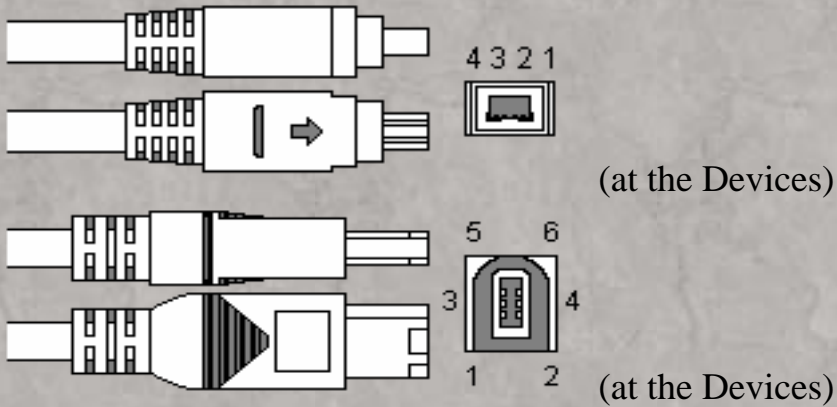
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*Document last modified:* 2001-06-08



# IEEE1394



4 PIN IEEE1394 FEMALE at the Devices.

6 PIN IEEE1394 FEMALE at the Devices.

Full name IEEE 1394-1995

Also known as FireWire (Apple), iLink (Sony) or Lynx

Pin	Name	Description
1	Power	Unregulated DC; 30 V no load
2	Ground	Ground return for power and inner cable shield
3	TPB-	Twisted-pair B, differential signals
4	TPB+	Twisted-pair B, differential signals
5	TPA-	Twisted-pair A, differential signals
6	TPA+	Twisted-pair A, differential signals
Shell	Outer	cable shield

Contributor: [Joakim Ögren](#)

Source:  
?

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# IEEE1394 (technical)

IEEE1394 was originally developed by Apple under the name Firewire.

## Features:

- Hot plug and unplug
- Easy of use
- 62 physical devices

## Bandwidth:

- Full speed: 400 Mbps speed
- Low speed: 200?? Mbps speed

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?

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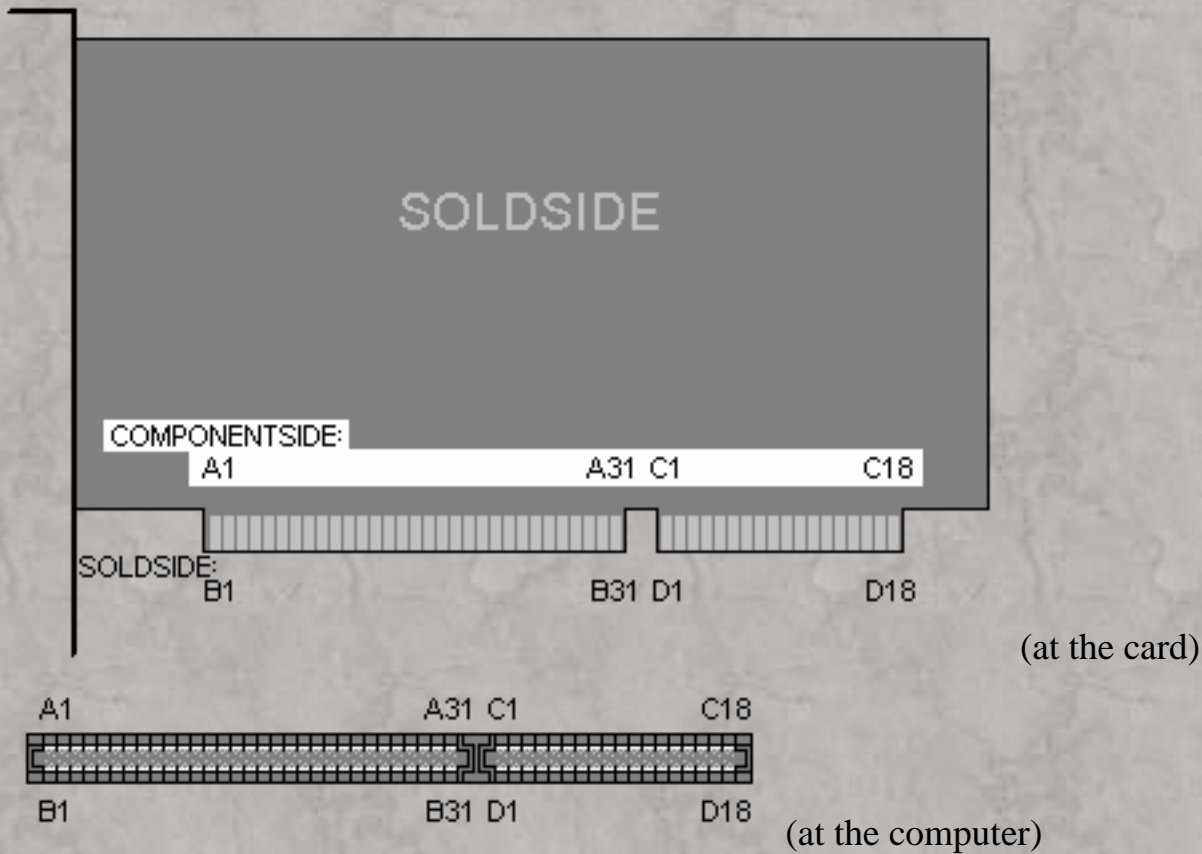
*Document last modified: 2001-06-06*





# ISA

ISA=Industry Standard Architecture





































62+36 PIN EDGE CONNECTOR MALE at the card.

62+36 PIN EDGE CONNECTOR FEMALE at the computer.

Pin	Name	Dir	Description
A1	/I/O CH CK	←	I/O channel check; active low=parity error
A2	D7	↔	Data bit 7
A3	D6	↔	Data bit 6
A4	D5	↔	Data bit 5
A5	D4	↔	Data bit 4
A6	D3	↔	Data bit 3

A7	D2		Data bit 2
A8	D1		Data bit 1
A9	D0		Data bit 0
A10	I/O CH RDY		I/O Channel ready, pulled low to lengthen memory cycles
A11	AEN		Address enable; active high when DMA controls bus
A12	A19		Address bit 19
A13	A18		Address bit 18
A14	A17		Address bit 17
A15	A16		Address bit 16
A16	A15		Address bit 15
A17	A14		Address bit 14
A18	A13		Address bit 13
A19	A12		Address bit 12
A20	A11		Address bit 11
A21	A10		Address bit 10
A22	A9		Address bit 9
A23	A8		Address bit 8
A24	A7		Address bit 7
A25	A6		Address bit 6
A26	A5		Address bit 5
A27	A4		Address bit 4
A28	A3		Address bit 3
A29	A2		Address bit 2
A30	A1		Address bit 1
A31	A0		Address bit 0
B1	GND		Ground
B2	RESET		Active high to reset or initialize system logic
B3	+5V		+5 VDC
B4	IRQ2		Interrupt Request 2
B5	-5VDC		-5 VDC
B6	DRQ2		DMA Request 2
B7	-12VDC		-12 VDC

B8	/N0WS		No WaitState
B9	+12VDC		+12 VDC
B10	GND		Ground
B11	/SMEMW		System Memory Write
B12	/SMEMR		System Memory Read
B13	/IOW		I/O Write
B14	/IOR		I/O Read
B15	/DACK3		DMA Acknowledge 3
B16	DRQ3		DMA Request 3
B17	/DACK1		DMA Acknowledge 1
B18	DRQ1		DMA Request 1
B19	/REFRESH		Refresh
B20	CLOCK		System Clock (67 ns, 8-8.33 MHz, 50% duty cycle)
B21	IRQ7		Interrupt Request 7
B22	IRQ6		Interrupt Request 6
B23	IRQ5		Interrupt Request 5
B24	IRQ4		Interrupt Request 4
B25	IRQ3		Interrupt Request 3
B26	/DACK2		DMA Acknowledge 2
B27	T/C		Terminal count; pulses high when DMA term. count reached
B28	ALE		Address Latch Enable
B29	+5V		+5 VDC
B30	OSC		High-speed Clock (70 ns, 14.31818 MHz, 50% duty cycle)
B31	GND		Ground
C1	SBHE		System bus high enable (data available on SD8-15)
C2	LA23		Address bit 23
C3	LA22		Address bit 22
C4	LA21		Address bit 21
C5	LA20		Address bit 20
C6	LA18		Address bit 19
C7	LA17		Address bit 18

C8	LA16		Address bit 17
C9	/MEMR		Memory Read (Active on all memory read cycles)
C10	/MEMW		Memory Write (Active on all memory write cycles)
C11	SD08		Data bit 8
C12	SD09		Data bit 9
C13	SD10		Data bit 10
C14	SD11		Data bit 11
C15	SD12		Data bit 12
C16	SD13		Data bit 13
C17	SD14		Data bit 14
C18	SD15		Data bit 15
D1	/MEMCS16		Memory 16-bit chip select (1 wait, 16-bit memory cycle)
D2	/IOCS16		I/O 16-bit chip select (1 wait, 16-bit I/O cycle)
D3	IRQ10		Interrupt Request 10
D4	IRQ11		Interrupt Request 11
D5	IRQ12		Interrupt Request 12
D6	IRQ15		Interrupt Request 15
D7	IRQ14		Interrupt Request 14
D8	/DACK0		DMA Acknowledge 0
D9	DRQ0		DMA Request 0
D10	/DACK5		DMA Acknowledge 5
D11	DRQ5		DMA Request 5
D12	/DACK6		DMA Acknowledge 6
D13	DRQ6		DMA Request 6
D14	/DACK7		DMA Acknowledge 7
D15	DRQ7		DMA Request 7
D16	+5 V		
D17	/MASTER		Used with DRQ to gain control of system
D18	GND		Ground

*Note: Direction is Motherboard relative ISA-Cards.*



*Note: B8 was /CARD SLCDTD on the XT. Card selected, activated by cards in XT's slot J8*

*Contributor: [Joakim Ögren](#), [Rob Gill](#)*

*Sources:*

*IBM PC/AT Technical Reference, pages 1-25 through 1-37*

*[comp.sys.ibm.pc.hardware.\\* FAQ Part 4](#) - maintained by [Ralph Valentino](#)*

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# ISA (technical)

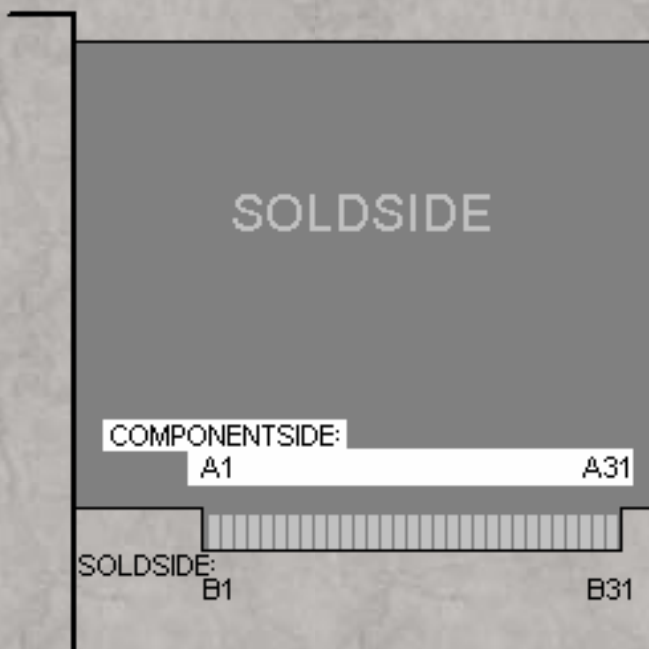
This file is designed to give a basic overview of the bus found in most IBM clone computers, often referred to as the XT or AT bus. The AT version of the bus is upwardly compatible, which means that cards designed to work on an XT bus will work on an AT bus. This bus was produced for many years without any formal standard. In recent years, a more formal standard called the ISA bus (Industry Standard Architecture) has been created, with an extension called the EISA (Extended ISA) bus also now as a standard. The EISA bus extensions will not be detailed here.

This file is not intended to be a thorough coverage of the standard. It is for informational purposes only, and is intended to give designers and hobbyists sufficient information to design their own XT and AT compatible cards.

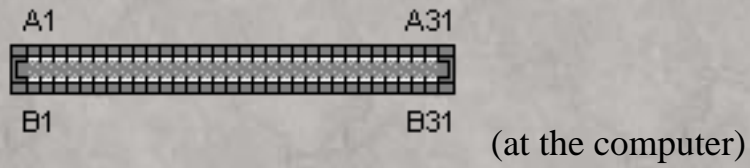
## Physical Design:

ISA cards can be either 8-bit or 16-bit. 8-bit cards only uses the first 62 pins and 16-bit cards uses all 98 pins. Some 8-bit cards uses some of the 16-bit extension pins to get more interrupts.

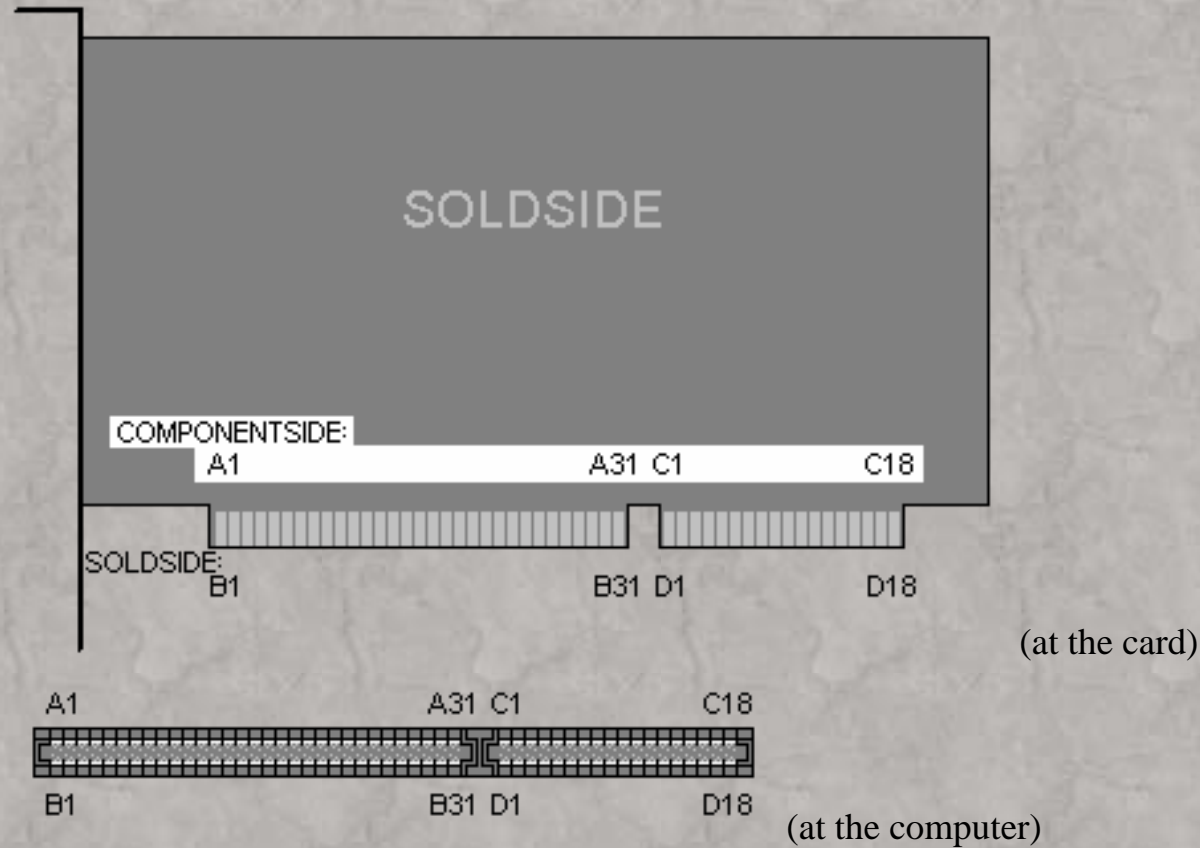
### 8-bit card:



(at the card)



## 16-bit card:



## Signal Descriptions:

### +5, -5, +12, -12

Power supplies. -5 is often not implemented.

### AEN

Address Enable. This is asserted when a DMAC has control of the bus. This prevents an I/O device from responding to the I/O command lines during a DMA transfer. When AEN is active, the DMA Controller has control of the address bus as the memory and I/O read/write command lines.

### BALE

**Bus Address Latch Enable.** The address bus is latched on the rising edge of this signal. The address on the SA bus is valid from the falling edge of BALE to the end of the bus cycle. Memory devices should latch the LA bus on the falling edge of BALE. Some references refer to this signal as Buffered Address Latch Enable, or just Address Latch Enable (ALE). The Buffered-Address Latch Enable is used to latch SA0-19 on the falling edge. This signal is forced high during DMA cycles.

## **BCLK**

**Bus Clock, 33% Duty Cycle. Frequency Varies. 4.77 to 8 MHz typical. 8.3 MHz is specified as the maximum, but many systems allow this clock to be set to 12 MHz and higher.**

## **DACKx**

**DMA Acknowledge.** The active-low DMA Acknowledge 0 to 3 and 5 to 7 are the corresponding acknowledge signals for DRQ 0-3, 5-7.

## **DRQx**

**DMA Request.** These signals are asynchronous channel requests used by I/O channel devices to gain DMA service. DMA request channels 0-3 are for 8-bit data transfer. DAM request channels 5-7 are for 16-bit data transfer. DMA request channel 4 is used internally on the system board. DMA requests should be held high until the corresponding DACK line goes active. DMA requests are serviced in the following priority sequence:

High: DRQ 0, 1, 2, 3, 5, 6, 7 Lowest

## **IOCS16**

**I/O size 16.** Generated by a 16 bit slave when addressed by a bus master. The active-low I/O Chip Select 16 indicates that the current transfer is a 1 wait state, 16 bit I/O cycle. Open Collector.

## **I/O CH CK**

**Channel Check.** A low signal generates an NMI. The NMI signal can be masked on a PC, externally to the processor (of course). Bit 7 of port 70(hex) (enable NMI interrupts) and bit 3 of port 61 (hex) (recognition of channel check) must both be set to zero for an NMI to reach the cpu. The I/O Channel Check is an active-low signal which indicates that a parity error exists in a device on the I/O channel.

## **I/O CH RDY**

**Channel Ready.** Setting this low prevents the default ready timer from timing out. The slave device may



then set it high again when it is ready to end the bus cycle. Holding this line low for too long (15 microseconds, typical) can prevent RAM refresh cycles on some systems. This signal is called IOCHRDY (I/O Channel Ready) by some references. CHRDY and NOWS should not be used simultaneously. This may cause problems with some bus controllers. This signal is pulled low by a memory or I/O device to lengthen memory or I/O read/write cycles. It should only be held low for a minimum of 2.5 microseconds.

## **IOR**

The I/O Read is an active-low signal which instructs the I/O device to drive its data onto the data bus, SD0-SD15.

## **IOW**

The I/O Write is an active-low signal which instructs the I/O device to read data from the data bus, SD0-SD15.

## **IRQx**

Interrupt Request. IRQ2 has the highest priority. IRQ 10-15 are only available on AT machines, and are higher priority than IRQ 3-7. The Interrupt Request signals which indicate I/O service attention. They are prioritized in the following sequence: Highest IRQ 9(2),10,11,12,14,3,4,5,6,7

## **LApp**

Latchable Address lines. Combine with the lower address lines to form a 24 bit address space (16 MB) These unlatched address signals give the system up to 16 MB of address ability. The are valid when "BALE" is high.

## **MASTER**

16 bit bus master. Generated by the ISA bus master when initiating a bus cycle. This active-low signal is used in conjunction with a DRQ line by a processor on the I/O channel to gain control of the system. The I/O processor first issues a DRQ, and upon receiving the corresponding DACK, the I/O processor may assert MASTER, which will allow it to control the system address, data and control lines. This signal should not be asserted for more than 15 microseconds, or system memory may be corrupted du to the lack of memory refresh activity.

## **MEMCS16**

The active-low Memory Chip Select 16 indicates that the current data transfer is a 1 wait state, 16 bit data

memory cycle.

## MEMR

The Memory Read is an active-low signal which instructs memory devices to drive data onto the data bus SD0-SD15. This signal is active on all memory read cycles.

## MEMW

The Memory Write is an active-low signal which instructs memory devices to store data present on the data bus SD0-SD15. This signal is active on all memory write cycles.

## NOWS

No Wait State. Used to shorten the number of wait states generated by the default ready timer. This causes the bus cycle to end more quickly, since wait states will not be inserted. Most systems will ignore NOWS if CHRDY is active (low). However, this may cause problems with some bus controllers, and both signals should not be active simultaneously.

## OSC

Oscillator, 14.31818 MHz, 50% Duty Cycle. Frequency varies. This was originally divided by 3 to provide the 4.77 MHz cpu clock of early PCs, and divided by 12 to produce the 1.19 MHz system clock. Some references have placed this signal as low as 1 MHz (possibly referencing the system clock), but most modern systems use 14.318 MHz.

This frequency (14.318 MHz) is four times the television colorburst frequency. Refresh timing on many PC's is based on OSC/18, or approximately one refresh cycle every 15 microseconds. Many modern motherboards allow this rate to be changed, which frees up some bus cycles for use by software, but also can cause memory errors if the system RAM cannot handle the slower refresh rates.

## REFRESH

Refresh. Generated when the refresh logic is bus master. This active-low signal is used to indicate a memory refresh cycle is in progress. An ISA device acting as bus master may also use this signal to initiate a refresh cycle.

## RESET

This signal goes low when the machine is powered up. Driving it low will force a system reset. This signal goes high to reset the system during powerup, low line-voltage or hardware reset. ??????????????

## SA0-SA19

System Address Lines, tri-state. The System Address lines run from bit 0 to bit 19. They are latched on to the falling edge of "BALE".

## SBHE

System Bus High Enable, tri-state. Indicates a 16 bit data transfer. The System Bus High Enable indicates high byte transfer is occurring on the data bus SD8-SD15. This may also indicate an 8 bit transfer using the upper half of the bus data (if an odd address is present).

## SD0-SD16

System Data lines, or Standard Data Lines. They are bidirectional and tri-state. On most systems, the data lines float high when not driven. These 16 lines provide for data transfer between the processor, memory and I/O devices.

## SMEMR

System Memory Read Command line. Indicates a memory read in the lower 1 MB area. This System Memory Read is an active-low signal which instructs memory devices to drive data onto the data bus SD0-SD15. This signal is active only when the memory address is within the lowest 1MB of memory address space.

## SMEMW

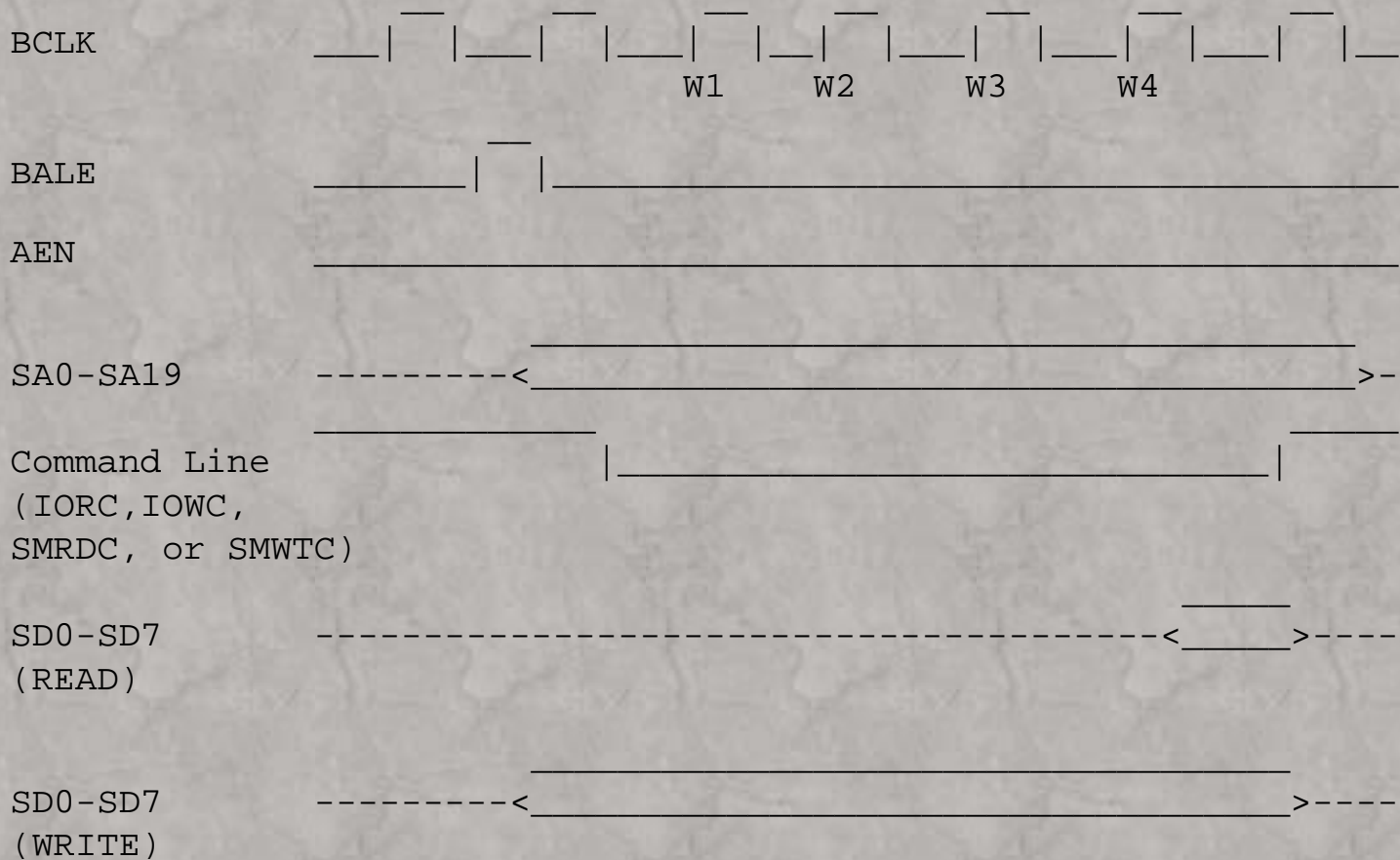
System Memory Write Command line. Indicates a memory write in the lower 1 MB area. The System Memory Write is an active-low signal which instructs memory devices to store data preset on the data bus SD0-SD15. This signal is active only when the memory address is within the lowest 1MB of memory address space.

## T/C

Terminal Count. Notifies the cpu that that the last DMA data transfer operation is complete. Terminal Count provides a pulse when the terminal count for any DMA channel is reached.

# 8 Bit Memory or I/O Transfer Timing Diagram (4 wait states shown)





Note: W1 through W4 indicate wait cycles.

BALE is placed high, and the address is latched on the SA bus. The slave device may safely sample the address during the falling edge of BALE, and the address on the SA bus remains valid until the end of the transfer cycle. Note that AEN remains low throughout the entire transfer cycle.

The command line is then pulled low (IORC or IOWC for I/O commands, SMRDSC or SMWTC for memory commands, read and write respectively). For write operations, the data remains on the SD bus for the remainder of the transfer cycle. For read operations, the data must be valid on the falling edge of the last cycle.

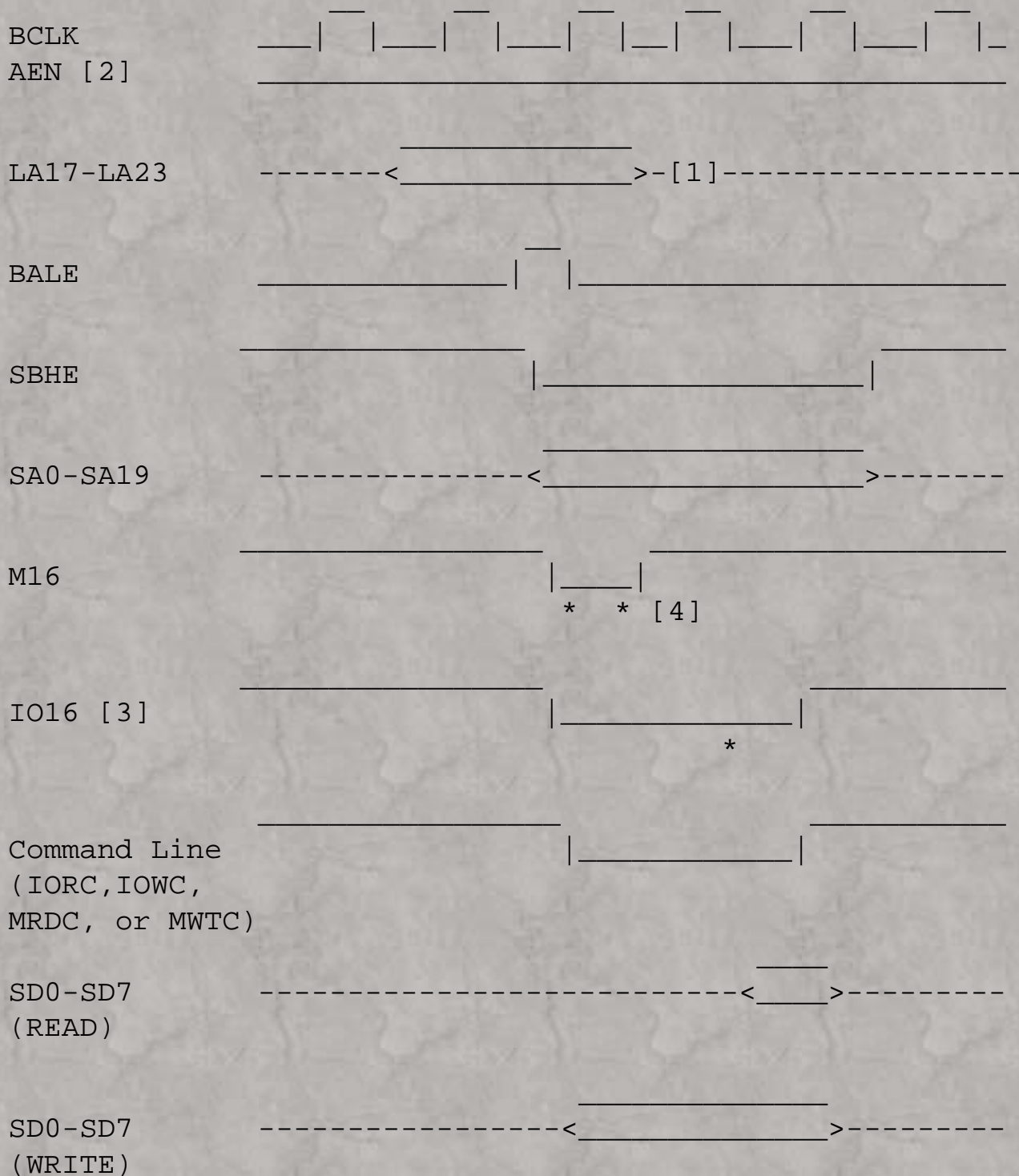
NOWS is sampled at the midpoint of each wait cycle. If it is low, the transfer cycle terminates without further wait states. CHRDY is sampled during the first half of the clock cycle. If it is low, further wait cycles will be inserted.

The default for 8 bit transfers is 4 wait states. Some computers allow the number of default wait states to be changed.

## 16 Bit Memory or I/O Transfer Timing Diagram (1



# wait state shown)



An asterisk (\*) denotes the point where the signal is sampled.

[1] The portion of the address on the LA bus for the NEXT cycle may now be placed on the bus. This is used so that cards may begin decoding the address early. Address pipelining must be active.

[2] AEN remains low throughout the entire transfer cycle, indicating that a normal (non-DMA) transfer is

occurring.

[3] Some bus controllers sample this signal during the same clock cycle as M16, instead of during the first wait state, as shown above. In this case, IO16 needs to be pulled low as soon as the address is decoded, which is before the I/O command lines are active.

[4] M16 is sampled a second time, in case the adapter card did not active the signal in time for the first sample (usually because the memory device is not monitoring the LA bus for early address information, or is waiting for the falling edge of BALE).

16 bit transfers follow the same basic timing as 8 bit transfers. A valid address may appear on the LA bus prior to the beginning of the transfer cycle. Unlike the SA bus, the LA bus is not latched, and is not valid for the entire transfer cycle (on most computers). The LA bus should be latched on the falling edge of BALE. Note that on some systems, the LA bus signals will follow the same timing as the SA bus. On either type of system, a valid address is present on the falling edge of BALE.

I/O adapter cards do not need to monitor the LA bus or BALE, since I/O addresses are always within the address space of the SA bus.

SBHE will be pulled low by the system board, and the adapter card must respond with IO16 or M16 at the appropriate time, or else the transfer will be split into two separate 8 bit transfers. Many systems expect IO16 or M16 before the command lines are valid. This requires that IO16 or M16 be pulled low as soon as the address is decoded (before it is known whether the cycle is I/O or Memory). If the system is starting a memory cycle, it will ignore IO16 (and vice-versa for I/O cycles and M16).

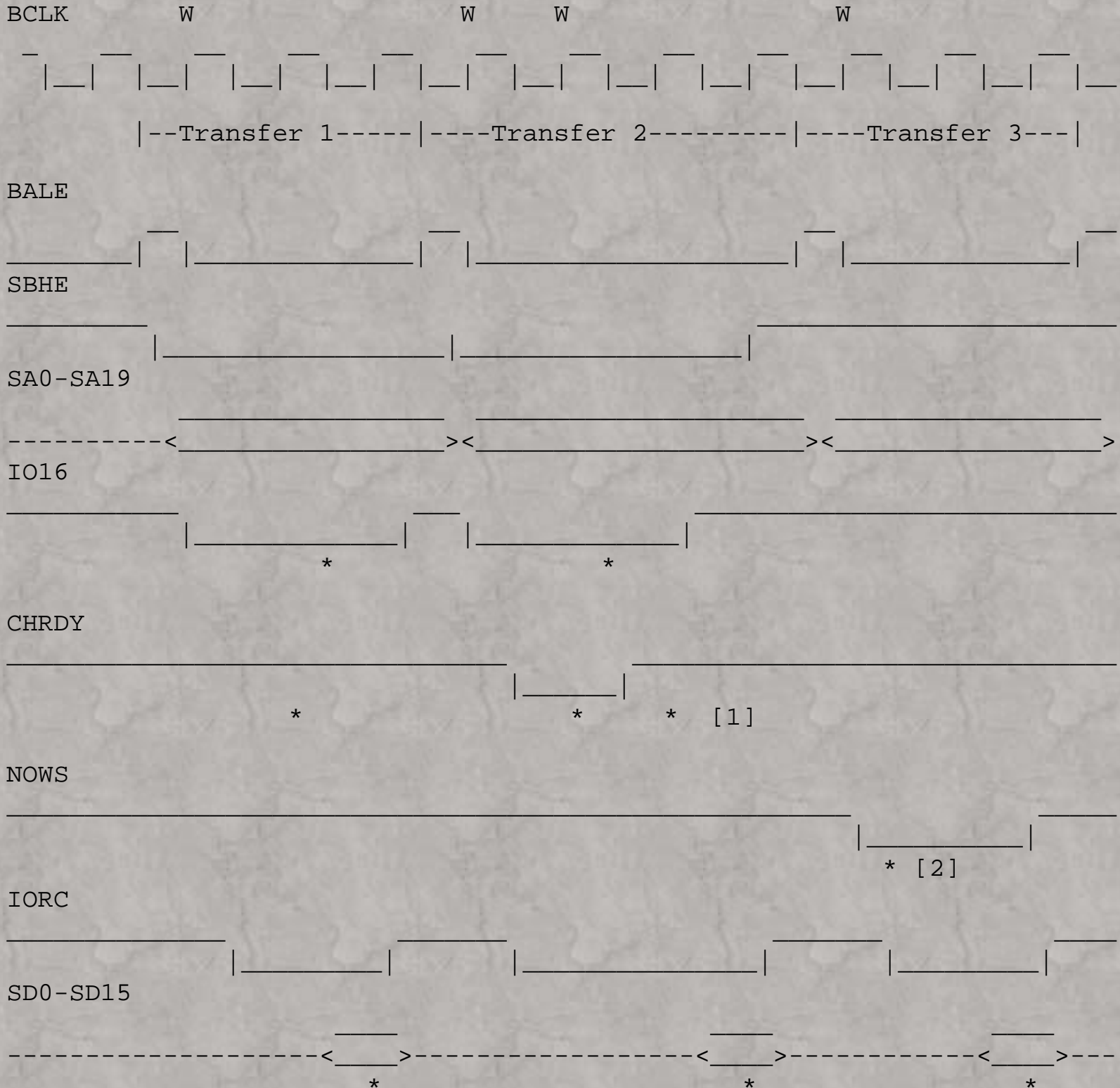
For read operations, the data is sampled on the rising edge of the last clock cycle. For write operations, valid data appears on the bus before the end of the cycle, as shown in the timing diagram. While the timing diagram indicates that the data needs to be sampled on the rising clock, on most systems it remains valid for the entire clock cycle.

The default for 16 bit transfers is 1 wait state. This may be shortened or lengthened in the same manner as 8 bit transfers, via NOWS and CHRDY. Many systems only allow 16 bit memory devices (and not I/O devices) to transfer using 0 wait states (NOWS has no effect on 16 bit I/O cycles).

SMRDC/SMWTC follow the same timing as MRDC/MWTC respectively when the address is within the lower 1 MB. If the address is not within the lower 1 MB boundary, SMRDC/SMWTC will remain high during the entire cycle.

It is also possible for an 8 bit bus cycle to use the upper portion of the bus. In this case, the timing will be similar to a 16 bit cycle, but an odd address will be present on the bus. This means that the bus is transferring 8 bits using the upper data bits (SD8-SD15).

# Shortening or Lengthening the bus cycle:



An asterisk (\*) denotes the point where the signal is sampled.

W=Wait Cycle

This timing diagram shows three different transfer cycles. The first is a 16 bit standard I/O read. This is



followed by an almost identical 16 bit I/O read, with one wait state inserted. The I/O device pulls CHRDY low to indicate that it is not ready to complete the transfer (see [1]). This inserts a wait cycle, and CHRDY is again sampled. At this second sample, the I/O device has completed its operation and released CHRDY, and the bus cycle now terminates. The third cycle is an 8 bit transfer, which is shortened to 1 wait state (the default is 4) by the use of NOWS.

## I/O Port Addresses

Note: Only the first 10 address lines are decoded for I/O operations. This limits the I/O address space to address 3FF (hex) and lower. Some systems allow for 16 bit I/O address space, but may be limited due to some I/O cards only decoding 10 of these 16 bits.

Port (hex)	Port Assignments
000-00F	DMA Controller
010-01F	DMA Controller (PS/2)
020-02F	Master Programmable Interrupt Controller (PIC)
030-03F	Slave PIC
040-05F	Programmable Interval Timer (PIT)
060-06F	Keyboard Controller
070-071	Real Time Clock
080-083	DMA Page Register
090-097	Programmable Option Select (PS/2)
0A0-0AF	PIC #2
0C0-0CF	DMAC #2
0E0-0EF	reserved
0F0-0FF	Math coprocessor, PCJr Disk Controller
100-10F	Programmable Option Select (PS/2)
110-16F	AVAILABLE
170-17F	Hard Drive 1 (AT)
180-1EF	AVAILABLE
1F0-1FF	Hard Drive 0 (AT)
200-20F	Game Adapter
210-217	Expansion Card Ports
220-26F	AVAILABLE



278-27F	Parallel Port 3
280-2A1	AVAILABLE
2A2-2A3	clock
2B0-2DF	EGA/Video
2E2-2E3	Data Acquisition Adapter (AT)
2E8-2EF	Serial Port COM4
2F0-2F7	Reserved
2F8-2FF	Serial Port COM2
300-31F	Prototype Adapter, Periscope Hardware Debugger
320-32F	AVAILABLE
330-33F	Reserved for XT/370
340-35F	AVAILABLE
360-36F	Network
370-377	Floppy Disk Controller
378-37F	Parallel Port 2
380-38F	SDLC Adapter
390-39F	Cluster Adapter
3A0-3AF	reserved
3B0-3BF	Monochrome Adapter
3BC-3BF	Parallel Port 1
3C0-3CF	EGA/VGA
3D0-3DF	Color Graphics Adapter
3E0-3EF	Serial Port COM3
3F0-3F7	Floppy Disk Controller
3F8-3FF	Serial Port COM1

Soundblaster cards usually use I/O ports 220-22F.  
Data acquisition cards frequently use 300-31F.

## DMA Read and Write

The ISA bus uses two DMA controllers (DMAC) cascaded together. The slave DMAC connects to the master DMAC via DMA channel 4 (channel 0 on the master DMAC). The slave therefore gains control of

the bus through the master DMAC. On the ISA bus, the DMAC is programmed to use fixed priority (channel 0 always has the highest priority), which means that channel 0-4 from the slave have the highest priority (since they connect to the master channel 0), followed by channels 5-7 (which are channel 1-3 on the master).

The DMAC can be programmed for read transfers (data is read from memory and written to the I/O device), write transfers (data is read from the I/O device and written to memory), or verify transfers (neither a read or a write - this was used by DMA CH0 for DRAM refresh on early PCs).

Before a DMA transfer can take place, the DMA Controller (DMAC) must be programmed. This is done by writing the start address and the number of bytes to transfer (called the transfer count) and the direction of the transfer to the DMAC. After the DMAC has been programmed, the device may activate the appropriate DMA request (DRQx) line.

## Slave DMA Controller

I/O	Port
0000	DMA CH0 Memory Address Register Contains the lower 16 bits of the memory address, written as two consecutive bytes.
0001	DMA CH0 Transfer Count Contains the lower 16 bits of the transfer count, written as two consecutive bytes.
0002	DMA CH1 Memory Address Register
0003	DMA CH1 Transfer Count
0004	DMA CH2 Memory Address Register
0005	DMA CH2 Transfer Count
0006	DMA CH3 Memory Address Register
0007	DMA CH3 Transfer Count
0008	DMAC Status/Control Register Status (I/O read) bits 0-3: Terminal Count, CH 0-3 - bits 4-7: Request CH0-3 Control (write) - bit 0: Mem to mem enable (1 = enabled) - bit 1: ch0 address hold enable (1 = enabled) - bit 2: controller disable (1 = disabled) - bit 3: timing (0 = normal, 1 = compressed) - bit 4: priority (0 = fixed, 1 = rotating) - bit 5: write selection (0 = late, 1 = extended) - bit 6: DRQx sense asserted (0 = high, 1 = low) - bit 7: DAKn sense asserted (0 = low, 1 = high)

0009	Software DRQn Request - bits 0-1: channel select (CH0-3) - bit 2: request bit (0 = reset, 1 = set)
000A	DMA mask register - bits 0-1: channel select (CH0-3) - bit 2: mask bit (0 = reset, 1 = set)
000B	DMA Mode Register - bits 0-1: channel select (CH0-3) - bits 2-3: 00 = verify transfer, 01 = write transfer, 10 = read transfer, 11 = reserved - bit 4: Auto init (0 = disabled, 1 = enabled) - bit 5: Address (0 = increment, 1 = decrement) - bits 6-7: 00 = demand transfer mode, 01 = single transfer mode, 10 = block transfer mode, 11 = cascade mode
000C	DMA Clear Byte Pointer Writing to this causes the DMAC to clear the pointer used to keep track of 16 bit data transfers into and out of the DMAC for hi/low byte sequencing.
000D	DMA Master Clear (Hardware Reset)
000E	DMA Reset Mask Register - clears the mask register
000F	DMA Mask Register - bits 0-3: mask bits for CH0-3 (0 = not masked, 1 = masked)
0081	DMA CH2 Page Register (address bits A16-A23)
0082	DMA CH3 Page Register
0083	DMA CH1 Page Register
0087	DMA CH0 Page Register
0089	DMA CH6 Page Register
008A	DMA CH7 Page Register
008B	DMA CH5 Page Register

## Master DMA Controller

I/O	Port
00C0	DMA CH4 Memory Address Register Contains the lower 16 bits of the memory address, written as two consecutive bytes.
00C2	DMA CH4 Transfer Count Contains the lower 16 bits of the transfer count, written as two consecutive bytes.
00C4	DMA CH5 Memory Address Register



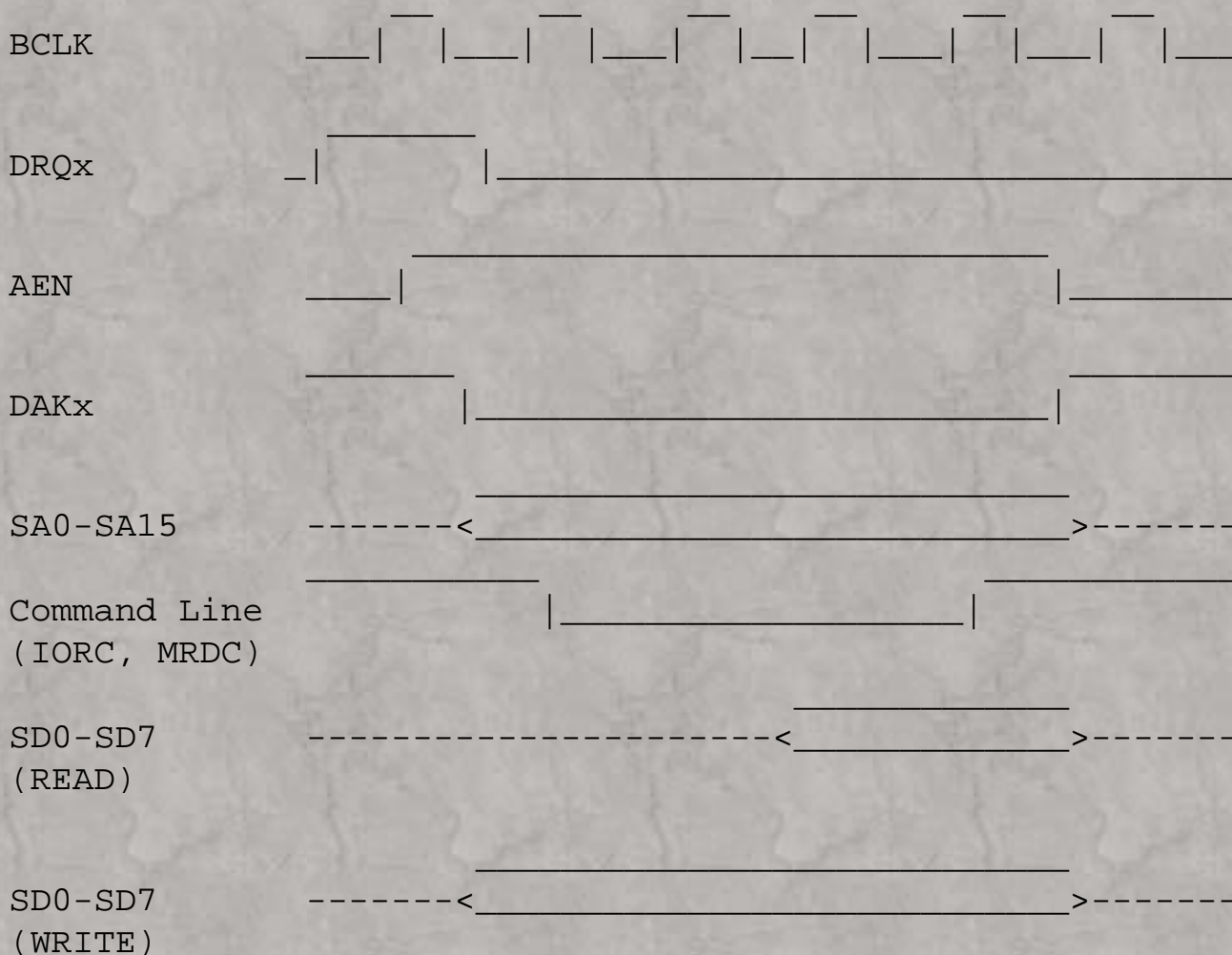
00C6	DMA CH5 Transfer Count
00C8	DMA CH6 Memory Address Register
00CA	DMA CH6 Transfer Count
00CC	DMA CH7 Memory Address Register
00CE	DMA CH7 Transfer Count
00D0	<p>DMAC Status/Control Register</p> <p>Status (I/O read) bits 0-3: Terminal Count, CH 4-7</p> <ul style="list-style-type: none"> <li>- bits 4-7: Request CH4-7</li> </ul> <p>Control (write)- bit 0: Mem to mem enable (1 = enabled)</p> <ul style="list-style-type: none"> <li>- bit 1: ch0 address hold enable (1 = enabled)</li> <li>- bit 2: controller disable (1 = disabled)</li> <li>- bit 3: timing (0 = normal, 1 = compressed)</li> <li>- bit 4: priority (0 = fixed, 1 = rotating)</li> <li>- bit 5: write selection (0 = late, 1 = extended)</li> <li>- bit 6: DRQx sense asserted (0 = high, 1 = low)</li> <li>- bit 7: DAKn sense asserted (0 = low, 1 = high)</li> </ul>
00D2	<p>Software DRQn Request</p> <ul style="list-style-type: none"> <li>- bits 0-1: channel select (CH4-7)</li> <li>- bit 2: request bit (0 = reset, 1 = set)</li> </ul>
00D4	<p>DMA mask register</p> <ul style="list-style-type: none"> <li>- bits 0-1: channel select (CH4-7)</li> <li>- bit 2: mask bit (0 = reset, 1 = set)</li> </ul>
00D6	<p>DMA Mode Register</p> <ul style="list-style-type: none"> <li>- bits 0-1: channel select (CH4-7)</li> <li>- bits 2-3: 00 = verify transfer, 01 = write transfer, 10 = read transfer, 11 = reserved</li> <li>- bit 4: Auto init (0 = disabled, 1 = enabled)</li> <li>- bit 5: Address (0 = increment, 1 = decrement)</li> <li>- bits 6-7: 00 = demand transfer mode, 01 = single transfer mode, 10 = block transfer mode, 11 = cascade mode</li> </ul>
00D8	<p>DMA Clear Byte Pointer</p> <p>Writing to this causes the DMAC to clear the pointer used to keep track of 16 bit data transfers into and out of the DMAC for hi/low byte sequencing.</p>
00DA	DMA Master Clear (Hardware Reset)
00DC	DMA Reset Mask Register - clears the mask register
00DE	<p>DMA Mask Register</p> <ul style="list-style-type: none"> <li>- bits 0-3: mask bits for CH4-7 (0 = not masked, 1 = masked)</li> </ul>

## Single Transfer Mode



The DMAC is programmed for transfer. The DMA device requests a transfer by driving the appropriate DRQ line high. The DMAC responds by asserting AEN and acknowledges the DMA request through the appropriate DAK line. The I/O and memory command lines are also asserted. When the DMA device sees the DAK signal, it drops the DRQ line.

The DMAC places the memory address on the SA bus (at the same time as the command lines are asserted), and the device either reads from or writes to memory, depending on the type of transfer. The transfer count is incremented, and the address incremented/decremented. DAK is de-asserted. The cpu now once again has control of the bus, and continues execution until the I/O device is once again ready for transfer. The DMA device repeats the procedure, driving DRQ high and waiting for DAK, then transferring data. This continues for a number of cycles equal to the transfer count. When this has been completed, the DMAC signals the cpu that the DMA transfer is complete via the TC (terminal count) signal.



## Block Transfer Mode

The DMAC is programmed for transfer. The device attempting DMA transfer drives the appropriate DRQ

line high. The motherboard responds by driving AEN high and DAK low. This indicates that the DMA device is now the bus master. In response to the DAK signal, the DMA device drops DRQ. The DMAC places the address for DMA transfer on the address bus. Both the memory and I/O command lines are asserted (since DMA involves both an I/O and a memory device). AEN prevents I/O devices from responding to the I/O command lines, which would not result in proper operation since the I/O lines are active, but a memory address is on the address bus. The data transfer is now done (memory read or write), and the DMAC increments/decrements the address and begins another cycle. This continues for a number of cycles equal to the DMAC transfer count. When this has been completed, the terminal count signal (TC) is generated by the DMAC to inform the cpu that the DMA transfer has been completed.

Note: Block transfer must be used carefully. The bus cannot be used for other things (like RAM refresh) while block mode transfers are being done.

## Demand Transfer Mode

The DMAC is programmed for transfer. The device attempting DMA transfer drives the appropriate DRQ line high. The motherboard responds by driving AEN high and DAK low. This indicates that the DMA device is now the bus master. Unlike single transfer and block transfer, the DMA device does not drop DRQ in response to DAK. The DMA device transfers data in the same manner as for block transfers. The DMAC will continue to generate DMA cycles as long as the I/O device asserts DRQ. When the I/O device is unable to continue the transfer (if it no longer had data ready to transfer, for example), it drops DRQ and the cpu once again has control of the bus. Control is returned to the DMAC by once again asserting DRQ. This continues until the terminal count has been reached, and the TC signal informs the cpu that the transfer has been completed.

## Interrupts on the ISA bus

Name	Interrupt	Description
NMI	2	Parity Error, Mem Refresh
IRQ0	8	8253 Channel 0 (System Timer)
IRQ1	9	Keyboard
IRQ2	A	Cascade from slave PIC
IRQ3	B	COM2
IRQ4	C	COM1
IRQ5	D	LPT2
IRQ6	E	Floppy Drive Controller
IRQ7	F	LPT1

IRQ8	F	Real Time Clock
IRQ9	F	Redirection to IRQ2
IRQ10	F	Reserved
IRQ11	F	Reserved
IRQ12	F	Mouse Interface
IRQ13	F	Coprocessor
IRQ14	F	Hard Drive Controller
IRQ15	F	Reserved

IRQ0,1,2,8, and 13 are not available on the ISA bus.

The IBM PC and XT had only a single 8259 interrupt controller. The AT and later machines have a second interrupt controller, and the two are used in a master/slave combination. IRQ2 and IRQ9 are the same pin on most ISA systems. Interrupts on most systems may be either edge triggered or level triggered. The default is usually edge triggered, and active high (low to high transition). The interrupt level must be held high until the first interrupt acknowledge cycle (two interrupt acknowledge bus cycles are generated in response to an interrupt request).

The software aspects of interrupts and interrupt handlers is intentionally omitted from this document, due to the numerous syntactical differences in software tools and the fact that adequate documentation of this topic is usually provided with development software.

## Bus Mastering:

An ISA device may take control of the bus, but this must be done with caution. There are no safety mechanisms involved, and so it is easily possible to crash the entire system by incorrectly taking control of the bus. For example, most systems require bus cycles for DRAM refresh. If the ISA bus master does not relinquish control of the bus or generate its own DRAM refresh cycles every 15 microseconds, the system RAM can become corrupted. The ISA adapter card can generate refresh cycles without relinquishing control of the bus by asserting REFRESH. MRDC can be then monitored to determine when the refresh cycle ends.

To take control of the bus, the device first asserts its DRQ line. The DMAC sends a hold request to the cpu, and when the DMAC receives a hold acknowledge, it asserts the appropriate DAK line corresponding to the DRQ line asserted. The device is now the bus master. AEN is asserted, so if the device wishes to access I/O devices, it must assert MASTER16 to release AEN. Control of the bus is returned to the system board by releasing DRQ.

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*Source:*

*[Mark Sokos ISA page](#)*

*"ISA System Architecture, 3rd Edition" by Tom Shanley and Don Anderson ISBN 0-201-40996-8*

*"Eisa System Architecture, 2nd Edition" by Tom Shanley and Don Anderson ISBN 0-201-40995-X*

*"Microcomputer Busses" by R.M. Cram ISBN 0-12-196155-9*

*HelpPC v2.10 Quick Reference Utility, by David Jurgens*

*ZIDA 80486 Mother Board User's Manual, OPTi 486, 82C495sx*

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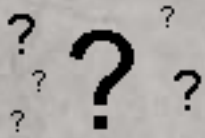
# IndustrialPCI

PCI=Peripheral Component Interconnect.

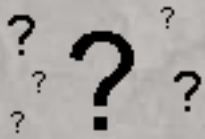
IndustrialPCI is a version of PCI adapted for industrial and/or embedded applications.

The IPCI connector has three parts:

- Optional 60 pin PCI 64 bit extension (Top)
- Mandatory 120 pin PCI 32 bit (Middle)
- Optional 60 pin Custom I/O (Bottom)



(at the backplane)



(at the device (card))

UNKNOWN CONNECTOR at the backplane.

UNKNOWN CONNECTOR at the device (card).

## System Slot (Middle)

Pin	Name	Description	Note
A1	+3,3V	+3.3 VDC	
A2	AD2	Address 2	
A3	AD6	Address 6	
A4	GND	Ground	
A5	AD10	Address 10	
A6	AD13	Address 13	
A7	GND	Ground	

A8	SDONE	Snoop Done	1
A9	GND	Ground	
A10	FRAME#	Indicate Address or Data phase	1
A11	AD18	Address 18	
A12	GND	Ground	
A13	+5V	+5 VDC	
A14	AD24	Address 24	
A15	AD27	Address 27	
A16	GND	Ground	
A17	REQ2	Request 2	1
A18	GND	Ground	
A19	CLK1	33 or 66 MHz Clock	
A20	CLK2		
A21	GND	Ground	
A22	CLK3		
A23	CLK4		
A24	+3,3V	+3.3 VDC	
B1	REQ64#	Request 64 ???	1
B2	AD3	Address 3	
B3	+5V	+5 VDC	
B4	AD8	Address 8	
B5	+3,3V	+3.3 VDC	
B6	AD14	Address 14	
B7	PAR	Parity	
B8	+3,3V	+3.3 VDC	
B9	STOP#	Stop	1
B10	C/BE2#	Command, Byte Enable 2	
B11	V(I/O)	+3.3 or +5 VDC	
B12	AD21	Address 21	
B13	+3,3V	+3.3 VDC	
B14	V(I/O)	+3.3 or +5 VDC	
B15	AD28	Address 28	

B16	AD31	Address 31	
B17	+3,3V	+3.3 VDC	
B18	GNT3	Grant 3	
B19	RST#	Reset	
B20	NMI#	Non Maskable Interrupt	
B21	X6	Reserved (6)	
B22	+5V	+5 VDC	:
B23	RSTIN#		2
B24	USB+	Universal Serial Bus (USB)(+)	
C1	ACK64#	Acknowledge 64 ???	1
C2	GND	Ground	
C3	AD7	Address 7	
C4	AD9	Address 9	
C5	AD11	Address 11	
C6	GND	Ground	
C7	SERR#	System Error	1
C8	PERR#	Parity Error	1
C9	DEVSEL#	Device Select	1
C10	GND	Ground	
C11	AD19	Address 19	
C12	AD22	Address 22	
C13	GND	Ground	
C14	AD25	Address 25	
C15	GND	Ground	
C16	X1	Reserved (1)	
C17	GNT2	Grant 2	
C18	REQ4	Request 4	1
C19	SLEEP#/SDAT	Sleep/Serial Data (I2C)	3
C20	X4	Reserved (4)	
C21	INTD#	Interrupt D	1
C22	INTB#	Interrupt B	1
C23	+5V	+5 VDC	

C24	USB-	Universal Serial Bus (USB)(-)	
D1	AD0	Address 0	
D2	AD4	Address 4	
D3	C/BE0#	Command, Byte Enable 0	
D4	+3,3V	+3.3 VDC	
D5	AD12	Address 12	
D6	AD15	Address 15	
D7	V(I/O)	+3.3 or +5 VDC	
D8	LOCK#	Resource Lock	1
D9	TRDY#	Test Logic Ready	1
D10	AD16	Address 16	
D11	AD20	Address 20	
D12	+5V	+5 VDC	
D13	+5V	+5 VDC	
D14	AD26	Address 26	
D15	AD29	Address 29	
D16	REQ1	Request 1	1
D17	REQ3	Request 3	1
D18	V(I/O)	+3.3 or +5 VDC	
D19	X2	Reserved (2)	
D20	X5	Reserved (5)	
D21	+3,3V	+3.3 VDC	
D22	INTA#	Interrupt A	1
D23	ICPEN#/SCLK	ICPEN/Serial Clock (I2C)	3
D24	OSC (PWDN)		
E1	AD1	Address 1	
E2	AD5	Address 5	
E3	GND	Ground	
E4	M66EN	Enable 66Mhz PCI-bus	
E5	GND	Ground	
E6	C/BE1#	Command, Byte Enable 1	
E7	SBO#	Snoop Backoff	1



E8	+5V	+5 VDC	
E9	IRDY#	Initiator Ready	1
E10	AD17	Address 17	
E11	GND	Ground	
E12	AD23	Address 23	
E13	C/BE3#	Command, Byte Enable 3	
E14	GND	Ground	
E15	AD30	Address 30	
E16	GNT1	Grant 1	
E17	+5V	+5 VDC	
E18	GNT4	Grant 4	
E19	X3	Reserved (3)	
E20	GND	Ground	
E21	INTC#	Interrupt C	1
E22	-12V	-12 VDC	
E23	+12V	+12 VDC	
E24	VBATT		

1 = Pullup resistor of 2,7 kOhm on the System Slot (CPU).

2 = Pullup resistor of 330 ohm on the System Slot (CPU).

3 = Pullup resistor of 4,7 KB ohm, if not supported by the System Slot (CPU).

## Module Bus Slot (Middle)

Pin	Name	Description	Note
A1	+3,3V	+3.3 VDC	
A2	AD2	Address 2	
A3	AD6	Address 6	
A4	GND	Ground	
A5	AD10	Address 10	
A6	AD13	Address 13	
A7	GND	Ground	

A8	SDONE	Snoop Done	1
A9	GND	Ground	
A10	FRAME#	Indicate Address or Data phase	1
A11	AD18	Address 18	
A12	GND	Ground	
A13	+5V	+5 VDC	
A14	AD24	Address 24	
A15	AD27	Address 27	
A16	GND	Ground	
A17	REQ2	Request 2	1
A18	CLKM		
A19	CLK1	33 or 66 MHz Clock	
A20	CLK2		
A21	GND	Ground	
A22	CLK3		
A23	CLK4		
A24	+3,3V	+3.3 VDC	
B1	REQ64#	Request 64 ???	1
B2	AD3	Address 3	
B3	+5V	+5 VDC	
B4	AD8	Address 8	
B5	+3,3V	+3.3 VDC	
B6	AD14	Address 14	
B7	PAR	Parity	
B8	+3,3V	+3.3 VDC	
B9	STOP#	Stop	1
B10	C/BE2#	Command, Byte Enable 2	
B11	V(I/O)	+3.3 or +5 VDC	
B12	AD21	Address 21	
B13	+3,3V	+3.3 VDC	
B14	V(I/O)	+3.3 or +5 VDC	
B15	AD28	Address 28	

B16	AD31	Address 31	
B17	+3,3V	+3.3 VDC	
B18	GNT3	Grant 3	
B19	RST#	Reset	
B20	NMI#	Non Maskable Interrupt	
B21	X6	Reserved (6)	
B22	+5V	+5 VDC	:
B23	RSTIN#		
B24	USB+	Universal Serial Bus (USB)(+)	
C1	ACK64#	Acknowledge 64 ???	1
C2	GND	Ground	
C3	AD7	Address 7	
C4	AD9	Address 9	
C5	AD11	Address 11	
C6	GND	Ground	
C7	SERR#	System Error	1
C8	PERR#	Parity Error	1
C9	DEVSEL#	Device Select	1
C10	GND	Ground	
C11	AD19	Address 19	
C12	AD22	Address 22	
C13	GND	Ground	
C14	AD25	Address 25	
C15	GND	Ground	
C16	X1	Reserved (1)	
C17	GNT2	Grant 2	
C18	REQ4	Request 4	1
C19	SLEEP#/SDAT	Sleep/Serial Data (I2C)	
C20	X4	Reserved (4)	
C21	INTD#	Interrupt D	1
C22	INTB#	Interrupt B	1
C23	+5V	+5 VDC	

C24	USB-	Universal Serial Bus (USB)(-)	
D1	AD0	Address 0	
D2	AD4	Address 4	
D3	C/BE0#	Command, Byte Enable 0	
D4	+3,3V	+3.3 VDC	
D5	AD12	Address 12	
D6	AD15	Address 15	
D7	V(I/O)	+3.3 or +5 VDC	
D8	LOCK#	Resource Lock	1
D9	TRDY#	Test Logic Ready	1
D10	AD16	Address 16	
D11	AD20	Address 20	
D12	+5V	+5 VDC	
D13	+5V	+5 VDC	
D14	AD26	Address 26	
D15	AD29	Address 29	
D16	REQ1	Request 1	1
D17	REQ3	Request 3	1
D18	V(I/O)	+3.3 or +5 VDC	
D19	X2	Reserved (2)	
D20	X5	Reserved (5)	
D21	+3,3V	+3.3 VDC	
D22	INTA#	Interrupt A	1
D23	ICPEN#/SCLK	ICPEN/Serial Clock (I2C)	3
D24	OSC (PWDN)		
E1	AD1	Address 1	
E2	AD5	Address 5	
E3	GND	Ground	
E4	M66EN	Enable 66Mhz PCI-bus	
E5	GND	Ground	
E6	C/BE1#	Command, Byte Enable 1	
E7	SBO#	Snoop Backoff	1



E8	+5V	+5 VDC	
E9	IRDY#	Initiator Ready	1
E10	AD17	Address 17	
E11	GND	Ground	
E12	AD23	Address 23	
E13	C/BE3#	Command, Byte Enable 3	
E14	GND	Ground	
E15	AD30	Address 30	
E16	GNT1	Grant 1	
E17	+5V	+5 VDC	
E18	GNT4	Grant 4	
E19	X3	Reserved (3)	
E20	GND	Ground	
E21	INTC#	Interrupt C	1
E22	-12V	-12 VDC	
E23	+12V	+12 VDC	
E24	VBATT		

1 = Pullup resistor of 2,7 kOhm on the System Slot (CPU).

## Card Slot (Middle)

Pin	Name	Description	Note
A1	+3,3V	+3.3 VDC	
A2	AD2	Address 2	
A3	AD6	Address 6	
A4	GND	Ground	
A5	AD10	Address 10	
A6	AD13	Address 13	
A7	GND	Ground	
A8	SDONE	Snoop Done	1
A9	GND	Ground	

A10	FRAME#	Indicate Address or Data phase	1
A11	AD18	Address 18	
A12	GND	Ground	
A13	+5V	+5 VDC	
A14	AD24	Address 24	
A15	AD27	Address 27	
A16	GND	Ground	
A17	IDSEL0	IDSEL0	1
A18	GND	Ground	
A19	CLK1	33 or 66 MHz Clock	
A20	GND	Ground	
A21	GND	Ground	
A22	GND	Ground	
A23	GND	Ground	
A24	+3,3V	+3.3 VDC	
B1	REQ64#	Request 64 ???	1
B2	AD3	Address 3	
B3	+5V	+5 VDC	
B4	AD8	Address 8	
B5	+3,3V	+3.3 VDC	
B6	AD14	Address 14	
B7	PAR	Parity	
B8	+3,3V	+3.3 VDC	
B9	STOP#	Stop	1
B10	C/BE2#	Command, Byte Enable 2	
B11	V(I/O)	+3.3 or +5 VDC	
B12	AD21	Address 21	
B13	+3,3V	+3.3 VDC	
B14	V(I/O)	+3.3 or +5 VDC	
B15	AD28	Address 28	
B16	AD31	Address 31	
B17	+3,3V	+3.3 VDC	

B18	GND	Ground	
B19	RST#	Reset	
B20	NMI#	Non Maskable Interrupt	
B21	X6	Reserved (6)	
B22	+5V	+5 VDC	:
B23	RSTIN#		
B24	USB+	Universal Serial Bus (USB)(+)	
C1	ACK64#	Acknowledge 64 ???	1
C2	GND	Ground	
C3	AD7	Address 7	
C4	AD9	Address 9	
C5	AD11	Address 11	
C6	GND	Ground	
C7	SERR#	System Error	1
C8	PERR#	Parity Error	1
C9	DEVSEL#	Device Select	1
C10	GND	Ground	
C11	AD19	Address 19	
C12	AD22	Address 22	
C13	GND	Ground	
C14	AD25	Address 25	
C15	GND	Ground	
C16	X1	Reserved (1)	
C17	IDSEL1	Initialization Device Select 1	
C18	GND	Ground	
C19	SLEEP#/SDAT	Sleep/Serial Data (I2C)	
C20	X4	Reserved (4)	
C21	INTD#	Interrupt D	1
C22	INTB#	Interrupt B	1
C23	+5V	+5 VDC	
C24	USB-	Universal Serial Bus (USB)(-)	
D1	AD0	Address 0	

D2	AD4	Address 4	
D3	C/BE0#	Command, Byte Enable 0	
D4	+3,3V	+3.3 VDC	
D5	AD12	Address 12	
D6	AD15	Address 15	
D7	V(I/O)	+3.3 or +5 VDC	
D8	LOCK#	Resource Lock	1
D9	TRDY#	Test Logic Ready	1
D10	AD16	Address 16	
D11	AD20	Address 20	
D12	+5V	+5 VDC	
D13	+5V	+5 VDC	
D14	AD26	Address 26	
D15	AD29	Address 29	
D16	REQ1	Request 1	1
D17	IDSEL2	Initialization Device Select 2	
D18	V(I/O)	+3.3 or +5 VDC	
D19	X2	Reserved (2)	
D20	X5	Reserved (5)	
D21	+3,3V	+3.3 VDC	
D22	INTA#	Interrupt A	1
D23	ICPEN#/SCLK	ICPEN/Serial Clock (I2C)	3
D24	OSC (PWDN)		
E1	AD1	Address 1	
E2	AD5	Address 5	
E3	GND	Ground	
E4	M66EN	Enable 66Mhz PCI-bus	
E5	GND	Ground	
E6	C/BE1#	Command, Byte Enable 1	
E7	SBO#	Snoop Backoff	1
E8	+5V	+5 VDC	
E9	IRDY#	Initiator Ready	1



E10	AD17	Address 17	
E11	GND	Ground	
E12	AD23	Address 23	
E13	C/BE3#	Command, Byte Enable 3	
E14	GND	Ground	
E15	AD30	Address 30	
E16	GNT1	Grant 1	
E17	+5V	+5 VDC	
E18	GNT4	Grant 4	
E19	X3	Reserved (3)	
E20	GND	Ground	
E21	INTC#	Interrupt C	1
E22	-12V	-12 VDC	
E23	+12V	+12 VDC	
E24	VBATT		

1 = Pullup resistor of 2,7 kOhm on the System Slot (CPU).

## 64-bit PCI (Top)

Pin	Name	Description	Note
A1	GND	Ground	
A2	X10	Reserved (10)	
A3	AD35	Address 35	2
A4	AD38	Address 38	2
A5	AD42	Address 42	2
A6	V(I/O)	+3.3 or +5 VDC	
A7	V(I/O)	+3.3 or +5 VDC	
A8	AD52	Address 52	2
A9	AD56	Address 56	2
A10	AD60	Address 60	2
A11	AD63	Address 63	2

A12	GND	Ground	
B1	X7	Reserved (7)	
B2	GND	Ground	
B3	AD36	Address 36	2
B4	AD39	Address 39	2
B5	AD43	Address 43	2
B6	AD46	Address 46	2
B7	AD49	Address 49	2
B8	AD53	Address 53	2
B9	AD57	Address 57	2
B10	AD61	Address 61	2
B11	GND	Ground	
B12	C/BE6#	Command, Byte Enable 6	2
C1	X8	Reserved (8)	
C2	AD32	Address 32	2
C3	GND	Ground	
C4	AD40	Address 40	2
C5	AD44	Address 44	2
C6	GND	Ground	
C7	GND	Ground	
C8	AD54	Address 54	2
C9	AD58	Address 58	2
C10	GND	Ground	
C11	PAR64	Parity 64 ???	2
C12	C/BE7#	Command, Byte Enable 7	2
D1	X9	Reserved (9)	
D2	AD33	Address 33	2
D3	AD37	Address 37	2
D4	GND	Ground	
D5	AD45	Address 45	2
D6	AD47	Address 47	2
D7	AD50	Address 50	2

D8	AD55	Address 55	2
D9	GND	Ground	
D10	AD62	Address 62	2
D11	C/BE4#	Command, Byte Enable 4	2
D12	X11	Reserved (11)	
E1	GND	Ground	
E2	AD34	Address 34	2
E3	V(I/O)	+3.3 or +5 VDC	
E4	AD41	Address 41	2
E5	GND	Ground	
E6	AD48	Address 48	2
E7	AD51	Address 51	2
E8	GND	Ground	
E9	AD59	Address 59	2
E10	V(I/O)	+3.3 or +5 VDC	
E11	C/BE5#	Command, Byte Enable 5	2
E12	X12	Reserved (12)	

2 = Pullup resistor of 2,7 kOhm (5V bus system) or 8,2 kOhm (3,3V bus system) on the backplane.

## ISA96/AT96 (Bottom)

Pin	Name	Description	Note
A1	RSTDRV		
A2	IRQ9	Interrupt 9	
A3	SD11	Data 11	
A4	SD9	Data 9	
A5	IOCHRDY		1
A6	IOW#	I/O Write	
A7	SA15	Address 15	
A8	CLK	Clock	
A9	SA10	Address 10	

A10	SA7	Address 7	
A11	T/C		
A12	SA2	Address 2	
B1	SD15	Data 15	
B2	SD13	Data 13	
B3	SD3	Data 3	
B4	SD1	Data 1	
B5	SMEMW#	System Memory Write	
B6	SA18	Address 18	
B7	SA14	Address 14	
B8	DACK6#	DMA Acknowledge 6	
B9	SA9	Address 9	
B10	IRQ3	Interrupt 3	
B11	IOCS16#	I/O 16-bit chip select	1
B12	SA1	Address 1	
C1	SD7	Data 7	
C2	SD5	Data 5	
C3	SD10	Data 10	
C4	SD8	Data 8	
C5	AEN	Address Enable	
C6	IOR#	I/O Read	
C7	SA13	Address 13	
C8	SA11	Address 11	
C9	IRQ5	Interrupt 5	
C10	SA6	Address 6	
C11	SA4	Address 4	
C12	IRQ11	Interrupt 11	
D1	SD14	Data 14	
D2	SD12	Data 12	
D3	SD2	Data 2	
D4	SD0	Data 0	
D5	SMEMR#	System Memory Read	



D6	SA17	Address 17	
D7	REF#		
D8	IRQ7	Interrupt 7	
D9	SA8	Address 8	
D10	MCS16#		1
D11	BALE		
D12	SA0	Address 0	
E1	SD6	Data 6	
E2	SD4	Data 4	
E3	OWS		1
E4	SBHE#		
E5	SA19	Address 19	
E6	SA16	Address 16	
E7	SA12	Address 12	
E8	DRQ6	DMA Request 6	
E9	IRQ4	Interrupt 4	
E10	SA5	Address 5	
E11	SA3	Address 3	
E12	IRQ10	Interrupt 10	

1 = Pullup resistor must be integrated into the System Slot (CPU).

## VMEbus (Bottom)

Pin	Name	Description
A1	D0	Data 0
A2	D2	Data 2
A3	D12	Data 12
A4	D7	Data 7
A5	DS1#	
A6	BR3#	
A7	AM1	

A8	AM3	
A9	IACKOUT#	
A10	A14	Address 14
A11	A12	Address 12
A12	A10	Address 10
B1	BBSY#	
B2	D10	Data 10
B3	D5	Data 5
B4	D15	Data 15
B5	SYSRES#	
B6	A23	Address 23
B7	A21	Address 21
B8	A19	Address 19
B9	A16	Address 16
B10	A6	Address 6
B11	A4	Address 4
B12	A2	Address 2
C1	D8	Data 8
C2	D3	Data 3
C3	D13	Data 13
C4	SYSCLK	
C5	DS0#	
C6	DTACK#	
C7	AS#	
C8	IACK#	
C9	AM4	
C10	A13	Address 13
C11	A11	Address 11
C12	A9	Address 9
D1	D1	Data 1
D2	D11	Data 11
D3	D6	Data 6

D4	BG3OUT#	
D5	WR#	Write
D6	AM0	
D7	AM2	
D8	A18	Address 18
D9	A15	Address 15
D10	A5	Address 5
D11	A3	Address 3
D12	A1	Address 1
E1	D9	Data 9
E2	D4	Data 4
E3	D14	Data 14
E4	BERR#	Bus Error
E5	AM5	
E6	A22	Address 22
E7	A20	Address 20
E8	A17	Address 17
E9	A7	Address 7
E10	IRQ5#	Interrupt 5
E11	IRQ3#	Interrupt 3
E12	A8	Address 8

## ECB (Bottom)

Pin	Name	Description
A1	D5	Data 5
A2	D2	Data 2
A3	A4	Data 4
A4	A7	Address 7
A5	BAI	
A6	2F	

A7	A10	Address 10
A8	INT#	
A9	VCMOS	
A10	PWRCLR#	
A11	A13	Address 13
A12	RESET#	Reset
B1	D0	Data 0
B2	D4	Data 4
B3	A1	Address 1
B4	WAIT#	
B5	A17	Address 17
B6	IEO	
B7	n/c	Not connected
B8	DMARDY	
B9	RD#	Read
B10	IORQ#	
B11	?	
B12	n/c	Not connected
C1	D6	Data 6
C2	A0	Address 0
C3	A5	Address 5
C4	A16	Address 16
C5	A18	Address 18
C6	BAO	
C7	M1#	
C8	WR#	
C9	n	
C10	A12	Address 12
C11	A9	Address 9
C12	n/c	Not connected
D1	D7	Data 7
D2	A2	Address 2



D3	A8	Address 8
D4	BUSRQ#	
D5	A19	Address 19
D6	A11	Address 11
D7	NMI#	Non Maskable Interrupt
D8	PF	
D9	HALT#	
D10	RFSH#	
D11	MRQ#	
D12	n/c	Not connected
E1	D3	Data 3
E2	A3	Address 3
E3	A6	Address 6
E4	IEI	
E5	D1	Data 1
E6	A14	Address 14
E7	n/c	Not connected
E8	n/c	Not connected
E9	DESLCT#	
E10	A15	Address 15
E11	BUSAK#	
E12	n/c	Not connected

## SMP16 (Bottom)

Pin	Name	Description
A1	NMI#	Non Maskable Interrupt
A2	IRQ0#	Interrupt 0
A3	D11	Data 11
A4	D9	Data 9
A5	RDYIN	

A6	IOW#	
A7	A15	Address 15
A8	CLK	
A9	A10	Address 10
A10	A7	Address 7
A11	TC/EOP#	
A12	A2	Address 2
B1	D15	Data 15
B2	D13	Data 13
B3	D3	Data 3
B4	D1	Data 1
B5	MEMW#	
B6	A18	Address 18
B7	A14	Address 14
B8	DACKx#	
B9	A9	Address 9
B10	IRQ3#	Interrupt 3
B11	IOCS16#	
B12	A1	Address 1
C1	D7	Data 7
C2	D5	Data 5
C3	D10	Data 10
C4	D8	Data 8
C5	BUSEN	
C6	IOR#	
C7	A13	Address 13
C8	A11	Address 11
C9	IRQ1#	Interrupt 1
C10	A6	Address 6
C11	A4	Address 4
C12	IRQ4#	Interrupt 4
D1	D14	Data 14

D2	D12	Data 12
D3	D2	Data 2
D4	D0	Data 0
D5	MEMR#	
D6	A17	Address 17
D7	INTA#	
D8	INT#	
D9	A8	Address 8
D10	MECS16#	
D11	ALE	
D12	A0	Address 0
E1	D6	Data 6
E2	D4	Data 4
E3	MMIO#	
E4	BHEN	
E5	A19	Address 19
E6	A16	Address 16
E7	A12	Address 12
E8	DRQx#	
E9	IRQ2#	Interrupt 2
E10	A5	Address 5
E11	A3	Address 3
E12	IRQ5#	Interrupt 5

## Floppy/EIDE (Bottom)

Pin	Name	Description
A1	FDSEL1	Floppy Select 1
A2	FDSEL0	Floppy Select 0
A3	FDME1	Floppy ?
A4	DIR	Floppy Direction

A5	STEP	Floppy Step
A6	WRDATA	Floppy Write Data
A7	WE	Floppy Write?
A8	TRK0	Floppy Track 0
A9	WP	Floppy Write?
A10	RDDATA	Floppy ?
A11	HDSEL	Floppy HD Select
A12	DSKCHG	Floppy DiskChange
B1	DRV DEN1	?
B2	DRV DEN0	?
B3	IDECS3P#	IDE ?
B4	IDEA2	IDE ?
B5	IDEIRQS	IDE ?
B6	IDEPUS	IDE ?
B7	IDEDRQP	IDE ?
B8	IDED14	IDE Data 14
B9	IDED8	IDE Data 8
B10	IDED6	IDE Data 6
B11	IDED11	IDE Data 11
B12	IDED3	IDE Data 3
C1	FDME0	Floppy Me?
C2	INDX	Floppy Index
C3	IDECS3S#	IDE ?
C4	IDEA0	IDE ?
C5	IDEDAKS#	IDE ?
C6	IDEIOR#	IDE ?
C7	IDEDRQS	IDE ?
C8	IDED1	IDE Data 1
C9	#IDERST	IDE ?
C10	IDED10	IDE Data 10
C11	IDED4	IDE Data 4
C12	IDED2	IDE Data 2



D1	IDELEDS#	IDE LED ?
D2	IDELEDP#	IDE LED ?
D3	IDECS1S#	IDE ?
D4	IDEIRQP	IDE ?
D5	IDEPUUP	IDE Pull Up ?
D6	IDEIOW#	IDE ?
D7	IDED15	IDE Data 15
D8	IDED13	IDE Data 13
D9	IDED7	IDE Data 7
D10	GND	Ground
D11	GND	Ground
D12	GND	Ground
E1	GND	Ground
E2	GND	Ground
E3	IDECS1P#	IDE ?
E4	IDEA1	IDE ?
E5	IDEDAKP#	IDE ?
E6	IDEIORDY	IDE ?
E7	IDED0	IDE Data 0
E8	IDED12	IDE Data 12
E9	IDED9	IDE Data 9
E10	IDED5	IDE Data 5
E11	GND	Ground
E12	GND	Ground

## SCSI (Bottom)

Pin	Name	Description
A1	TERM	
A2	GND	Ground
A3	I/O#	

A4	REQ#	
A5	ATN#	
A6	D8	Data 8
A7	D9	Data 9
A8	D10	Data 10
A9	D2	Data 2
A10	D4	Data 4
A11	DP0	
A12	GND	Ground
B1	TERM	
B2	GND	Ground
B3	GND	Ground
B4	GND	Ground
B5	GND	Ground
B6	GND	Ground
B7	GND	Ground
B8	GND	Ground
B9	GND	Ground
B10	GND	Ground
B11	GND	Ground
B12	GND	Ground
C1	TERM	
C2	GND	Ground
C3	C/D#	
C4	MSG#	
C5	ACK#	
C6	D12	Data 12
C7	DP1	Data P1
C8	D13	Data 13
C9	D1	Data 1
C10	D5	Data 5
C11	D7	Data 7

C12	GND	Ground
D1	TERM	
D2	GND	Ground
D3	GND	Ground
D4	GND	Ground
D5	GND	Ground
D6	GND	Ground
D7	GND	Ground
D8	GND	Ground
D9	GND	Ground
D10	GND	Ground
D11	GND	Ground
D12	GND	Ground
E1	TERM	
E2	GND	Ground
E3	SEL#	
E4	RST#	
E5	BSY#	
E6	D14	Data 14
E7	D15	Data 15
E8	D11	Data 11
E9	D0	Data 0
E10	D3	Data 3
E11	D6	Data 6
E12	GND	Ground

Contributor: [Joakim Ögren](#), [Rob Gill](#)

Source:

[IndustrialPCI page](#) at [Standard Industrial PC Systems's \(SIPS\) homepage](#)

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# JAMMA

JAMMA=Japanese Arcade Machine Manufacturers Association

An old group trying to set standards for board pinouts (at arcade machines). This was designed to make board changes easy, just take out the old game and plug in the new. Unfortunately games have evolved, and the Jamma standard is no longer up to the job as it can't handle more than 4 buttons or two players. Also replacing a board from a different manufacturer meant readjusting the picture on the monitor as it would not be centred in the same position.

28 PIN UNKNOWN CONNECTOR on the arcade machine

## Sold side

Pin	Description
A	Ground
B	Ground
C	+5V
D	+5V
E	-5V
F	+12V
H	Key (no connection)
J	Meter 2
K	Lockout 2
L	Speaker -
M	Audio Ground
N	Video Green
P	Video Sync
R	Service Switch
S	Tilt Switch "Pinball Slam"



T	Coin 2
U	2 Player start
V	Player 2 Up
W	Player 2 Down
X	Player 2 Left
Y	Player 2 Right
Z	Player 2 Button 1
Aa	Player 2 Button 2
Ab	Player 2 Button 3
Ac	(Player 2 Button 4)
Ad	Not used
Ae	Ground
Af	Ground

## Component side

Pin	Description
1	Ground
2	Ground
3	+5V
4	+5V
5	-5V
6	+12V
7	Key (no connection)
8	Meter 1
9	Lockout 1
10	Speaker +
11	Audio +
12	Video Red
13	Video Blue
14	Video Ground

15	Test Switch
16	Coin 1
17	1 Player start
18	Player 1 Up
19	Player 1 Down
20	Player 1 Left
21	Player 1 Right
22	Player 1 Button 1
23	Player 1 Button 2
24	Player 1 Button 3
25	(Player 1 Button 4)
26	Not used
27	Ground
28	Ground

*Note: All signals are active low.*

*Contributor:* [Joakim Ögren](#)

*Source:*  
*JAMMA pinout at* [Technick.net](#)

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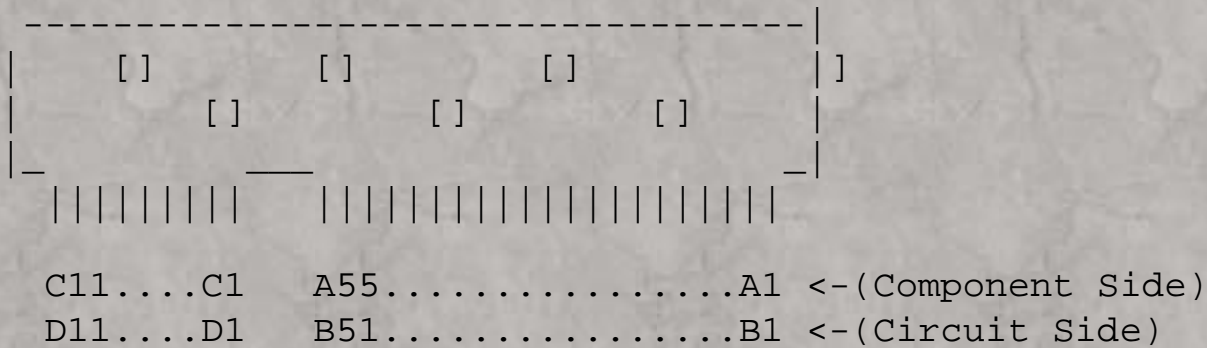


# MCA

MCA=

62+36 PIN EDGE CONNECTOR MALE at the card.

62+36 PIN EDGE CONNECTOR FEMALE at the computer.



Pin	Name
A1	VSYNC
A2	HSYNC
A3	BLANC
A4	GND
A5	P6
A6	EDCLK
A7	DCLK
A8	GND
A9	P7
A10	EVIDEO
A11	CD/SETUP
A12	MADE24
A13	GND
A14	A11
A15	A10

A16	A9
A17	+5V
A18	A8
A19	A7
A20	A6
A21	+5V
A22	A5
A23	A4
A24	A3
A25	+5V
A26	A2
A27	A1
A28	A0
A29	+12V
A30	ADL
A31	PREEMPT
A32	BURST
A33	-12V
A34	ARB0
A35	ARB1
A36	ARB2
A37	-12V
A38	ARB3
A39	ARB/GNT
A40	TC
A41	+5V
A42	S0
A43	S1
A44	M/IO
A45	+12V
A46	CD CHRDY
A47	D0



A48	D2
A49	+5V
A50	D5
A51	D6
A52	D7
A53	GND
A54	DS 16 RIN
A55	REFRESH
B1	ESYNC
B2	GND
B3	P5
B4	P4
B5	P3
B6	GND
B7	P2
B8	P1
B9	P0
B10	GND
B11	Audio/GND
B12	Audio
B13	GND
B14	Oscillator
B15	GND
B16	A23
B17	A22
B18	A21
B19	GND
B20	A20
B21	A19
B22	A18
B23	GND
B24	A17

B25	A16
B26	A15
B27	GND
B28	A14
B29	A13
B30	A12
B31	GND
B32	IRQ9
B33	IRQ3
B34	IRQ4
B35	GND
B36	IRQ5
B37	IRQ6
B38	IRQ7
B39	GND
B40	Reserved
B41	Reserved
B42	CHCK
B43	GND
B44	CMD
B45	CHROYRTN
B46	CD SFDBK
B47	GND
B48	D1
B49	D3
B50	D4
B51	GND
B52	CHRESET
B53	Reserved
B54	Reserved
B55	GND
C1	+5V

C2	D10
C3	D11
C4	D13
C5	+12V
C6	Reserved
C7	SBHE
C8	CD DS 16
C9	+5V
C10	IRQ14
C11	IRQ15
D1	D8
D2	D9
D3	GND
D4	D12
D5	D14
D6	D15
D7	GND
D8	IORQ10
D9	IORQ11
D10	IORQ12
D11	GND

Contributor: [Joakim Ögren](#), [Rob Gill](#)

Source:  
[MCA pinout](#) at [The Pin-Out directory](#)

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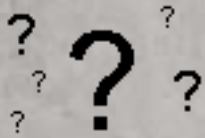
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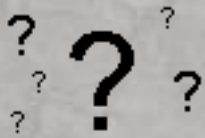
# Miniature Card

Developed by Intel.

Miniature Card is a memory-only expansion card.



(at the device)


































(at the card)













UNKNOWN CONNECTOR at the device.

UNKNOWN CONNECTOR at the card.


Pin	Name	Description	Dir
1	A18	Address Bus	←
2	A16	Address Bus	←
3	A14	Address Bus	←
4	Vccr	Voltage Refresh	←
5	CEH#	Card Enable High Byte	←
6	A11	Address Bus	←
7	A9	Address Bus	←
8	A8	Address Bus	←
9	A6	Address Bus	←
10	A5	Address Bus	←
11	A3	Address Bus	←
12	A2	Address Bus	←
13	A0	Address Bus	←
14	RAS#	Row Address Strobe	←



15	A24	Address Bus	
16	A23	Address Bus	
17	A22	Address Bus	
18	OE#	Output Enable	
19	D15	Data Bus	
20	D13	Data Bus	
21	D12	Data Bus	
22	D10	Data Bus	
23	D9	Data Bus	
24	D0	Data Bus	
25	D2	Data Bus	
26	D4	Data Bus	
27	RFU	Reserved for future use	
28	D7	Data Bus	
29	SDA	Serial Data and Address	
30	SCL	Serial Clock	
31	A19	Address Bus	
32	A17	Address Bus	
33	A15	Address Bus	
34	A13	Address Bus	
35	A12	Address Bus	
36	RESET#	Reset	
37	A10	Address Bus	
38	VS1#	Voltage Sense 1	
39	A7	Address Bus	
40	BS8#	Bus Size 8	
41	A4	Address Bus	
42	CEL#	Card Enable Low Byte	
43	A1	Address Bus	
44	CASL#	Column Address Strobe Low Byte	
45	CASH#	Column Address Strobe High Byte	
46	CD#	Card Detect	

47	A21	Address Bus	
48	BUSY#	Ready/Busy	
49	WE#	Write Enable	
50	D14	Data Bus	
51	RFU	Reserved for future use	
52	D11	Data Bus	
53	VS2#	Voltage Sense 2	
54	D8	Data Bus	
55	D1	Data Bus	
56	D3	Data Bus	
57	D5	Data Bus	
58	D6	Data Bus	
59	RFU	Reserved for future use	
60	A20	Address Bus	

The following three is separate:

Name	Description	Dir
GND	Ground	
VCC	Power	
CINS#	Card Insertion	

*Note: Direction is card relative device.*

Contributor: [Joakim Ögren](#)

Source:

*Minicature Card v1.1 spec at Miniature Card Implementers Forum's homepage*

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# Miniature Card (technical)

This section is currently based solely on the Miniature Card specification v1.1.

## Signal Descriptions:

### A0-A24

Address A0 to A24 are the address bus lines that can address up to 32 Mwords (64 MBytes). The Miniature Card specification does not require the Miniature Card to decode the upper address lines. A 2 Mbyte Miniature Card that does not decode the upper address lines would repeat its address space every 2 Mbytes. Address 0h would access the same physical location as 200000h, 400000h, 600000h, etc.

### D0-D15

Data lines D0 through D15 constitute the data bus. The data bus is composed of two bytes, the low byte D[7:0] and the high byte D[15:8].

### OE#

OE# indicates that the current bus cycle is a read cycle.

### WE#

WE# indicates that the current bus cycle is a write cycle.

### VS1#

Voltage Sense 1 signal. The card grounds this signal to indicate it can operate at 3.3 Volts. This signal must either be connected to card GND or left open.

### VS2#

Voltage Sense 2 signal. The card grounds this signal to indicate it can operate at x.x Volts (the value to

be determined at a later date). This signal must either be connected to card GND or left open.

## **CEL#**

CEL# enables the low byte of the data bus (D[7:0]) on the card. This signal is not used in DRAM cards.

## **CEH#**

CEH# enables the high byte of the data bus (D[15:8]) on the card. This signal is not used in DRAM cards.

## **RAS#**

RAS# strobes in the row address for DRAM cards.

## **CASL#**

CASL# strobes in the low byte column address for DRAM cards.

## **CASH#**

CASH# strobes in the high byte column address for DRAM cards.

## **RESET#**

RESET# controls card initialization. When RESET# transitions from a low state to a high state, the Miniature Card must reset to a predetermined state.

## **BUSY#**

BUSY# is a signal generated by the card to indicate the status of operations within the Miniature Card. When BUSY# is high, the Miniature Card is ready to accept the next command from the host. When BUSY# is low, the Miniature Card is busy and unable to accept some data operations from the host. For example, in Flash Miniature Cards the BUSY# signal is tied to the components RY/BY# signal. However, ROM Miniature Cards would always drive BUSY# high since the host will always be able to read from a ROM Miniature Card.

## **Vccr**



Vccr provides a low current (refresh) voltage supply. Vccr is a feature used by DRAM Miniature Cards to "self-refresh" during "sleep" mode.

## SDA

I<sup>2</sup>C: Serial Data/Address.

## SCL

I<sup>2</sup>C: Serial Clock are used to read the attribute information structure (AIS) from the serial EEPROM in a DRAM card.

## CD#

CD# is a grounded interface signal. After a Miniature Card has been inserted, CD# will be forced low. The card detect signal is located in the center of the second row of interface signals, and should be one of the last interface signals to connect to the host. Do not confuse CD# with CINS#. CINS# is an early card detect that is one of the first signals to connect to the host.

## BS8#

BS8# is a signal driven by the host to indicate if the data bus is x8 or x16. An 8-bit host must drive BS8# low and tie the high byte data bus D[15:8] to the low byte data bus D[7:0]. A 16-bit host must drive this signal high.

## GND

Ground

## Vcc

Vcc is used to supply power to the card.

## CINS#

CINS# is a grounded signal on the front of the Miniature Card that can be used for early detection of a card insertion. CINS# makes contact on the host when the front of the card is inserted into the socket, before the interface signals connect.

Contributor: [Joakim Ögren](#)

Source:

*Minicature Card v1.1 spec at Miniature Card Implementers Forum's homepage*

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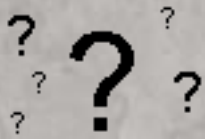


# NuBus

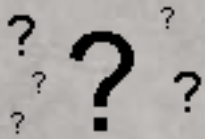
Available on old Apple Macintosh computers and on NeXT computers.

Standard: IEEE 1196, "Nubus-A simple 32-bit backplane bus".

Texas Instruments owns the standard today.



(at the card)



(at the computer)

UNKNOWN CONNECTOR at the card.

UNKNOWN CONNECTOR at the computer.

## Row A

Pin	Name	Description
1	-12 V	-12 VDC
2	-	
3	/SPV	
4	/SP	
5	/TM1	
6	/AD1	Address/Data 1
7	/AD3	Address/Data 3
8	/AD5	Address/Data 5
9	/AD7	Address/Data 7
10	/AD9	Address/Data 9
11	/AD11	Address/Data 11

12	/AD13	Address/Data 13
13	/AD15	Address/Data 15
14	/AD17	Address/Data 17
15	/AD19	Address/Data 19
16	/AD21	Address/Data 21
17	/AD23	Address/Data 23
18	/AD25	Address/Data 25
19	/AD27	Address/Data 27
20	/AD29	Address/Data 29
21	/AD31	Address/Data 31
22	GND	Ground
23	GND	Ground
24	/ARB1	
25	/ARB3	
26	/ID1	
27	/ID3	
28	/ACK	
29	+5 V	+5 VDC
30	/RQST	
31	/NMRQ	
32	+12 V	+12 VDC

## Row B

Pin	Name	Description
1	-12 V	-12 VDC
2	GND	Ground
3	GND	Ground
4	+5 V	+5 VDC
5	+5 V	+5 VDC
6	+5 V	+5 VDC



7	+5 V	+5 VDC
8	*	Reserved ?
9	*	Reserved ?
10	*	Reserved ?
11	*	Reserved ?
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	**	Reserved ?
25	**	Reserved ?
26	**	Reserved ?
27	**	Reserved ?
28	+5 V	+5 VDC
29	+5 V	+5 VDC
30	GND	Ground
31	GND	Ground
32	+12 V	

## Row C

Pin	Name	Description
1	/RESET	Reset

2	-	
3	+5 V	+5 VDC
4	+5 V	+5 VDC
5	/TM0	
6	/AD0	Address/Data 0
7	/AD2	Address/Data 2
8	/AD4	Address/Data 4
9	/AD6	Address/Data 6
10	/AD8	Address/Data 8
11	/AD10	Address/Data 10
12	/AD12	Address/Data 12
13	/AD14	Address/Data 14
14	/AD16	Address/Data 16
15	/AD18	Address/Data 18
16	/AD20	Address/Data 20
17	/AD22	Address/Data 22
18	/AD24	Address/Data 24
19	/AD26	Address/Data 26
20	/AD28	Address/Data 28
21	/AD30	Address/Data 30
22	GND	Ground
23	/PFW	
24	/ARB0	
25	/ARB2	
26	/ID0	
27	/ID2	
28	/START	
29	+5 V	+5 VDC
30	+5 V	+5 VDC
31	GND	Ground
32	/CLK	Clock

## **+5V**

Power to slot; 2 amps per slot maximum continuous.

## **+12V**

Power to slot; 0.25 amps per slot maximum continuous.

## **-12V**

Power to slot; 0.1 amps per slot maximum continuous.

## **-5.2V**

Unused

## **GND**

Power return for +5V, +12V, and -12V

## **RESET**

Open collector signal; card should use to reset circuitry.

## **SPV**

Slot Parity Valid; asserted if card provides parity. Never asserted under Apple NuBus.

## **SP**

Slot Parity; odd parity of AD0-AD3 if SPV asserted.

## **TM0 - TM1**

Transaction modifiers.

## **AD<31:0>**

Address/Data bits 31 to 0.

## **PFW**

Power Fail Warning given 2ms before AC power is lost.

## **ARB<3:0>**

Arbitration bits 3 to 0; arbitrates system mastership.

## **ID<3:0>**

Geographical address 3 to 0; hard-coded to slot.

## **START**

Asserted to indicate an address on AD lines.

## **ACK**

Acknowledge of START cycle.

## **RQST**

Request; asserted to request bus mastership.

## **NMRQ**

Non-master request; used to signal an interrupt.

## **CLK**



Clock. Asymmetrical 10MHz clock; synchronous transactions on NuBus.

*Contributor:* [Joakim Ögren](#), [Karsten Wenke](#), [Michael Van den Acker](#), [Godel?](#)

*Source:*

[Apple Tech Info Library 2194: Macintosh II NuBus Slots, Pinout](#) at [Apple TIL homepage](#)

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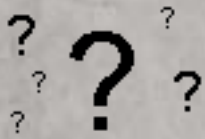
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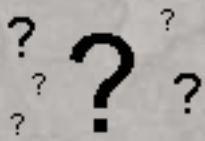


# NuBus 90

Available on old Apple Macintosh computers.



(at the card)



(at the computer)

UNKNOWN CONNECTOR at the card.

UNKNOWN CONNECTOR at the computer.

## Row A

Pin	Name	Description
1	-12 V	-12 VDC
2	SB0	
3	/SPV	
4	/SP	
5	/TM1	
6	/AD1	Address/Data 1
7	/AD3	Address/Data 3
8	/AD5	Address/Data 5
9	/AD7	Address/Data 7
10	/AD9	Address/Data 9
11	/AD11	Address/Data 11
12	/AD13	Address/Data 13

13	/AD15	Address/Data 15
14	/AD17	Address/Data 17
15	/AD19	Address/Data 19
16	/AD21	Address/Data 21
17	/AD23	Address/Data 23
18	/AD25	Address/Data 25
19	/AD27	Address/Data 27
20	/AD29	Address/Data 29
21	/AD31	Address/Data 31
22	GND	Ground
23	GND	Ground
24	/ARB1	
25	/ARB3	
26	/ID1	
27	/ID3	
28	/ACK	
29	+5 V	+5 VDC
30	/RQST	
31	/NMRQ	
32	+12 V	+12 VDC

## Row B

Pin	Name	Description
1	-12 V	-12 VDC
2	GND	Ground
3	GND	Ground
4	+5 V	+5 VDC
5	+5 V	+5 VDC
6	+5 V	+5 VDC
7	+5 V	+5 VDC

8	/TM2	
9	/CM0	
10	/CM1	
11	/CM2	
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	/CLK2X	
25	STDBYPWR	
26	/CLK2XEN	
27	/CBUSY	
28	+5 V	+5 VDC
29	+5 V	+5 VDC
30	GND	Ground
31	GND	Ground
32	+12 V	+12 VDC

## Row C

Pin	Name	Description
1	/RESET	Reset
2	SB1	



3	+5 V	+5 VDC
4	+5 V	+5 VDC
5	/TM0	
6	/AD0	Address/Data 0
7	/AD2	Address/Data 2
8	/AD4	Address/Data 4
9	/AD6	Address/Data 6
10	/AD8	Address/Data 8
11	/AD10	Address/Data 10
12	/AD12	Address/Data 12
13	/AD14	Address/Data 14
14	/AD16	Address/Data 16
15	/AD18	Address/Data 18
16	/AD20	Address/Data 20
17	/AD22	Address/Data 22
18	/AD24	Address/Data 24
19	/AD26	Address/Data 26
20	/AD28	Address/Data 28
21	/AD30	Address/Data 30
22	GND	Ground
23	/PFW	
24	/ARB0	
25	/ARB2	
26	/ID0	
27	/ID2	
28	/START	
29	+5 V	+5 VDC
30	+5 V	+5 VDC
31	GND	Ground
32	/CLK	Clock

Contributor: [Joakim Ögren](#), [Karsten Wenke](#)

*Source:*

*?*

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# PC Card

16-bit bus defined by PCMCIA.

**NOT  
DRAWN  
YET...**



(at the controller)

**NOT  
DRAWN  
YET...**



(at the peripherals)

68 PIN ??? MALE at the controller.

68 PIN ??? FEMALE at the peripherals.

Pin	Memory	I/O+Mem	Description
1	GND	GND	Ground
2	D3	D3	Data 3
3	D4	D4	Data 4
4	D5	D5	Data 5
5	D6	D6	Data 6
6	D7	D7	Data 7
7	CE1#	CE1#	
8	A10	A10	Address 10
9	OE#	OE#	Output Enable
10	A11	A11	Address 11
11	A9	A9	Address 9
12	A8	A8	Address 8
13	A13	A13	Address 13
14	A14	A14	Address 14

15	WE#	WE#	Write Enable ???
16	READY	IREQ#	
17	Vcc	Vcc	Vcc
18	Vpp1	Vpp1	Vpp1
19	A16	A16	Address 16
20	A15	A15	Address 15
21	A12	A12	Address 12
22	A7	A7	Address 7
23	A6	A6	Address 6
24	A5	A5	Address 5
25	A4	A4	Address 4
26	A3	A3	Address 3
27	A2	A2	Address 2
28	A1	A1	Address 1
29	A0	A0	Address 0
30	D0	D0	Data 0
31	D1	D1	Data 1
32	D2	D2	Data 2
33	WP	IOIS16#	
34	GND	GND	Ground
35	GND	GND	Ground
36	CD1#	CD1#	Card Detect 1
37	D11	D11	Data 11
38	D12	D12	Data 12
39	D13	D13	Data 13
40	D14	D14	Data 14
41	D15	D15	Data 15
42	CE2#	CE2#	
43	VS1#	VS1#	
44	RSRVD	IORD#	Reserved / IORD#
45	RSRVD	IOWR#	Reserved / IOWR#
46	A17	A17	Address 17



47	A18	A18	Address 18
48	A19	A19	Address 19
49	A20	A20	Address 20
50	A21	A21	Address 21
51	Vcc	Vcc	Vcc
52	Vpp2	Vpp2	Vpp2
53	A22	A22	Address 22
54	A23	A23	Address 23
55	A24	A24	Address 24
56	A25	A25	Address 25
57	VS2#	VS2#	
58	RESET	RESET	Reset
59	WAIT#	WAIT#	
60	RSRVD	INPACK#	Reserved / ???
61	REG#	REG#	
62	BVD2	SPKR#	Battery Voltage 2 / Speaker ???
63	BVD1	STSCHG#	Battery Voltage 1 / ???
64	D8	D8	Data 8
65	D9	D9	Data 9
66	D10	D10	Data 10
67	CD2#	CD2#	
68	GND	GND	Ground

Contributor: [Joakim Ögren](#)

Source:  
PC Card Standard at PC Card's homepage

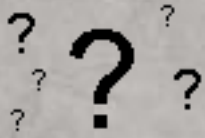
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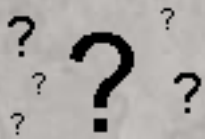
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# PC/104



(at the backplane)



(at the device (card))

UNKNOWN CONNECTOR at the backplane.

UNKNOWN CONNECTOR at the device (card).

Pin	J1/P1	J1/P1	J2/P2	J2/P2
Number	Row A	Row B	Row C1	Row D1
0	--	--	0V	0V
1	IOCHCHK*	0V	SBHE*	MEMCS16*
2	SD7	RESETDRV	LA23	IOCS16*
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	ENDXFR*	LA17	DACK0*
9	SD0	+12V	MEMR*	DRQ0
10	IOCHRDY	(KEY)2	MEMW*	DACK5*
11	AEN	SMEMW*	SD8	DRQ5
12	SA19	SMEMR*	SD9	DACK6*
13	SA18	IOW*	SD10	DRQ6
14	SA17	IOR*	SD11	DACK7*

15	SA16	DACK3*	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	DACK1*	SD14	MASTER*
18	SA13	DRQ1	SD15	0V
19	SA12	REFRESH*		(KEY)2 0V
20	SA11	SYSCLK	--	--
21	SA10	IRQ7	--	--
22	SA9	IRQ6	--	--
23	SA8	IRQ5	--	--
24	SA7	IRQ4	--	--
25	SA6	IRQ3	--	--
26	SA5	DACK2*	--	--
27	SA4	TC	--	--
28	SA3	BALE	--	--
29	SA2	+5V	--	--
30	SA1	OSC	--	--
31	SA0	0V	--	--
32	0V	0V	--	--

Contributor: [Joakim Ögren](#)

Source:  
[PC/104 v2.3 spec](#)

Info: [PC/104 Consortium](#)

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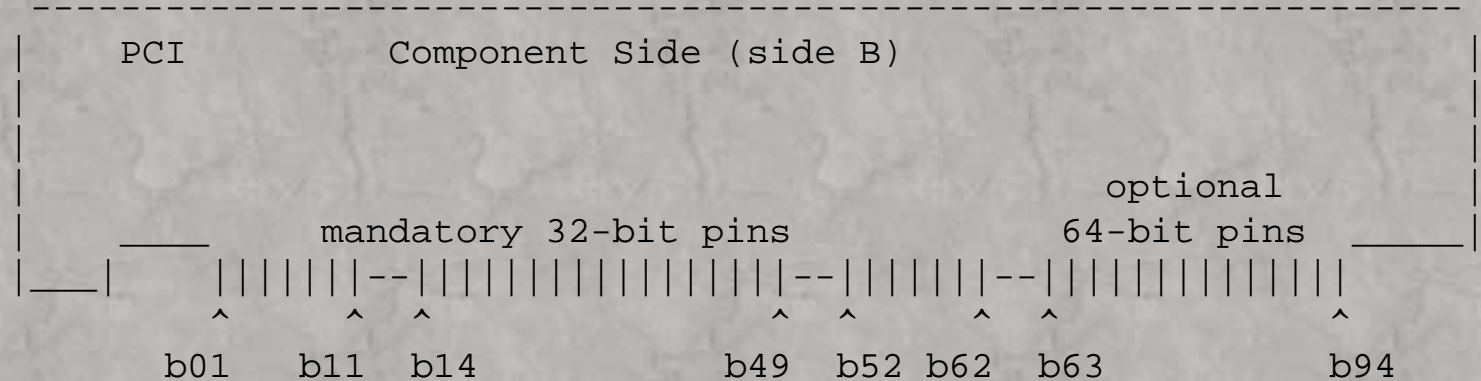
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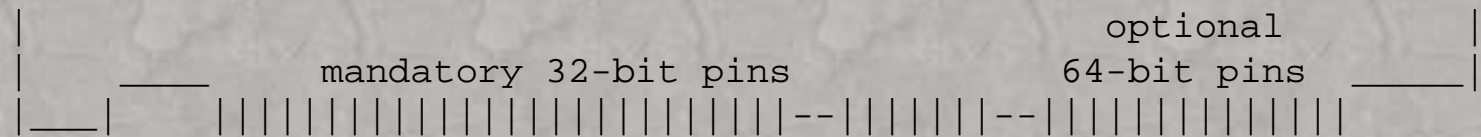
# PCI

PCI=Peripheral Component Interconnect

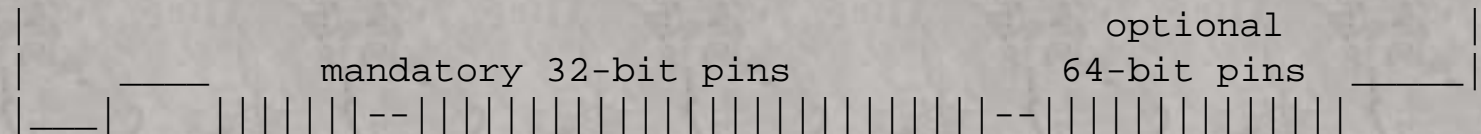
PCI Universal Card 32/64 bit



PCI 5V Card 32/64 bit



PCI 3.3V Card 32/64 bit



**NOT  
DRAWN  
YET...**

(at the computer)

98+22 PIN EDGE CONNECTOR at the computer.

Pin	+5V	+3.3V	Universal	Description
A1	TRST			Test Logic Reset
A2	+12V			+12 VDC



A3	TMS			Test Mde Select
A4	TDI			Test Data Input
A5	+5V			+5 VDC
A6	INTA			Interrupt A
A7	INTC			Interrupt C
A8	+5V			+5 VDC
A9	RESV01			Reserved VDC
A10	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A11	RESV03			Reserved VDC
A12	GND03	(OPEN)	(OPEN)	Ground or Open (Key)
A13	GND05	(OPEN)	(OPEN)	Ground or Open (Key)
A14	RESV05			Reserved VDC
A15	RESET			Reset
A16	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A17	GNT			Grant PCI use
A18	GND08			Ground
A19	RESV06			Reserved VDC
A20	AD30			Address/Data 30
A21	+3.3V01			+3.3 VDC
A22	AD28			Address/Data 28
A23	AD26			Address/Data 26
A24	GND10			Ground
A25	AD24			Address/Data 24
A26	IDSEL			Initialization Device Select
A27	+3.3V03			+3.3 VDC
A28	AD22			Address/Data 22
A29	AD20			Address/Data 20
A30	GND12			Ground
A31	AD18			Address/Data 18
A32	AD16			Address/Data 16
A33	+3.3V05			+3.3 VDC
A34	FRAME			Address or Data phase

A35	GND14			Ground
A36	TRDY			Target Ready
A37	GND15			Ground
A38	STOP			Stop Transfer Cycle
A39	+3.3V07			+3.3 VDC
A40	SDONE			Snoop Done
A41	SBO			Snoop Backoff
A42	GND17			Ground
A43	PAR			Parity
A44	AD15			Address/Data 15
A45	+3.3V10			+3.3 VDC
A46	AD13			Address/Data 13
A47	AD11			Address/Data 11
A48	GND19			Ground
A49	AD9			Address/Data 9
A52	C/BE0			Command, Byte Enable 0
A53	+3.3V11			+3.3 VDC
A54	AD6			Address/Data 6
A55	AD4			Address/Data 4
A56	GND21			Ground
A57	AD2			Address/Data 2
A58	AD0			Address/Data 0
A59	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A60	REQ64			Request 64 bit ???
A61	VCC11			+5 VDC
A62	VCC13			+5 VDC
A63	GND			Ground
A64	C/BE[7]#			Command, Byte Enable 7
A65	C/BE[5]#			Command, Byte Enable 5
A66	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A67	PAR64			Parity 64 ???

A68	AD62			Address/Data 62
A69	GND			Ground
A70	AD60			Address/Data 60
A71	AD58			Address/Data 58
A72	GND			Ground
A73	AD56			Address/Data 56
A74	AD54			Address/Data 54
A75	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A76	AD52			Address/Data 52
A77	AD50			Address/Data 50
A78	GND			Ground
A79	AD48			Address/Data 48
A80	AD46			Address/Data 46
A81	GND			Ground
A82	AD44			Address/Data 44
A83	AD42			Address/Data 42
A84	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
A85	AD40			Address/Data 40
A86	AD38			Address/Data 38
A87	GND			Ground
A88	AD36			Address/Data 36
A89	AD34			Address/Data 34
A90	GND			Ground
A91	AD32			Address/Data 32
A92	RES			Reserved
A93	GND			Ground
A94	RES			Reserved
B1	-12V			-12 VDC
B2	TCK			Test Clock
B3	GND			Ground
B4	TDO			Test Data Output

B5	+5V			+5 VDC
B6	+5V			+5 VDC
B7	INTB			Interrupt B
B8	INTD			Interrupt D
B9	PRSNT1			Reserved
B10	RES			+V I/O (+5 V or +3.3 V)
B11	PRSNT2			??
B12	GND	(OPEN)	(OPEN)	Ground or Open (Key)
B13	GND	(OPEN)	(OPEN)	Ground or Open (Key)
B14	RES			Reserved VDC
B15	GND			Reset
B16	CLK			Clock
B17	GND			Ground
B18	REQ			Request
B19	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B20	AD31			Address/Data 31
B21	AD29			Address/Data 29
B22	GND			Ground
B23	AD27			Address/Data 27
B24	AD25			Address/Data 25
B25	+3.3V			+3.3VDC
B26	C/BE3			Command, Byte Enable 3
B27	AD23			Address/Data 23
B28	GND			Ground
B29	AD21			Address/Data 21
B30	AD19			Address/Data 19
B31	+3.3V			+3.3 VDC
B32	AD17			Address/Data 17
B33	C/BE2			Command, Byte Enable 2
B34	GND13			Ground
B35	IRDY			Initiator Ready
B36	+3.3V06			+3.3 VDC



B37	DEVSEL			Device Select
B38	GND16			Ground
B39	LOCK			Lock bus
B40	PERR			Parity Error
B41	+3.3V08			+3.3 VDC
B42	SERR			System Error
B43	+3.3V09			+3.3 VDC
B44	C/BE1			Command, Byte Enable 1
B45	AD14			Address/Data 14
B46	GND18			Ground
B47	AD12			Address/Data 12
B48	AD10			Address/Data 10
B49	GND20			Ground
B50	(OPEN)	GND	(OPEN)	Ground or Open (Key)
B51	(OPEN)	GND	(OPEN)	Ground or Open (Key)
B52	AD8			Address/Data 8
B53	AD7			Address/Data 7
B54	+3.3V12			+3.3 VDC
B55	AD5			Address/Data 5
B56	AD3			Address/Data 3
B57	GND22			Ground
B58	AD1			Address/Data 1
B59	VCC08			+5 VDC
B60	ACK64			Acknowledge 64 bit ???
B61	VCC10			+5 VDC
B62	VCC12			+5 VDC
B63	RES			Reserved
B64	GND			Ground
B65	C/BE[6]#			Command, Byte Enable 6
B66	C/BE[4]#			Command, Byte Enable 4
B67	GND			Ground

B68	AD63			Address/Data 63
B69	AD61			Address/Data 61
B70	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B71	AD59			Address/Data 59
B72	AD57			Address/Data 57
B73	GND			Ground
B74	AD55			Address/Data 55
B75	AD53			Address/Data 53
B76	GND			Ground
B77	AD51			Address/Data 51
B78	AD49			Address/Data 49
B79	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B80	AD47			Address/Data 47
B81	AD45			Address/Data 45
B82	GND			Ground
B83	AD43			Address/Data 43
B84	AD41			Address/Data 41
B85	GND			Ground
B86	AD39			Address/Data 39
B87	AD37			Address/Data 37
B88	+5V	+3.3V	Signal Rail	+V I/O (+5 V or +3.3 V)
B89	AD35			Address/Data 35
B90	AD33			Address/Data 33
B91	GND			Ground
B92	RES			Reserved
B93	RES			Reserved
B94	GND			Ground

*Notes: Pin 63-94 exists only on 64 bit PCI implementations.*

*+V I/O is 3.3V on 3.3V boards, 5V on 5V boards, and define signal rails on the Universal board.*

*Contributor: [Joakim Ögren](#), [Phil Toms](#)*

*Source:*  
*?*

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# PCI (technical)

This section is currently based solely on the work by Mark Sokos.

This file is not intended to be a thorough coverage of the PCI standard. It is for informational purposes only, and is intended to give designers and hobbyists an overview of the bus so that they might be able to design their own PCI cards. Thus, I/O operations are explained in the most detail, while memory operations, which will usually not be dealt with by an I/O card, are only briefly explained. Hobbyists are also warned that, due to the higher clock speeds involved, PCI cards are more difficult to design than ISA cards or cards for other slower busses. Many companies are now making PCI prototyping cards, and, for those fortunate enough to have access to FPGA programmers, companies like Xilinx are offering PCI compliant designs which you can use as a starting point for your own projects.

For a copy of the full PCI standard, contact:

PCI Special Interest Group (SIG)  
PO Box 14070  
Portland, OR 97214  
1-800-433-5177  
1-503-797-4207

## Signal Descriptions:

### AD(x)

Address/Data Lines.

### CLK

Clock. 33 MHz maximum.

### C/BE(x)

Command, Byte Enable.

### FRAME



Used to indicate whether the cycle is an address phase or a data phase.

## **DEVSEL**

Device Select.

## **IDSEL**

Initialization Device Select

## **INT(x)**

Interrupt

## **IRDY**

Initiator Ready

## **LOCK**

Used to manage resource locks on the PCI bus.

## **REQ**

Request. Requests a PCI transfer.

## **GNT**

Grant. indicates that permission to use PCI is granted.

## **PAR**

Parity. Used for AD0-31 and C/BE0-3.

## **PERR**

Parity Error.

## **RST**

Reset.

## **SBO**

Snoop Backoff.

## **SDONE**

Snoop Done.

## **SERR**

System Error. Indicates an address parity error for special cycles or a system error.

## **STOP**

Asserted by Target. Requests the master to stop the current transfer cycle.

## **TCK**

Test Clock

## **TDI**

Test Data Input

## **TDO**

Test Data Output

## **TMS**

Test Mode Select

## **TRDY**

Target Ready

## **TRST**

### Test Logic Reset

The PCI bus treats all transfers as a burst operation. Each cycle begins with an address phase followed by one or more data phases. Data phases may repeat indefinitely, but are limited by a timer that defines the maximum amount of time that the PCI device may control the bus. This timer is set by the CPU as part of the configuration space. Each device has its own timer (see the Latency Timer in the configuration space).

The same lines are used for address and data. The command lines are also used for byte enable lines. This is done to reduce the overall number of pins on the PCI connector.

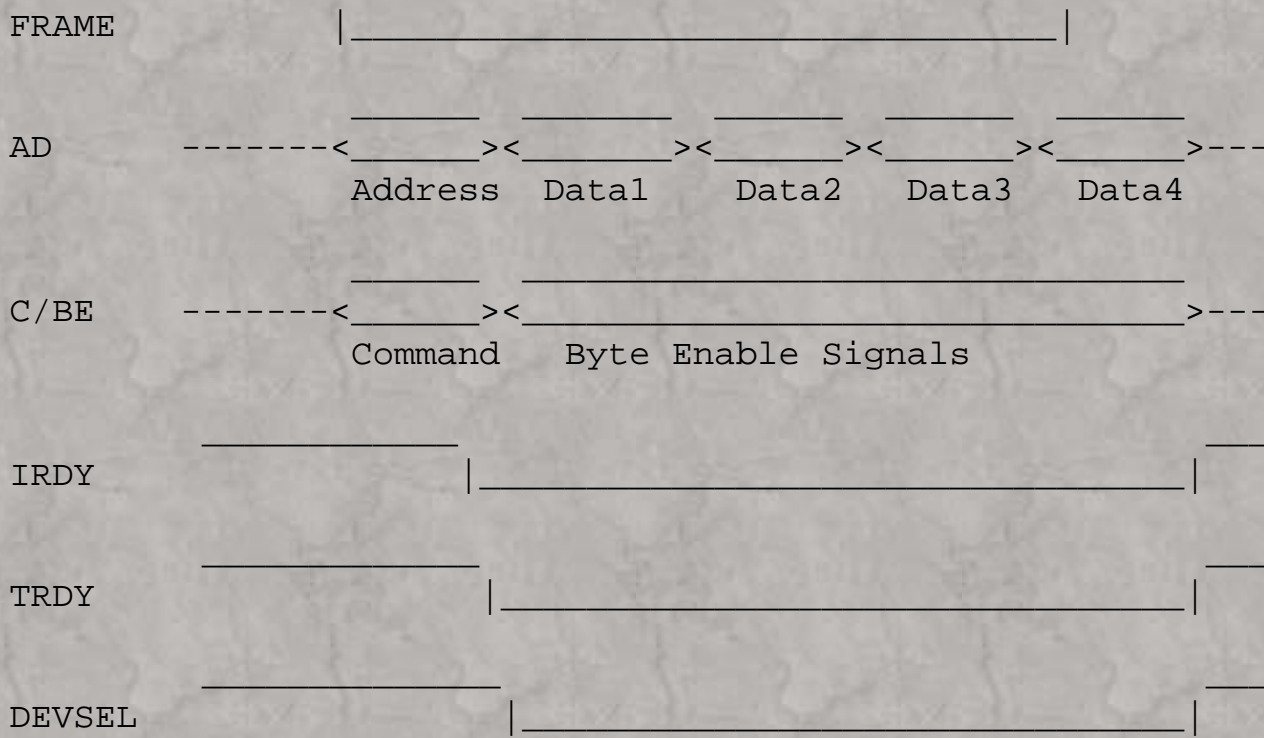
The Command lines (C/BE3 to C/BE0) indicate the type of bus transfer during the address phase.

C/BE	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	reserved
0101	reserved
0110	Memory Read
0111	Memory Write
1000	reserved
1001	reserved
1010	Configuration Read
1011	Configuration Write
1100	Multiple Memory Read
1101	Dual Address Cycle
1110	Memory-Read Line
1111	Memory Write and Invalidate

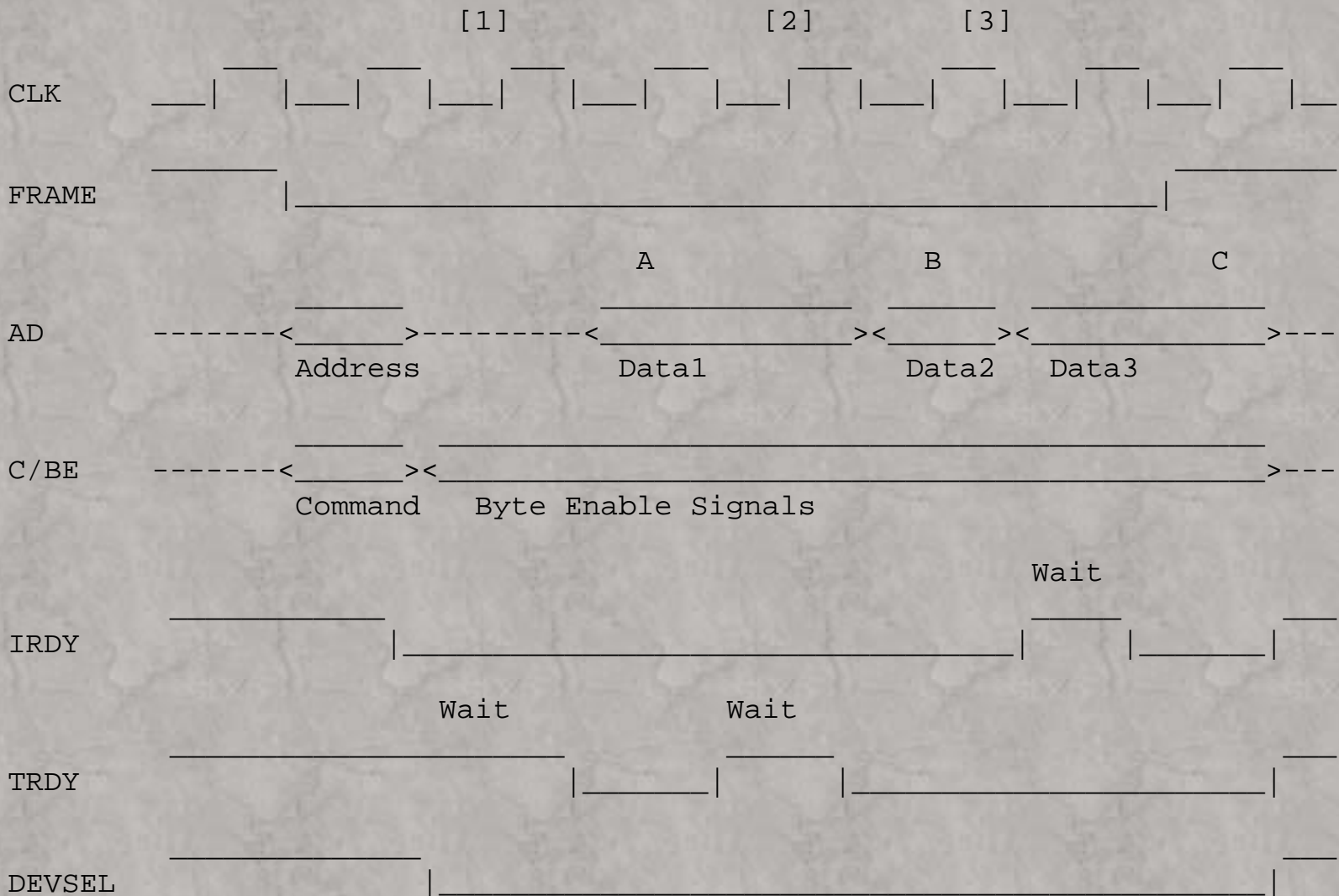
The three basic types of transfers are I/O, Memory, and Configuration.

## PCI timing diagrams:





PCI transfer cycle, 4 data phases, no wait states. Data is transferred on the rising edge of CLK.





PCI transfer cycle, with wait states. Data is transferred on the rising edge of CLK at points labelled A, B, and C.

## Bus Cycles:

### Interrupt Acknowledge (0000)

The interrupt controller automatically recognizes and reacts to the INTA (interrupt acknowledge) command. In the data phase, it transfers the interrupt vector to the AD lines.

### Special Cycle (0001)

AD15-AD0	Description
0x0000	Processor Shutdown
0x0001	Processor Halt
0x0002	x86 Specific Code
0x0003 to 0xFFFF	Reserved

### I/O Read (0010) and I/O Write (0011)

Input/Output device read or write operation. The AD lines contain a byte address (AD0 and AD1 must be decoded). PCI I/O ports may be 8 or 16 bits. PCI allows 32 bits of address space. On IBM compatible machines, the Intel CPU is limited to 16 bits of I/O space, which is further limited by some ISA cards that may also be installed in the machine (many ISA cards only decode the lower 10 bits of address space, and thus mirror themselves throughout the 16 bit I/O space). This limit assumes that the machine supports ISA or EISA slots in addition to PCI slots.

The PCI configuration space may also be accessed through I/O ports 0x0CF8 (Address) and 0x0CFC (Data). The address port must be written first.

### Memory Read (0110) and Memory Write (0111)

A read or write to the system memory space. The AD lines contain a doubleword address. AD0 and AD1 do not need to be decoded. The Byte Enable lines (C/BE) indicate which bytes are valid.

### Configuration Read (1010) and Configuration Write (1011)

A read or write to the PCI device configuration space, which is 256 bytes in length. It is accessed in

doubleword units. AD0 and AD1 contain 0, AD2-7 contain the doubleword address, AD8-10 are used for selecting the addressed unit a the malfunction unit, and the remaining AD lines are not used.

Address	Bit 32	16	15	0
00	Unit ID		Manufacturer ID	
04	Status		Command	
08	Class Code			Revision
0C	BIST	Header	Latency	CLS
10-24	Base Address Register			
28	Reserved			
2C	Reserved			
30	Expansion ROM Base Address			
34	Reserved			
38	Reserved			
3C	MaxLat	MnGNT	INT-pin	INT-line
40-FF	available for PCI unit			

## Multiple Memory Read (1100)

This is an extension of the memory read bus cycle. It is used to read large blocks of memory without caching, which is beneficial for long sequential memory accesses.

## Dual Address Cycle (1101)

Two address cycles are necessary when a 64 bit address is used, but only a 32 bit physical address exists. The least significant portion of the address is placed on the AD lines first, followed by the most significant 32 bits. The second address cycle also contains the command for the type of transfer (I/O, Memory, etc). The PCI bus supports a 64 bit I/O address space, although this is not available on Intel based PCs due to limitations of the CPU.

## Memory-Read Line (1110)

This cycle is used to read in more than two 32 bit data blocks, typically up to the end of a cache line. It is more efficient than normal memory read bursts for a long series of sequential memory accesses.

## Memory Write and Invalidate (1111)

This indicates that a minimum of one cache line is to be transferred. This allows main memory to be updated, saving a cache write-back cycle.

## Bus Arbitration:

This section is under construction.

## PCI BIOS:

This section is under construction.

*Contributor:* [Joakim Ögren](#), [Mark Sokos](#)

*Sources:*

[Mark Sokos PCI page](#)

*"Inside the PCI Local Bus" by Guy W. Kendall, Byte, February 1994 v 19 p. 177-180*

*"The Indispensable PC Hardware Book" by Hans-Peter Messmer, ISBN 0-201-8769-3*

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# PCMCIA

PCMCIA=Personal Computer Memory Card International Association.

**NOT  
DRAWN  
YET...**

(at the controller)

**NOT  
DRAWN  
YET...**
























(at the peripherals)



















68 PIN ??? MALE at the controller.

68 PIN ??? FEMALE at the peripherals.

Pin	Name	Dir	Description
1	GND	—	Ground
2	D3	↔	Data 3
3	D4	↔	Data 4
4	D5	↔	Data 5
5	D6	↔	Data 6
6	D7	↔	Data 7
7	/CE1	→	Card Enable 1
8	A10	→	Address 10
9	/OE	→	Output Enable
10	A11	→	Address 11
11	A9	→	Address 9
12	A8	→	Address 8
13	A13	→	Address 13
14	A14	→	Address 14



15	/WE:/P		Write Enable : Program
16	/READY:/IREQ		Ready : Busy (IREQ)
17	VCC		+5V
18	VPP1		Programming Voltage (EPROM)
19	A16		Address 16
20	A15		Address 15
21	A12		Address 12
22	A7		Address 7
23	A6		Address 6
24	A5		Address 5
25	A4		Address 4
26	A3		Address 3
27	A2		Address 2
28	A1		Address 1
29	A0		Address 0
30	D0		Data 0
31	D1		Data 1
32	D2		Data 2
33	/WP:/IOIS16		Write Protect : IOIS16
34	GND		Ground
35	GND		Ground
36	/CD1		Card Detect 1
37	D11		Data 11
38	D12		Data 12
39	D13		Data 13
40	D14		Data 14
41	D15		Data 15
42	/CE2		Card Enable 2
43	/VS1		Refresh
44	/IORD	?	I/O Read
45	/IOWR	?	I/O Write
46	A17		Address 17

47	A18		Address 18
48	A19		Address 19
49	A20		Address 20
50	A21		Address 21
51	VCC		+5V
52	VPP2		Programming Voltage 2 (EPROM)
53	A22		Address 22
54	A23		Address 23
55	A24		Address 24
56	A25		Address 25
57	/VS2	?	RFU
58	RESET	?	RESET
59	/WAIT	?	WAIT
60	/INPACK	?	
61	/REG		Register Select
62	/BVD2:SPKR		Battery Voltage Detect 2 : SPKR
63	/BVD1:STSCHG		Battery Voltage Detect 1 : STSCHG
64	D8		Data 8
65	D9		Data 9
66	D10		Data 10
67	/CD2		Card Detect 2
68	GND		Ground

*Note: Direction is Controller (computer) relative PCMCIA-card.*

*Contributor: [Joakim Ögren](#), [Karsten Wenke](#)*

*Source:  
?*

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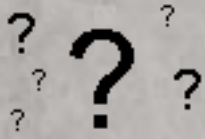
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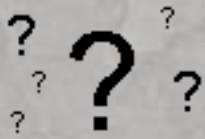


# SSFDC

SSFDC=Solid State Floppy Disk Card.



(at the motherboard)



(at the device)

UNKNOWN CONNECTOR at the motherboard.

UNKNOWN CONNECTOR at the device.

**I don't have any technical information about SSFDC at the moment. If you have any information of value please send it to me.**

Contributor: [Joakim Ögren](#)

Source:  
?

Info: [Solid State Floppy Disk Card Forum](#)

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# SUN SBus

96 PIN UNKNOWN FEMALE CONNECTOR (Fujitsu FCN 234P096-G/Y) at the Motherboard

96 PIN UNKNOWN MALE CONNECTOR (Fujitsu FCN 234P096-G) at the Motherboard

Available on the SUN SPARCengine 5 motherboard

Pin	Name	Description
1	GND	Ground
2	sb_br*	sb_br
3	sb_sel*	sb_sel
4	sb_irq1*	?
5	sb_d(0)	Data bit 0
6	sb_d(2)	Data bit 2
7	sb_d(4)	Data bit 4
8	sb_irq2*	Interrupt Request 2
9	sb_d(6)	Data bit 6
10	sb_d(8)	Data bit 8
11	sb_d(10)	Data bit 10
12	sb_irq3*	Interrupt Request 3
13	sb_d(12)	Data bit 12
14	sb_d(14)	Data bit 14
15	sb_d(16)	Data bit 16
16	sb_irq4*	Interrupt Request 4
17	sb_d(19)	Data bit 19
18	sb_d(21)	Data bit 21
19	sb_d(23)	Data bit 23
20	sb_irq5*	Interrupt Request 5
21	sb_d(25)	Data bit 25



22	sb_d(27)	Data bit 27
23	sb_d(29)	Data bit 29
24	sb_irq6*	Interrupt Request 6
25	sb_d(31)	Data bit 31
26	sb_siz(0)	sb_siz(0)
27	sb_siz(2)	sb_siz(2)
28	sb_irq7*	Interrupt Request 7
29	sb_a(0)	Address bit 0
30	sb_a(2)	Address bit 2
31	sb_a(4)	Address bit 4
32	sb_merr*	sb_merr
33	sb_a(6)	Address bit 6
34	sb_a(8)	Address bit 8
35	sb_a(10)	Address bit 10
36	sb_err*	sb_err
37	sb_pa(12)	Address bit 12
38	sb_pa(14)	Address bit 14
39	sb_pa(16)	Address bit 16
40	sb_ack8*	sb_ack8
41	sb_pa(18)	Address bit 18
42	sb_pa(20)	Address bit 20
43	sb_pa(22)	Address bit 22
44	sb_ack32*	sb_ack32
45	sb_pa(24)	Address bit 24
46	sb_pa(26)	Address bit 26
47	N/C	Not connected
48	-12V	-12 VDC
49	sb_clk	Clock
50	sb_bg*	sb_bg
51	sb_as*	sb_as
52	GND	Ground
53	sb_d(1)	Data bit 1

54	sb_d(3)	Data bit 3
55	sb_d(5)	Data bit 5
56	+5V	+5 VDC
57	sb_d(7)	Data bit 7
58	sb_d(9)	Data bit 9
59	sb_d(11)	Data bit 11
60	GND	Ground
61	sb_d(13)	Data bit 13
62	sb_d(15)	Data bit 15
63	sb_d(17)	Data bit 17
64	+5V	+5 VDC
65	sb_d(18)	Data bit 18
66	sb_d(20)	Data bit 20
67	sb_d(22)	Data bit 22
68	GND	Ground
69	sb_d(24)	Data bit 24
70	sb_d(26)	Data bit 26
71	sb_d(28)	Data bit 28
72	+5V	+5 VDC
73	sb_d(30)	Data bit 30
74	sb_siz(1)	sb_siz(1
75	sb_rd	sb_rd
76	GND	Ground
77	sb_a(1)	Address bit 1
78	sb_a(3)	Address bit 3
79	sb_a(5)	Address bit 5
80	+5V	+5 VDC
81	sb_a(7)	Address bit 7
82	sb_a(9)	Address bit 9
83	sb_a(11)	Address bit 11
84	GND	Ground
85	sb_pa(13)	Address bit 13

86	sb_pa(15)	Address bit 15
87	sb_pa(17)	Address bit 17
88	+5V	+5 VDC
89	sb_pa(19)	Address bit 19
90	sb_pa(21)	Address bit 21
91	sb_pa(23)	Address bit 23
92	GND	Ground
93	sb_pa(25)	Address bit 25
94	sb_pa(27)	Address bit 27
95	sb_reset*	Reset
96	+12V	+12 VDC

Contributor: [Joakim Ögren](#)

Source:  
[SUN SPARCengine 5 manual](#) at [SUN manuals site](#)

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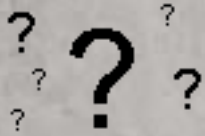
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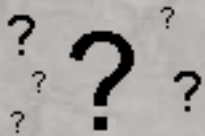
# SmallPCI

PCI=Peripheral Component Interconnect.

SmallPCI is a version of PCI adapted for small computers and PDAs.



(at the motherboard)



(at the device)

UNKNOWN CONNECTOR at the motherboard.

UNKNOWN CONNECTOR at the device.

**I don't have any technical information about SmallPCI at the moment. If you have any information of value please send it to me.**

The specifications can be obtained from:

PCI Special Interest Group  
2575 NE Kathryn St. #17  
Hillsboro, OR 97124  
Phone: 1-800-433-5177  
Fax: 1-503-693-8344

Contributor: [Joakim Ögren](#)

Source:  
?

Info: [SmallPCI overview](#) at [PCI Special Interest Group's homepage](#)

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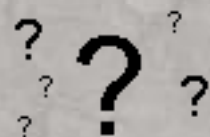
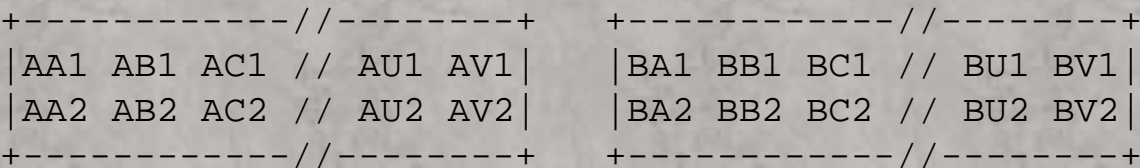


*Document last modified: 2001-06-08*



# Unibus

Available on the old Digital PDP-11.



(at the computer)

2 x 36 EDGE FEMALE at the backplane.  
2 x 36 EDGE MALE at the cards/modules.

Pin	Name
AA1	/INIT
AA2	POWER(+5v)
AB1	/INTR
AB2	GROUND
AC1	/D00
AC2	GROUND
AD1	/D02
AD2	/D01
AE1	/D04
AE2	/D03
AF1	/D06
AF2	/D05
AH1	/D08
AH2	/D07

AJ1	/D10
AJ2	/D09
AK1	/D12
AK2	/D11
AL1	/D14
AL2	/D13
AM1	/PA
AM2	/D15
AN1	GROUND
AN2	/PB
AP1	GROUND
AP2	/BBSY
AR1	GROUND
AR2	/SACK
AS1	GROUND
AS2	/NPR
AT1	GROUND
AT2	/BR7
AU1	NPG
AU2	/BR6
AV1	BG7
AV2	GROUND
BA1	BG6
BA2	POWER(+5v)
BB1	BG5
BB2	GROUND
BC1	/BR5
BC2	GROUND
BD1	GROUND
BD2	/BR4
BE1	GROUND

BE2	BG4
BF1	/ACLO
BF2	/DCLO
BH1	/A01
BH2	/A00
BJ1	/A03
BJ2	/A02
BK1	/A05
BK2	/A04
BL1	/A07
BL2	/A06
BM1	/A09
BM2	/A08
BN1	/A11
BN2	/A10
BP1	/A13
BP2	/A12
BR1	/A15
BR2	/A14
BS1	/A17
BS2	/A16
BT1	GROUND
BT2	/C1
BU1	/SSYN
BU2	/CO
BV1	/MSYN
BV2	GROUND

Contributor: [Rob Gill](#)

Source:  
*Digital PDP-11 peripherals handbook*



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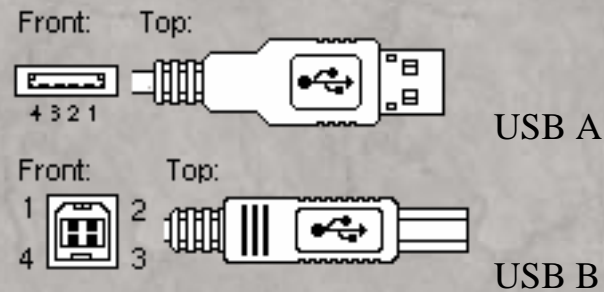
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# Universal Serial Bus (USB)

Developed by Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC and Phillips.



Series "A" plugs are used towards the host system and series "B" plugs are used towards the USB device.

Pin	Name	Description
1	VBUS	+5 VDC
2	D-	Data -
3	D+	Data +
4	GND	Ground

Contributor: [Joakim Ögren, Tomas Ögren](#)

Source:

[USB FAQ](#) at [USB Implementers Forum](#),

USB Specification v2.0 at [USB Implementers Forum](#)

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# Universal Serial Bus (USB) (technical)

Developed by Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC and Phillips.

## Features:

- True Plug'n'Play.
- Hot plug and unplug
- Low cost
- Easy of use
- 127 physical devices
- Low cost cables and connectors

## Bandwidth:

- High speed: 480 Mbps speed (in USB 2.0 and above)
- Full speed: 12 Mbps speed (requires shielded cable)
- Low speed: 1.5 Mbps speed (non-shielded cable)

## Definitions:

USB Host = The computer, only one host per USB system.

USB Device = A *hub* or a *Function*.

## Power usage:

**Bus-powered hubs:** Draw Max 100 mA at power up and 500 mA normally.

**Self-powered hubs:** Draw Max 100 mA, must supply 500 mA to each port.

**Low power, bus-powered functions:** Draw Max 100 mA.

**High power, bus-powered functions:** Self-powered hubs: Draw Max 100 mA, must supply 500 mA to each port.

**Self-powered functions:** Draw Max 100 mA.

**Suspended device:** Max 0.5 mA

# Voltage:

- Supplied voltage by a host or a powered hub ports is between 4.75 V and 5.25 V.
- Maximum voltage drop for bus-powered hubs is 0.35 V from it's host or hub to the hubs output port.
- All hubs and functions must be able to send configuration data at 4.4 V, but only low-power functions need to be working at this voltage.
- Normal operational voltage for functions is minimum 4.75 V.

# Shielding:

Shield should only be connected to Ground at the host. No device should connect Shield to Ground.

# Cable:

## Shielded:

Data: 28 AWG twisted

Power: 28 AWG - 20 AWG non-twisted

## Non-shielded:

Data: 28 AWG non-twisted

Power: 28 AWG - 20 AWG non-twisted

Power Gauge	Max length
28	0.81 m
26	1.31 m
24	2.08 m
22	3.33 m
20	5.00 m

# Cable colors:

Pin	Name	Cable color	Description
1	VBUS	Red	+5 VDC
2	D-	White	Data -



3	D+	Green	Data +
4	GND	Black	Ground

Contributor: [Joakim Ögren](#)

Source:

[USB FAQ](#) at [USB Implementers Forum](#),

USB Specification v2.0 at [USB Implementers Forum](#)

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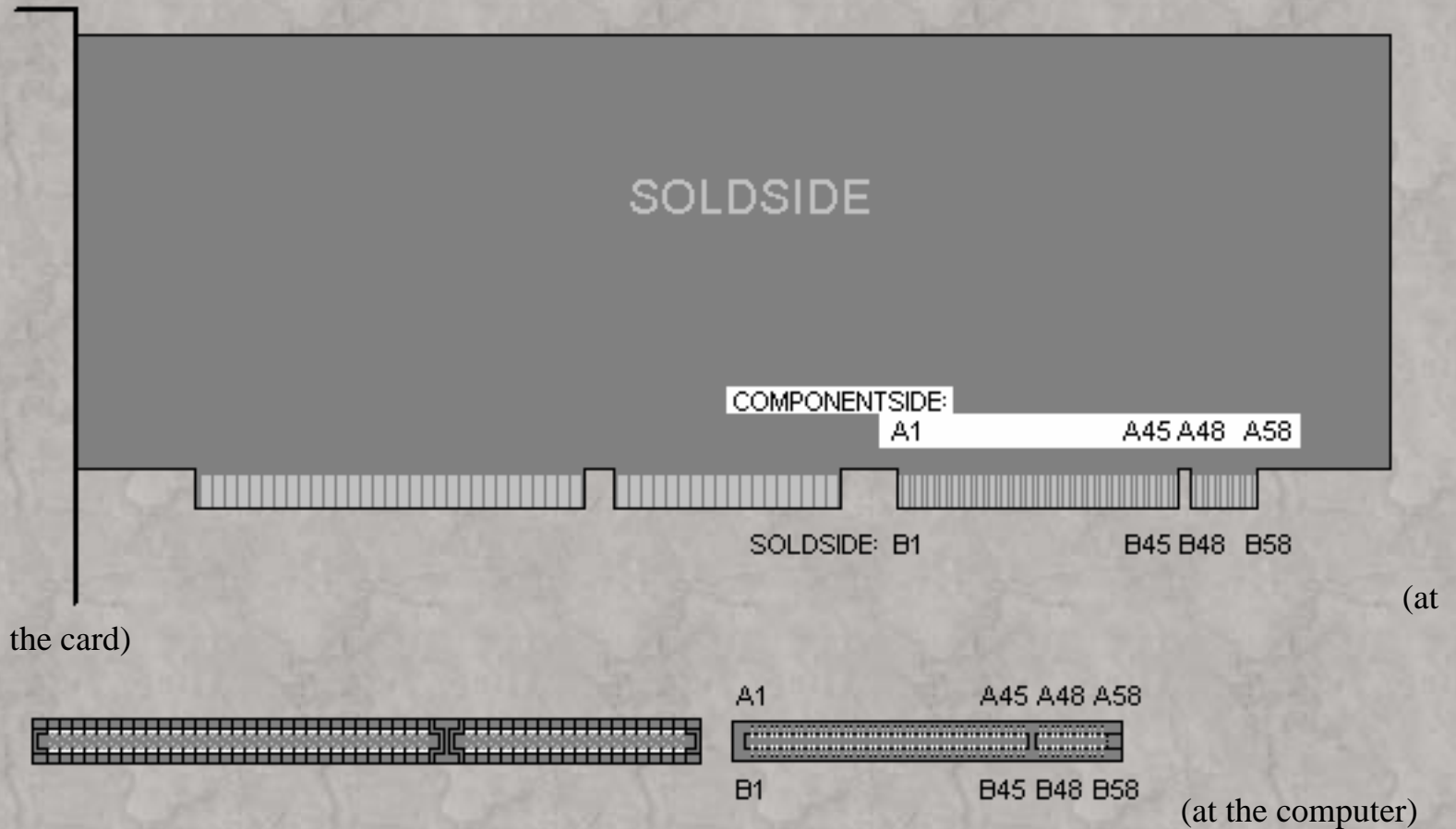
Document last modified: 2001-06-06



# VESA LocalBus (VLB)

VLB=VESA Local Bus.

VESA=Video Electronics Standards Association.



58 PIN EDGE CONNECTOR MALE at the card.

58 PIN EDGE CONNECTOR FEMALE at the computer.

Pin	Name	Description
A1	D1	Data 1
A2	D3	Data 3
A3	GND	Ground
A4	D5	Data 5
A5	D7	Data 7

A6	D9	Data 9
A7	D11	Data 11
A8	D13	Data 13
A9	D15	Data 15
A10	GND	Ground
A11	D17	Data 17
A12	Vcc	+5 VDC
A13	D19	Data 19
A14	D21	Data 21
A15	D23	Data 23
A16	D25	Data 25
A17	GND	Ground
A18	D27	Data 27
A19	D29	Data 2
A20	D31	Data 31
A21	A30	Address 30
A22	A28	Address 28
A23	A26	Address 26
A24	GND	Ground
A25	A24	Address 24
A26	A22	Address 22
A27	VCC	+5 VDC
A28	A20	Address 20
A29	A18	Address 18
A30	A16	Address 16
A31	A14	Address 14
A32	A12	Address 12
A33	A10	Address 10
A34	A8	Address 8
A35	GND	Ground
A36	A6	Address 6
A37	A4	Address 4

A38	WBACK#	Write Back
A39	BE0#	Byte Enable 0
A40	VCC	+5 VDC
A41	BE1#	Byte Enable 1
A42	BE2#	Byte Enable 2
A43	GND	Ground
A44	BE3#	Byte Enable 3
A45	ADS#	Address Strobe
A48	LRDY#	Local Ready
A49	LDEV	Local Device
A50	LREQ	Local Request
A51	GND	Ground
A52	LGNT	Local Grant
A53	VCC	+5 VDC
A54	ID2	Identification 2
A55	ID3	Identification 3
A56	ID4	Identification 4
A57	LKEN#	
A58	LEADS#	Local Enable Address Strobe
B1	D0	Data 0
B2	D2	Data 2
B3	D4	Data 4
B4	D6	Data 6
B5	D8	Data 8
B6	GND	Ground
B7	D10	Data 10
B8	D12	Data 12
B9	VCC	+5 VDC
B10	D14	Data 14
B11	D16	Data 16



B12	D18	Data 18
B13	D20	Data 20
B14	GND	Ground
B15	D22	Data 22
B16	D24	Data 24
B17	D26	Data 26
B18	D28	Data 28
B19	D30	Data 30
B20	VCC	+5 VDC
B21	A31	Address 31
B22	GND	Ground
B23	A29	Address 29
B24	A27	Address 27
B25	A25	Address 25
B26	A23	Address 23
B27	A21	Address 21
B28	A19	Address 19
B29	GND	Ground
B30	A17	Address 17
B31	A15	Address 15
B32	VCC	+5 VDC
B33	A13	Address 13
B34	A11	Address 11
B35	A9	Address 9
B36	A7	Address 7
B37	A5	Address 5
B38	GND	Ground
B39	A3	Address 3
B40	A2	Address 2
B41	n/c	Not connected
B42	RESET#	Reset
B43	DC#	Data/Command

B44	M/IO#	Memory/IO
B45	W/R#	Write/Read
B48	RDYRTN#	Ready Return
B49	GND	Ground
B50	IRQ9	Interrupt 9
B51	BRDY#	Burst Ready
B52	BLAST#	Burst Last
B53	ID0	Identification 0
B54	ID1	Identification 1
B55	GND	Ground
B56	LCLK	Local Clock
B57	VCC	+5 VDC
B58	LBS16#	Local Bus Size 16

Contributor: [Joakim Ögren](#)

Source: " [comp.sys.ibm.pc.hardware.\\* FAQ Part 4](#), maintained by [Ralph Valentino](#)

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# VESA LocalBus (VLB) (technical)

This section is currently based solely on the work by Mark Sokos.

This file is intended to provide a basic functional overview of the Vesa Local Bus, so that hobbyists and amateurs can design their own VLB compatible cards.

It is not intended to provide complete coverage of the VLB standard.

VLB Connectors are usually inline with ISA connectors, so that adapter cards may use both. However, the VLB is separate, and does not need to connect to the ISA portion of the bus.

The 64 bit expansion of the bus (optional) does not add additional pins or connectors. Instead, it multiplexes the existing pins. The 32 bit VLB bus does not use the 64 bit signals shown in the above pinouts.

## Signal Descriptions

### A2-A31

Address Bus

### ADS

Address Strobe

### BE0-BE3

Byte Enable. Indicates that the 8 data lines corresponding to each signal will deliver valid data.

### BLAST

Burst Last. Indicates a VLB Burst Cycle, which will complete with \*BRDY. The VLB Burst cycle consists of an address phase followed by four data phases.

## BRDY

Burst Ready. Indicates the end of the current burst transfer.

## D0-D31

Data Bus. Valid bytes are indicated by \*BE(x) signals.

## D/C

Data/Command. Used with M/IO and W/R to indicate the type of cycle.

M/IO	D/C	W/R	
0	0	0	INTA sequence
0	0	1	Halt/Special (486)
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Instruction Fetch
1	0	1	Halt/Shutdown (386)
1	1	0	Memory Read
1	1	1	Memory Write

## ID0-ID4

Identification Signals.

ID0	ID1	ID4	CPU	Bus Width	Burst
0	0	0	(res)		
0	0	1	(res)		
0	1	0	486	16/32	Burst Possible
0	1	1	486	16/32	Read Burst
1	0	0	386	16/32	None
1	0	1	386	16/32	None
1	1	0	(res)		



1	1	1	486	16/32/64	Read/Write Burst
---	---	---	-----	----------	------------------

ID2 Indicates wait:	0 = 1 wait cycle (min)
	1 = no wait
ID3 Indicates bus speed:	0 = greater than 33.3 MHz
	1 = less than 33.3 MHz

## IRQ9

Interrupt Request. Connected to IRQ9 on ISA bus. This allows standalone VLB adapters (not connected to ISA portion of the bus) to have one IRQ.

## LEADS

Local Enable Address Strobe. Set low by VLB master (not CPU). Also used for cache invalidation signal.

## LBS16

Local Bus Size 16. Used by slave device to indicate that it has a transfer width of only 16 bits.

## LCLK

Local Clock. Runs at the same frequency as the cpu, up to 50 MHz. 66 MHz is allowed for on-board devices.

## LDEV

Local Device: When appropriate address and M/IO signals are present on the bus, the VLB device must pull this line low to indicate that it is a VLB device. The VLB controller will then use the VLB bus for the transfer.

## LRDY

Local Ready. Indicates that the VLB device has completed the cycle. This signal is only used for single

cycle transfers. \*BRDY is used for burst transfers.

## LGNT

Local Grant. Indicates that an \*LREQ signal has been granted, and control is being transferred to the new VLB master.

## LREQ

Local Request. Used by VLB Master to gain control of the bus.

## M/IO

Memory/IO. See D/C for signal description.

## RDYRTN

Ready Return. Indicates VLB cycle has been completed. May precede LRDY by one cycle.

## RESET

Reset. Resets all VLB devices.

## WBACK

Write Back.

# 64-bit Expansion Signals

## ACK64

Acknowledge 64 bit transfer. Indicates that the device can perform the requested 64 bit transfer cycle.

## BE4-BE7

Byte Enable. Indicates which bytes are valid (similar to BE0-BE3).

## D32-D63

Upper 32 bits of data bus. Multiplexed with address bus.

## LBS64

Local Bus Size 64 bits. Used by VLB Master to indicate that it desires a 64 bit transfer.

## W/R

Write/Read. See D/C for signal description.

## 64 Bit Data Transfer Timing Diagram:



Contributor: [Joakim Ögren](#), [Mark Sokos](#)

Source:

[Mark Sokos VLB page](#)

*"The Indispensible PC Hardware Book" by Hans-Peter Messmer, ISBN 0-201-8769-3*

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*Document last modified: 2001-06-08*





# VME64x

**NOT  
DRAWN  
YET...**

(at the network device).

**NOT  
DRAWN  
YET...**

(at the transciever).

160 PIN DIN 41612 (???) FEMALE at the backplane

160 PIN DIN 41612 (???) MALE at the boards.

J=Jack (Backplane), P=Plug (Board)

See [VMEbus](#) for more signals. Only signals changed/added in VME64x are listed below

## P1/J1 (Required)

Pin	Name
z1	MPR
z2	GND
z3	MCLK
z4	GND
z5	MSD
z6	GND
z7	MMD
z8	GND
z9	MCTL
z10	GND
z11	RESP*

z12	GND
z13	RsvBus
z14	GND
z15	RsvBus
z16	GND
z17	RsvBus
z18	GND
z19	RsvBus
z20	GND
z21	RsvBus
z22	GND
z23	RsvBus
z24	GND
z25	RsvBus
z26	GND
z27	RsvBus
z28	GND
z29	RsvBus
z30	GND
z31	RsvBus
z32	GND

b21	SERA
b22	SERB

Pin	Name
d1	VPC
d2	GND
d3	+V1
d4	+V2
d5	RsvU
d6	-V1
d7	-V2

d8	RsvU
d9	GAP*
d10	GA0*
d11	GA1*
d12	+3.3V
d13	GA2*
d14	+3.3V
d15	GA3*
d16	+3.3V
d17	GA4*
d18	+3.3V
d19	RsvBus
d20	+3.3V
d21	RsvBus
d22	+3.3V
d23	RsvBus
d24	+3.3V
d25	RsvBus
d26	+3.3V
d27	LI/I*
d28	+3.3V
d29	LI/O*
d30	+3.3V
d31	GND
d32	VPC

## P2/J2 (Optional)

Pin	Name
z1	UsrDef
z2	GND

z3	UsrDef
z4	GND
z5	UsrDef
z6	GND
z7	UsrDef
z8	GND
z9	UsrDef
z10	GND
z11	UsrDef
z12	GND
z13	UsrDef
z14	GND
z15	UsrDef
z16	GND
z17	UsrDef
z18	GND
z19	UsrDef
z20	GND
z21	UsrDef
z22	GND
z23	UsrDef
z24	GND
z25	UsrDef
z26	GND
z27	UsrDef
z28	GND
z29	UsrDef
z30	GND
z31	UsrDef
z32	GND
b3	RETRY*



Pin	Name
d1	UsrDef
d2	UsrDef
d3	UsrDef
d4	UsrDef
d5	UsrDef
d6	UsrDef
d7	UsrDef
d8	UsrDef
d9	UsrDef
d10	UsrDef
d11	UsrDef
d12	UsrDef
d13	UsrDef
d14	UsrDef
d15	UsrDef
d16	UsrDef
d17	UsrDef
d18	UsrDef
d19	UsrDef
d20	UsrDef
d21	UsrDef
d22	UsrDef
d23	UsrDef
d24	UsrDef
d25	UsrDef
d26	UsrDef
d27	UsrDef
d28	UsrDef
d29	UsrDef
d30	UsrDef

d31	GND
d32	VPC

*\*) Active Low*

*Contributor: [Joakim Ögren](#), [Kevin D. Plymel](#)*

*Source:*  
*[VMEbus Connector Pin Assignment](#) at [VITA's VMEbus FAQ](#)*

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# VME64x (technical)

## Signal Descriptions:

### A01 - A31

Address lines [A01 - A31] carry a binary address.

### AM0 - AM5

The address modifier code [AM0 - AM5] is a 'tag' that indicates the type of VMEbus cycle in progress.

### BG0IN\* - BG3IN\*

### BG0OUT\* - BG3OUT\*

The bus grant signals [BG0IN\* - BG3IN\* and BG0OUT\* - BG3OUT\*] are part of the bus grant daisy chain and are driven by arbiters and requesters. The slot 01 arbiter asserts a bus grant in response to a bus request on the same level [BR0\* - BR3\*]. The bus grant daisy-chain starts at the slot 01 system controller and propagates from module to module until it reaches the module that initially requested the bus. Each VMEbus module has a bus grant input and a bus grant output. They are standard totem-pole class signals.

### BR0\* - BR3\*

Bus requests [BR0\* - BR3\*] are asserted by a requester whenever its master or interrupt handler needs the bus. Before accepting the bus, the master waits until the arbiter grants the bus by way of the bus grant daisy-chain [BG0IN\* - BG3IN\*]. They are open-collector class signals.

### D00-D31

Data bus [D00-D31] is driven by masters, slaves or interrupters. These are bi-directional signals and are used for data transfers. Different portions of the data bus are used depending upon the state of DS0\*, DS1\*, A01 and LWORD\* pins. They are standard three-state signals. The data lines can also be used to transfer a portion of the address during MD32, MBLT and 2eVME cycles.

## DS0\*, DS1\*

Data strobes DS0\* and DS1\* are driven by masters and interrupt handlers. These signals serve not only to qualify data, but also to indicate the size and position of the data transfer. When combined with LWORD\* and A01, the data strobes indicate the size and type of data transfer. DS0\* - DS1\* are high current three-state class signals.

## DTACK\*

Data transfer acknowledge [DTACK\*] is driven by slaves or interrupters. During write cycles DTACK\* is asserted by a slave after it has latched data. During read and interrupt acknowledge cycles, DTACK\* is asserted by a slave after data is placed onto the bus. DTACK\* can be an open-collector or a high current three-state class signal.

## GA0\* - GA4\*

The geographical address [GA0\*-GA4\*] is a binary code that indicates the slot number of the backplane. They are open collector signals, and were added to the 160 pin P1/J1 connector in the VME64x specification.

## GAP\*

The geographical address parity [GAP\*] is tied high or floating, depending upon the parity of the geographical address lines [GA0\*-GA4\*]. It is an open collector signal, and was added to the 160 pin P1/J1 connector in the VME64x specification.

## GND

Ground [GND] is used both as a signal reference and a power return path.

## IACK\*

Interrupt acknowledge [IACK\*] is driven by interrupt handlers in response to interrupt requests. It is connected to IACKIN\* at slot 01 (on the backplane), and used by the IACK\* daisy-chain driver to start propagation of the [IACKIN\* - IACKOUT\*] daisy-chain. IACK\* can be either an open-collector or a standard three-state class signal.

## IACKIN\*, IACKOUT\*



The interrupt acknowledge daisy chain [IACKIN\* - IACKOUT\*] is driven by the IACK\* daisy-chain driver. These signals are used both to indicate that an interrupt acknowledge cycle is in progress, and to determine which interrupters should return a STATUS/ID. They are standard totem-pole class signals.

## **IRQ1\*-IRQ7\***

Priority interrupt requests [IRQ1\*-IRQ7\*] are asserted by interrupters. Level seven is the high-est priority, and level one the lowest. They are open-collector class signals.

## **LI/I\***

The live insertion input [LI/I\*] signal is used to carry hot swap (live insertion) control information. It is a three state driven signal and was added to the 160 pin P1/J1 connector in the VME64x specification.

## **LI/O\***

The live insertion output [LI/O\*] signal is used to carry hot swap (live insertion) control information. It is a three state driven signal and was added to the 160 pin P1/J1 connector in the VME64x specification.

## **LWORD\***

Long word [LWORD\*] is driven by masters. It is used in conjunction with A01, DS0\* and DS1\* to indicate the size of the current data transfer. LWORD\* is a standard three-state class signal. During 64-bit address transfers, LWORD\* doubles as address bit A00. During 64-bit data transfers, LWORD\* doubles as a data bit.

## **MCLK, MCTL, MMD, MPR, MSD**

These signals are part of the IEEE 1149.5 MTM bus. They are three-state driven signals which was added to the 160 pin P1/J1 connector in the VME64x specification.

## **RESERVED**

The RESERVED signal pin is obsolete and is no longer used. Under the IEEE 1014-1987 version of the bus specification there was a single reserved pin. This pin was redefined under VME64 as the RETRY\* pin. The VME64x specification uses the names RsvB and RsvU for reserved pins.

## **RESP\***

The response [RESP\*] signal is used to carry the information as defined by the 2eVME protocol. It was added to the 160 pin P1/J1 connector in the VME64x specification.

## RsvB

The reserved/bused [RsvB] signal should not be used. VME64x backplanes must bus and terminate this signal. It was added to the 160 pin P1/J1 connector in the VME64x specification.

## RsvU

The reserved/unbused [RsvU] signal should not be used. VME64x backplanes must not bus or terminate this signal. It was added to the 160 pin P1/J1 connector in the VME64x specification.

## RETRY\*

[RETRY\*], together with [BERR\*], can be asserted by a slave to postpone a data transfer. The master must then attempt the cycle again at a later time. The retry cycle prevents deadlock (deadly embrace) conditions in bus-to-bus links and secondary buses. RETRY\* is a standard three-state signal. The [RETRY\*] signal was added in the ANSI/VITA 1-1994 (VME64) version of the bus specification. This pin was RESERVED in earlier versions. However, boards that support [RETRY\*] should work just fine with older backplanes, as they were required to bus and terminate this signal line.

## SERA, SERB

The [SERA] and [SERB] signals are used for an (optional) serial bus such as the AUTOBAHN (IEEE 1394) or VMSbus. Under the ANSI/VITA 1-1994 (VME64) bus specification, these pins can be used for any user defined serial bus. Earlier versions of the VMEbus specification defined these pins as [SERCLK] and [SERDAT\*], which were originally intended for a serial bus called VMSbus. However, they were rarely used for that purpose.

## SERCLK, SERDAT\*

The [SERCLK] and [SERDAT\*] signals were made obsolete under the ANSI/VITA 1-1994 (VME64) bus specification. Refer to [SERA] and [SERB] for more details.

## SYSCLK

16 MHz utility clock [SYSCLK] is driven by the slot 01 system controller. This clock can be used for any purpose, and has no timing relationship to other VMEbus signals. SYSCLK\* is a high current totem-pole class signal.

## **SYSFAIL\***

System fail [SYSFAIL\*] can be asserted or monitored by any module. It indicates that a failure has occurred in the system. Implementation of [SYSFAIL\*] is user de-fined, and its use is optional. SYSFAIL\* is an open-collector class signal.

## **SYSRESET\***

System reset [SYSRESET\*] can be driven by any module and indicates that a reset (such as power-up) is in progress. SYSRESET\* is an open-collector class signal.

## **UsrDef, UD**

Pins that are user defined [specified as 'UsrDef' or 'UD'] can be specified by the user. Generally, they are routed directly through the backplane so that they can be connected to cables or to rear I/O transition modules.

## **VPC**

Voltage pre-charge [VPC] pins forma a 'make first / break last' contact. They are intended to be used as pre-charge power sources for live insertion logic. These pins were added to the 160 pin P1/J1 and P2/J2 connectors in the VME64x specification. The VPC pins are connected to the +5 VDC power supply on VME64x backplanes. These pins may also be used as additional +5 VDC power pins in boards that do not support live insertion.

## **+V1, -V1, +V2, -V2**

The [+/- V1/V2] power pins supply 38 - 75 VDC to the bus module. They are also known as the auxiliary power pins, and were originally intended to be used as 48 VDC battery supplies in Telecom systems. However, they can be used for any purpose. These pins were added to the 160 pin P1/J1 connector in the VME64x specification.

## **WRITE\***

The read / write signal [WRITE\*] is driven by masters. It indicates the direction of data transfer over the bus. It is asserted during a write cycle and negated during a read cycle. WRITE\* is a stan-dard three-state class signal.

## **+5V STDBY**



[+5V STDBY] is an optional +5 VDC standby power supply. This power pin is often connected to a rechargeable battery. This eliminates the need for individual batteries on VMEbus modules. Individual batteries are often used for real time clock and static RAM chips.

## **+3.3 V**

Main +3.3 VDC power source. These pins were added to the 160 pin P1/J1 connector in the VME64x specification.

## **+5 VDC**

## **+12 VDC, -12 VDC**

The main system power supplies are [+5 VDC], [+12 VDC] and [-12 VDC].

*Contributor:* [Joakim Ögren](#), [Kevin D. Plymel](#)

*Source:*

[VMEbus Connector Pin Assignment](#) at [VITA's VMEbus FAQ](#)

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# VMEbus

**NOT  
DRAWN  
YET...**



(at the network device).

**NOT  
DRAWN  
YET...**



(at the transciever).

96 PIN DIN 41612 FEMALE at the backplane

96 PIN DIN 41612 MALE at the boards.

J=Jack (Backplane), P=Plug (Board)

## P1/J1 (Required)

Pin	Name
a1	D00
a2	D01
a3	D02
a4	D03
a5	D04
a6	D05
a7	D06
a8	D07
a9	GROUND
a10	SYSCLK
a11	GROUND
a12	DS1*

a13	DS0*
a14	WRITE*
a15	GROUND
a16	DTACK*
a17	GROUND
a18	AS*
a19	GROUND
a20	IACK*
a21	IACKIN*
a22	IACKOUT*
a23	AM4
a24	A07
a25	A06
a26	A05
a27	A04
a28	A03
a29	A02
a30	A01
a31	-12V
a32	+5V

Pin	Name
b1	BBSY*
b2	BCLR*
b3	ACFAIL*
b4	BG0IN*
b5	BG0OUT*
b6	BG1IN*
b7	BG1OUT*
b8	BG2IN*
b9	BG2OUT*
b10	BG3IN*

b11	BG3OUT*
b12	BR0*
b13	BR1*
b14	BR2*
b15	BR3*
b16	AM0
b17	AM1
b18	AM2
b19	AM3
b20	GROUND
b21	SERCLK*
b22	SERDAT*
b23	GROUND
b24	IRQ7*
b25	IRQ6*
b26	IRQ5*
b27	IRQ4*
b28	IRQ3*
b29	IRQ2*
b30	IRQ1*
b31	+5V STDBY
b32	+5V

Pin	Name
c1	D08
c2	D09
c3	D10
c4	D11
c5	D12
c6	D13
c7	D14
c8	D15

c9	GROUND
c10	SYSFAIL*
c11	BERR*
c12	SYSRESET*
c13	LWORD*
c14	AM5
c15	A23
c16	A22
c17	A21
c18	A20
c19	A19
c20	A18
c21	A17
c22	A16
c23	A15
c24	A14
c25	A13
c26	A12
c27	A11
c28	A10
c29	A09
c30	A08
c31	+12V
c32	+5V

## P2/J2 (Optional)

Pin	Name
b1	+5v
b2	GROUND
b3	RESERVED



b4	A24
b5	A25
b6	A26
b7	A27
b8	A28
b9	A29
b10	A30
b11	A31
b12	GROUND
b13	+5V
b14	D16
b15	D17
b16	D18
b17	D19
b18	D20
b19	D21
b20	D22
b21	D23
b22	GROUND
b23	D24
b24	D25
b25	D26
b26	D27
b27	D28
b28	D29
b29	D30
b30	D31
b31	GROUND
b32	+5V

\*) *Active Low*

*Contributor: [Joakim Ögren](#), [Kevin D. Plymel](#), And many more!*

*Source:*

*[VMEbus Connector Pin Assignment](#) at [VITA's VMEbus FAQ](#)  
[comp.arch.bus.vmebus FAQ](#) by Robert J. Boys*

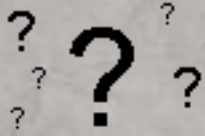
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# Zorro II



(at the A2000)

86 PIN EDGE CONNECTOR at the A2000.

Pin	A500	A1000	A2000	A2000B	Name	Description
1	X	X	X	X	GND	Ground
2	X	X	X	X	GND	Ground
3	X	X	X	X	GND	Ground
4	X	X	X	X	GND	Ground
5	X	X	X	X	+5V	+5 Volts DC
6	X	X	X	X	+5V	+5 Volts DC
7	X	X	X	X	n/c	
8	X	X	X	X	-5V	-5 Volts DC
9	X	X			n/c	
			X	X	28CLOCK	28MHz Clock
10	X	X	X	X	+12V	+12 Volts DC
11	X	X			n/c	
			X	X	/COPCFG	Configuration Out
12	X	X	X	X	CONFIG IN, Grounded	
13	X	X	X	X	GND	Ground
14	X	X	X	X	/C3	C3 Clock
15	X	X	X	X	CDAC	Clock
16	X	X	X	X	/C1	C1 Clock
17	X	X	X	X	/OVR	
18	X	X	X	X	RDY	Ready

19	X	X	X	X	/INT2	Interrupt 2
20	X	X			/PALOPE	
			X		n/c	
				X	/BOSS	
21	X	X	X	X	A5	Address 5
22	X	X	X	X	/INT6	Interrupt 6
23	X	X	X	X	A6	Address 6
24	X	X	X	X	A4	Address 4
25	X	X	X	X	GND	Ground
26	X	X	X	X	A3	Address 3
27	X	X	X	X	A2	Address 2
28	X	X	X	X	A7	Address 7
29	X	X	X	X	A1	Address 1
30	X	X	X	X	A8	Address 8
31	X	X	X	X	FC0	Processor status 0
32	X	X	X	X	A9	Address 9
33	X	X	X	X	FC1	Processor status 1
34	X	X	X	X	A10	Address 10
35	X	X	X	X	FC2	Processor status 2
36	X	X	X	X	A11	Address 11
37	X	X	X	X	GND	Ground
38	X	X	X	X	A12	Address 12
39	X	X	X	X	A13	Address 13
40	X	X	X	X	/IPL0	
41	X	X	X	X	A14	Address 14
42	X	X	X	X	/IPL1	
43	X	X	X	X	A15	Address 15
44	X	X	X	X	/IPL2	
45	X	X	X	X	A16	Address 16
46	X	X	X	X	/BEER	Bus Error
47	X	X	X	X	A17	Address
48	X	X	X	X	/VPA	



49	X	X	X	X	GND	Ground
50	X	X	X	X	ECLK	E Clock
51	X	X	X	X	/VMA	
52	X	X	X	X	A18	Address 18
53	X	X	X	X	RST	Reset
54	X	X	X	X	A19	Address 19
55	X	X	X	X	/HLT	Halt
56	X	X	X	X	A20	Address 20
57	X	X	X	X	A22	Address 22
58	X	X	X	X	A21	Address 21
59	X	X	X	X	A23	Address 23
60	X	X			/BR	
			X	X	/CBR	
61	X	X	X	X	GND	Ground
62	X	X	X	X	/BGACK	
63	X	X	X	X	D15	Data 15
64	X	X			/BG	
			X	X	/CBG	
65	X	X	X	X	D14	Data 14
66	X	X	X	X	/DTACK	
67	X	X	X	X	D13	Data 13
68	X	X	X	X	R/W	Read/Write
69	X	X	X	X	D12	Data 12
70	X	X	X	X	/LDS	
71	X	X	X	X	D11	Data 11
72	X	X	X	X	/UDS	
73	X	X	X	X	GND	Ground
74	X	X	X	X	/AS	
75	X	X	X	X	D0	Data 0
76	X	X	X	X	D10	Data 10
77	X	X	X	X	D1	Data 1
78	X	X	X	X	D9	Data 9

79	X	X	X	X	D2	Data 2
80	X	X	X	X	D8	Data 8
81	X	X	X	X	D3	Data 3
82	X	X	X	X	D7	Data 7
83	X	X	X	X	D4	Data 4
84	X	X	X	X	D6	Data 6
85	X	X	X	X	GND	Ground
86	X	X	X	X	D5	Data 5

Contributor: [Joakim Ögren](#)

Source:

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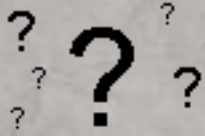
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# Zorro II/III



(at the computer)

100 PIN EDGE CONNECTOR at the computer.

Pin	Physical Name	Zorro II Name	Zorro III Address Phase	Zorro III Data Phase
1	Ground	Ground	Ground	Ground
2	Ground	Ground	Ground	Ground
3	Ground	Ground	Ground	Ground
4	Ground	Ground	Ground	Ground
5	+5VDC	+5VDC	+5VDC	+5VDC
6	+5VDC	+5VDC	+5VDC	+5VDC
7	/OWN	/OWN	/OWN	/OWN
8	-5VDC	-5VDC	-5VDC	-5VDC
9	/SLAVEn	/SLAVEn	/SLAVEn	/SLAVEn
10	+12VDC	+12VDC	+12VDC	+12VDC
11	/CFGOUTn	/CFGOUTn	/CFGOUTn	/CFGOUTn
12	/CFGINn	/CFGINn	/CFGINn	/CFGINn
13	Ground	Ground	Ground	Ground
14	/C3	/C3 Clock	/C3 Clock	/C3 Clock
15	CDAC	CDAC Clock	CDAC Clock	CDAC Clock
16	/C1	/C1 Clock	/C1 Clock	/C1 Clock
17	/CINH	/OVR	/CINH	/CINH
18	/MTCR	XRDY	/MTCR	/MTCR
19	/INT2	/INT2	/INT2	/INT2

20	-12VDC	-12VDC	-12VDC	-12VDC
21	A5	A5	A5	A5
22	/INT6	/INT6	/INT6	/INT6
23	A6	A6	A6	A6
24	A4	A4	A4	A4
25	Ground	Ground	Ground	Ground
26	A3	A3	A3	A3
27	A2	A2	A2	A2
28	A7	A7	A7	A7
29	/LOCK	A1	/LOCK	/LOCK
30	AD8	A8	A8	D0
31	FC0	FC0	FC0	FC0
32	AD9	A9	A9	D1
33	FC1	FC1	FC1	FC1
34	AD10	A10	A10	D2
35	FC2	FC2	FC2	FC2
36	AD11	A11	A11	D3
37	Ground	Ground	Ground	Ground
38	AD12	A12	A12	D4
39	AD13	A13	A13	D5
40	Reserved	(/EINT7)	Reserved	Reserved
41	AD14	A14	A14	D6
42	Reserved	(/EINT5)	Reserved	Reserved
43	AD15	A15	A15	D7
44	Reserved	(/EINT4)	Reserved	Reserved
45	AD16	A16	A16	D8
46	/BERR	/BERR	/BERR	/BERR
47	AD17	A17	A17	D9
48	/MTACK	(/VPA)	/MTACK	/MTACK
49	Ground	Ground	Ground	Ground
50	E Clock	E Clock	E Clock	E Clock
51	/DS0	(/VMA)	/DS0	/DS0



52	AD18	A18	A18	D10
53	/RESET	/RST	/RESET	/RESET
54	AD19	A19	A19	D11
55	/HLT	/HLT	/HLT	/HLT
56	AD20	A20	A20	D12
57	AD22	A22	A22	D14
58	AD21	A21	A21	D13
59	AD23	A23	A23	D15
60	/BRn	/BRn	/BRn	/BRn
61	Ground	Ground	Ground	Ground
62	/BGACK	/BGACK	/BGACK	/BGACK
63	AD31	D15	A31	D31
64	/BGn	/BGn	/BGn	/BGn
65	AD30	D14	A30	D30
66	/DTACK	/DTACK	/DTACK	/DTACK
67	AD29	D13	A29	D29
68	READ	READ	READ	READ
69	AD28	D12	A28	D28
70	/DS2	/LDS	/DS2	/DS2
71	AD27	D11	A27	D27
72	/DS3	/UDS	/DS3	/DS3
73	Ground	Ground	Ground	Ground
74	/CCS	/AS	/CCS	/CCS
75	SD0	D0	Reserved	D16
76	AD26	D10	A26	D26
77	SD1	D1	Reserved	D17
78	AD25	D9	A25	D25
79	SD2	D2	Reserved	D18
80	AD24	D8	A24	D24
81	SD3	D3	Reserved	D19
82	SD7	D7	Reserved	D23
83	SD4	D4	Reserved	D20

84	SD6	D6	Reserved	D22
85	Ground	Ground	Ground	Ground
86	SD5	D5	Reserved	D21
87	Ground	Ground	Ground	Ground
88	Ground	Ground	Ground	Ground
89	Ground	Ground	Ground	Ground
90	Ground	Ground	Ground	Ground
91	SenseZ3	Ground	SenseZ3	SenseZ3
92	7M	E7M	7M	7M
93	DOE	DOE	DOE	DOE
94	/IORST	/BUSRST	/IORST	/IORST
95	/BCLR	/GBG	/BCLR	/BCLR
96	Reserved	(/EINT1)	Reserved	Reserved
97	/FCS	No Connect	/FCS	/FCS
98	/DS1	No Connect	/DS1	/DS1
99	Ground	Ground	Ground	Ground
100	Ground	Ground	Ground	Ground

Contributor: [Joakim Ögren](#)

Source:  
*Amiga 4000 User's Guide from Commodore*

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# Apple Digital Audio/Video (DAV)

## 60 PIN UNKNOWN CONNECTOR

The Audio/Video Input/Output Card has a separate connector called the DAV (digital audio video) connector. The DAV connector provides access to the Audio/Video card's 4:2:2 unscaled YUV video input data bus and associated control signals. By means of a 60-pin cable to the DAV connector, a PCI expansion card can gain access to the digital video bus on the Audio/Video Input/Output Card and use it to transfer real-time video data to the computer. Such a PCI expansion card can contain a hardware video compressor or other video processor.

The DAV connector accepts YUV video and analog sound from the PCI expansion card.

The 60-pin DAV connector is located at the top edge of the Audio/Video Input/Output Card. A PCI expansion card that uses the DAV interface can be connected to the Audio/Video Input/Output Card with a 7-inch 60-conductor flat-ribbon cable.

Pin	Description
1	Ground
2	Reserved (or GeoPort Clock)
3	Ground
4	Reserved (or LLC_OUT)
5	Ground
6	Reserved (or PXQ_OUT)
7	Ground
8	Reserved (or VS_OUT)
9	Ground
10	Reserved (or HS_OUT)
11	UV bit 7
12	UV bit 6
13	UV bit 5
14	UV bit 4

15	UV bit 3
16	UV bit 2
17	UV bit 1
18	UV bit 0
19	Y bit 7
20	Y bit 6
21	Y bit 5
22	Y bit 4
23	Y bit 3
24	Y bit 2
25	Y bit 1
26	Y bit 0
27	Ground
28	Line-locked clock (LLC) in
29	Ground
30	Clock reference qualifier (PXQ) In
31	Ground
32	Vertical sync (VS) In
33	Ground
34	Reserved (or Horizontal Sync (HS) In)
35	Ground
36	HRef In
37	Ground
38	DIR * (or FLD)
39	IIC Data *
40	IIC Clock
41	Ground
42	Analog audio input left
43	Analog audio input common
44	Analog audio input right
45	Ground
46	Digital audio input



47	Ground
48	Digital audio output
49	Ground
50	Digital audio clock
51	Ground
52	Digital audio sync
53	Ground
54	S video input C component
55	Video input ground
56	S video input Y component
57	Video input ground
58	Reserved
59	Reserved
60	Reserved

Contributor: [Joakim Ögren](#)

Source:  
[Apple Tech Info Library 18547: Power Macintosh 7200, 7500, 8500, 9500 Pinouts](#) at [Apple TIL homepage](#)

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# Apple Digital Video Application (DVA)

## 34 PIN UNKNOWN CONNECTOR

DVA is somewhat similar to the Digital Audio/Video connector

Available on Apple Macintosh LC 630 / Quadra 630

Pin	Description
1	Y bit 7
2	Y bit 6
3	Y bit 5
4	Y bit 4
5	Y bit 3
6	Y bit 2
7	Y bit 1
8	Y bit 0
9	UV bit 7
10	UV bit 6
11	UV bit 5
12	UV bit 4
13	UV bit 3
14	UV bit 2
15	UV bit 1
16	UV bit 0
17	Ground
18	Line-locked clock (LLC) in
19	Ground
20	Clock reference (CREF) in

21	Ground
22	Vertical sync (VS) In
23	Ground
24	Horizontal Sync (HS) In
25	Ground
26	Horizontal Reference Signal (HREF) In
27	Ground
28	YUV Direction Signal (DIR)
29	Ground
30	Reserved
31	Ground
32	Analog audio input left
33	Analog audio input common
34	Analog audio input right

Contributor: [Joakim Ögren](#)

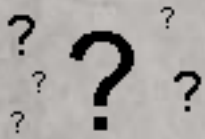
Source:  
*Apple Macintosh LC 630 / Quadra 630 Developer Note*

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# +4 User Port

Available on Commodore +4 computer.



(at the Computer)

UNKNOWN CONNECTOR at the Computer.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 VDC
3	/BRESET	?
4	P2/CSE	Data 2/Cassette Sense
5	P3	Data 3
6	P4	Data 4
7	P5	Data 5
8	RxC	Receive Clock
9	ATN	Attention?
10	+9V	+9 VAC
11	+9V	+9 VAC
12	GND	Ground
A	GND	Ground
B	P0	Data 0
C	RxD	Receive Data
D	RTS	Request to Send
E	DTR	Data Terminal Ready
F	P7	Data 7



G	DCD	Data Carrier Detect
H	P6	Data 6
I	CTS	Clear to Send
J	DSR	Data Set Ready
K	TxD	Transmit Data
L	GND	Ground

*Contributor:* [Joakim Ögren](#), [Arwin Vosselman](#)

*Sources:*

*Usenet posting in comp.sys.cbm, [Pinout specs for cbm machines needed](#) by [Lonnie McClure](#)*

*SAMS Computerfacts CC8 Commodore 16*

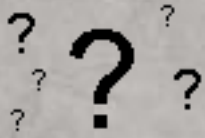
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# Amiga 1000 Ramex



(at the computer)

60 PIN EDGE CONNECTOR (.156") at the computer.

Pin	Name	Description
1	GND	Ground
2	D15	Data 15
3	+5V	+5 Volts DC
4	D12	Data 12
5	GND	Ground
6	D11	Data 11
7	+5V	+5 Volts DC
8	D8	Data 8
9	GND	Ground
10	D7	Data 7
11	+5V	+5 Volts DC
12	D4	Data 4
13	GND	Ground
14	D3	Data 3
15	+5V	+5 Volts DC
16	D0	Data 0
17	GND	Ground
18	DRA4	
19	DRA5	
20	DRA6	

21	DRA7	
22	GND	Ground
23	/RAS	
24	GND	Ground
25	GND	Ground
26	/CASU0	
27	GND	Ground
28	/CASL0	
29	+5V	+5 Volts DC
30	+5V	+5 Volts DC
A	GND	Ground
B	D14	Data 14
C	+5V	+5 Volts DC
D	D13	Data 13
E	GND	Ground
F	D10	Data 10
H	+5V	+5 Volts DC
J	D9	Data 9
K	GND	Ground
L	D6	Data 6
M	+5V	+5 Volts DC
N	D5	Data 5
P	GND	Ground
R	D2	Data 2
S	+5V	+5 Volts DC
T	D1	Data 1
U	GND	Ground
V	DRA3	
W	DRA2	
X	DRA1	
Y	DRA0	

Z	GND	Ground
AA	/RRW	
BB	GND	Ground
CC	GND	Ground
DD	/CASU1	
EE	GND	Ground
FF	/CASL1	
HH	+5V	+5 Volts DC
JJ	+5V	+5 Volts DC

Contributor: [Joakim Ögren](#)

Source:  
?

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# Apple Communication Slot

## 112 PIN UNKNOWN CONNECTOR

Available on:

Apple Macintosh 575 family  
 Apple Macintosh 630 family  
 Apple Macintosh 5200 family  
 Apple Macintosh 5300 family  
 Apple Performa 6200CD series  
 Apple Performa 6300 series

Pin	Name	Description
1	Audio MODEM to Host	
2	Audio Host to MODEM	
3	Audio MH GND	
4	MIC to MODEM	
5	R/W*	
6	DS*	
7	BERR*	
8	DSACK1*	
9	DSACK0*	
10	GND	
11	IOSIZE0*	
12	C16M	
13	IOSIZE1*	
14	GND	
15	RESET*	
16	Bus Grant-Sacramento	
17	IOD[31]	
18	IOD[30]	

19	IOD[29]
20	IOD[28]
21	IOD[27]
22	IOD[26]
23	IOD[25]
24	IOD[24]
25	IOD[23]
26	IOD[22]
27	+5V
28	IOD[21]
29	IOD[20]
30	IOD[19]
31	IOD[18]
32	IOD[17]
33	IOD[16]
34	IOD[15]
35	IOD[14]
36	IOD[13]
37	IOD[12]
38	IOD[11]
39	IOD[10]
40	IOD[9]
41	IOD[8]
42	GND
43	IOD[7]
44	IOD[6]
45	IOD[5]
46	IOD[4]
47	IOD[3]
48	IOD[2]
49	IOD[1]
50	IOD[0]

51	BGACK*
52	Bus Request-Sacramento
53	IO_CS_TIMED*
54	IO_CS_DSACK*
55	+5V
56	Sacramento IRQ*
57	IOA[1]
58	IOA[0]
59	A[2]
60	A[3]
61	A[4]
62	A[5]
63	A[6]
64	A[7]
65	A[8]
66	A[9]
67	A[10]
68	A[11]
69	A[12]
70	GND
71	A[13]
72	A[14]
73	A[15]
74	A[16]
75	A[17]
76	A[18]
77	A[19]
78	A[20]
79	A[21]
80	A[22]
81	A[23]
82	A[24]

83	+5V
84	A[25]
85	A[26]
86	A[27]
87	A[28]
88	A[29]
89	A[30]
90	A[31]
91	CPU_AS*
92	GND
93	TRICKLE+5V
94	System wakeup
95	'040 bus clock
96	-5V
97	+12V
98	GND
99	spare
100	C32M
101	spare
102	GND
103	spare
104	spare
105	SCC port A enable
106	spare
107	TxDA
108	RxDA
109	RTSA*
110	CTSA*
111	DTRA*
112	DCDA*

*Note: \* = active low signal*



*Contributor:* [Joakim Ögren](#)

*Source:*

[Apple Tech Info Library 15081: Communication Slot Specifications](#) at [Apple TIL homepage](#)

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# Apple Macintosh Portable ROM Expansion

## 50 PIN UNKNOWN CONNECTOR

Pin	Name	Description
1	+5V	+5 VDC
2	A1	Address bit 1
3	A2	Address bit 2
4	A3	Address bit 3
5	A4	Address bit 4
6	A5	Address bit 5
7	A6	Address bit 6
8	A7	Address bit 7
9	A8	Address bit 8
10	A9	Address bit 9
11	A10	Address bit 10
12	A11	Address bit 11
13	A12	Address bit 12
14	A13	Address bit 13
15	A14	Address bit 14
16	A15	Address bit 15
17	A16	Address bit 16
18	A17	Address bit 17
19	A18	Address bit 18
20	A19	Address bit 19
21	A20	Address bit 20
22	A21	Address bit 21

23	A22	Address bit 22
24	A23	Address bit 23
25	GND	Ground
26	GND	Ground
27	/DTACK	Data Transfer Acknowledge
28	/AS	Address Strobe
29	/ROM_CS	ROM Chip Select
30	16M	16 MHz Clock
31	/EXT_DTACK	External Data Transfer Acknowledge
32	/DELAY_CS	
33	D0	Data bit 0
34	D1	Data bit 1
35	D2	Data bit 2
36	D3	Data bit 3
37	D4	Data bit 4
38	D5	Data bit 5
39	D6	Data bit 6
40	D7	Data bit 7
41	D8	Data bit 8
42	D9	Data bit 9
43	D10	Data bit 10
44	D11	Data bit 11
45	D12	Data bit 12
46	D13	Data bit 13
47	D14	Data bit 14
48	D15	Data bit 15
49	+5V	+5 VDC
50	+5V	+5 VDC

## D0-D15

Unbuffered data bus, bits 0 through 15

# A1-A23

Unbuffered 68HC000 address bus, bits 1 through 23

# 16M

16 MHz system clock

# /EXT.DTACK

External data transfer acknowledge that disables main system /DTACK.

# /AS

68HC000 Address strobe

# /DTACK

Data transfer acknowledge, /DTACK input to 68HC000.

# /DELAY\_CS

This signal is generated by the addressing PAL and is used to put the ROM board into the idle mode by inserting multiple wait states.

# /ROM\_CS

Permanent ROM chip select signal. Selects in range \$90 0000 through \$9F FFFF.

*Contributor:* [Joakim Ögren](#)

*Source:*

[Technote HW13: Macintosh Portable ROM Expansion](#) at [Apple Technical Notes](#)

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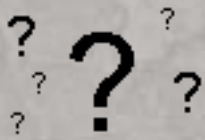


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# Atari 2600 Cartridge

Top											
D3	D4	D5	D6	D7	A12	A10	A11	A9	A8	+5V	SGND
--1--	--2--	--3--	--4--	--5--	--6--	--7--	--8--	--9--	--10--	--11--	--12--
GND	D2	D1	D0	A0	A1	A2	A3	A4	A5	A6	A7
Bottom											



(at the Atari)

UNKNOWN CONNECTOR at the Atari.

Connect a 2716 or 2732/2532 EPROM.

## Top Row

Pin	2716 Pin	CPU Name	Description
1	13	D3	Data 3
2	14	D4	Data 4
3	15	D5	Data 5
4	16	D6	Data 6
5	17	D7	Data 7
6	*	A12	Address 12
7	19	A10	Address 10
8	n/c	A11	Address 11
9	22	A9	Address 9
10	23	A8	Address 8
11	24	+5V	+5 VDC

12	12	SGND	Shield Ground
----	----	------	---------------

\* to inverter and back to 18 for chip select

## Bottom Row

Pin	2716 Pin	CPU Name	Description
1	1	A7	Address 7
2	2	A6	Address 6
3	3	A5	Address 5
4	4	A4	Address 4
5	5	A3	Address 3
6	6	A2	Address 2
7	7	A1	Address 1
8	8	A0	Address 0
9	9	D0	Data 0
10	10	D1	Data 1
11	11	D2	Data 2
12	n/c	GND	Ground

Contributor: [Joakim Ögren](#)

Source:

*Classic Atari 2600/5200/7800 Game Systems FAQ*

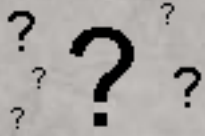
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# Atari 5200 Cartridge



(at the Atari)

UNKNOWN CONNECTOR at the Atari.

Pin	Name
1	D0
2	D1
3	D2
4	D3
5	D4
6	D5
7	D6
8	D7
9	Enable 80-8F
10	Enable 40-7F
11	Not Connected
12	Ground
13	Ground
14	Ground (System Clock 02 on 2 port)
15	A6
16	A5
17	A2
18	Interlock
19	A0
20	A1



21	A3
22	A4
23	Ground
24	Ground (Video In on 2 port)
25	Ground
26	+5 VDC
27	A7
28	Not Connected
29	A8
30	Audio In (2 port)
31	A9
32	A13
33	A10
34	A12
35	A11
36	Interlock

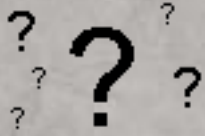
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# Atari 5200 Expansion



(at the Atari)

UNKNOWN CONNECTOR at the Atari.

Pin	Name
1	+5 VDC
2	Audio Out (2 port)
3	Ground
4	R/W Early
5	Enable E0-EF
6	D6
7	D4
8	D2
9	D0
10	IRQ
11	Ground
12	Serial Data In
13	Serial In Clock
14	Serial Out Clock
15	Serial Data Out
16	Audio In
17	A14
18	System Clock 01
19	A11
20	A7

21	A6
22	A5
23	A4
24	A3
25	A2
26	A1
27	A0
28	Ground
29	D1
30	D3
31	D5
32	D7
33	Not connected
34	Ground
35	Not connected
36	+5 VDC

Contributor: [Joakim Ögren](#)

Source:  
*Classic Atari 2600/5200/7800 Game Systems FAQ*

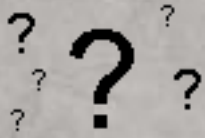
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# Atari 7800 Cartridge



(at the Atari)

UNKNOWN CONNECTOR at the Atari.

Pin	Name	Description
1	R/W	Read/Write
2	HALT	Halt
3	D3	Data 3
4	D4	Data 4
5	D5	Data 5
6	D6	Data 6
7	D7	Data 7
8	A12	Address 12
9	A10	Address 10
10	A11	Address 11
11	A9	Address 9
12	A8	Address 8
13	+5V	+5 VDC
14	GND	Ground
15	A13	Address 13
16	A14	Address 14
17	A15	Address 15
18	EAUDIO	EAudio ???
19	A7	Address 7
20	A6	Address 6



21	A5	Address 5
22	A4	Address 4
23	A3	Address 3
24	A2	Address 2
25	A1	Address 1
26	A0	Address 0
27	D0	Data 0
28	D1	Data 1
29	D2	Data 2
30	Gnd	Gnd
31	IRQ	Interrupt
32	CLK2	Clock 2 ???

Contributor: [Joakim Ögren](#)

Source:

*Classic Atari 2600/5200/7800 Game Systems FAQ*

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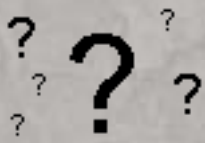
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# Atari 7800 Expansion

Gnd	+5v	CVideo	MLum0	MLum3	Blank	OscDis	ExtMen	Gnd
--1--	--2--	--3--	--4--	--5--	--6--	--7--	--8--	--9--
-18--	-17--	-16--	-15--	-14--	-13--	-12--	-11--	-10--
Gnd	Audio	Rdy	MCol	MLum2	MLum1	Msync	Clk2	ExtOsc



(at the Atari)

UNKNOWN CONNECTOR at the Atari.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 VDC
3	CVIDEO	Input to RF modulator (Video+Audio)
4	MLUM0	Maria Luminance Bit 0
5	MLUM3	Maria Luminance Bit 3
6	BLANK	Blanking output
7	OSCDIS	Disable 14.31818 MHz Master Clock
8	EXTMEN	External Maria Enable Input
9	GND	Ground
10	EXTOSC	External clock to replace Master Clock
11	CLK2	Phase 2 Clock from the 6502
12	MSYNC	Maria Composite Sync
13	MLUM1	Maria Luminance Bit 1
14	MLUM2	Maria Luminance Bit 2
15	MCOL	Maria Color Phase Angle

16	RDY	Input to the 6502
17	AUDIO	Audio
18	GND	Ground

*Contributor:* [Joakim Ögren](#)

*Source:*

*Classic Atari 2600/5200/7800 Game Systems FAQ - Pinout by Harry Dodgson*

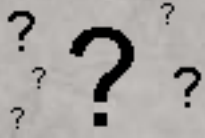
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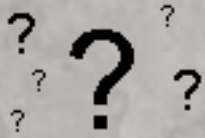
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# Atari Cartridge Port



(at the Computer)



(at the Devices)

40 PIN EDGE ?? at the Computer.

40 PIN EDGE ?? at the Devices.

Pin	Name	Description
1	+5V	+5 VDC
2	+5V	+5 VDC
3	D14	Data 14
4	D15	Data 15
5	D12	Data 12
6	D13	Data 13
7	D10	Data 10
8	D11	Data 11
9	D8	Data 8
10	D9	Data 9
11	D6	Data 6
12	D7	Data 7
13	D4	Data 4
14	D5	Data 5
15	D2	Data 2
16	D3	Data 3



17	D0	Data 0
18	D1	Data 1
19	A13	Address 13
20	A15	Address 15
21	A8	Address 8
22	A14	Address 14
23	A7	Address 7
24	A9	Address 9
25	A6	Address 6
26	A10	Address 10
27	A5	Address 5
28	A12	Address 12
29	A11	Address 11
30	A4	Address 4
31	RS3	ROM Select 3
32	A3	Address 3
33	RS4	ROM Select 4
34	A2	Address 2
35	UDS	Upper Data Strobe
36	A1	Address 1
37	LDS	Lower Data Strobe
38	GND	Ground
39	GND	Ground
40	GND	Ground

Contributor: [Joakim Ögren](#), [Lawrence Wright](#), [Steve & Sally Blair](#)

Source:  
?

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# Atari Falcon030 DSP Port

26 PIN UNKNOWN 3 ROW FEMALE CONNECTOR on the computer

Pin	Description
1	General Purpose 0
2	General Purpose 2
3	General Purpose 1
4	SDMA Play Data
5	SDMA Play Clock
6	SDMA Play Sync
7	Not Connect
8	Ground
9	+12V
10	Ground
11	Sync Serial I/F Ctrl 0
12	Sync Serial I/F Ctrl 1
13	Sync Serial I/F Ctrl 2
14	Ground
15	Sync Serial Data In
16	Ground
17	+12V
18	Ground
19	SDMA Record Data
20	SDMA Record Clock
21	SDMA Record Sync
22	DSP Interrupt
23	Sync Serial I/F Data Out
24	Sync Serial I/F Clock

25	Ground
26	External Clock Input

*Contributor:* [Joakim Ögren](#), Jan Krupka

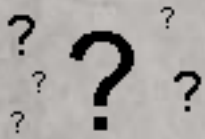
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*Atari Falcon030 DSP pinout at [Technick.net](#)*

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# C128 Expansion Bus

Available at the Commodore 128.



(at the computer)

44 PIN FEMALE EDGE at the computer.

Pin	Name	Description
1	GND	System Ground
2	+5V	System Vcc
3	+5V	System Vcc
4	/IRQ	Interrupt request
5	R/W	System Read/Write Signal
6	DClock	8.18MHz Video Dot Clock
7	I/O1	I/O Chip select \$de00-deff
8	/GAME	Sensed for memory map configuration
9	/EXROM	Sensed for memory map configuration
10	I/O2	I/O Chip select \$df00-dfff
11	/ROML	External ROM select \$8000-Bfff
12	BA	Bus available output
13	/DMA	Direct memory access input
14	D7	Data bit 7
15	D6	Data bit 6
16	D5	Data bit 5
17	D4	Data bit 4
18	D3	Data bit 3



19	D2	Data bit 2
20	D1	Data bit 1
21	D0	Data bit 0
22	GND	System Ground
A	GND	System Ground
B	/ROMH	External ROM Select \$c000-ffff
C	/RESET	System Reset Signal
D	/NMI	Non-Maskable Interrupt
E	1MHz	System 1MHz clock
F	TA15	Translated address bit 15
H	TA14	Translated address bit 14
J	TA13	Translated address bit 13
K	TA12	Translated address bit 12
L	TA11	Translated address bit 11
M	TA10	Translated address bit 10
N	TA9	Translated address bit 9
P	TA8	Translated address bit 8
R	SA7	Shared address bit 7
S	SA6	Shared address bit 6
T	SA5	Shared address bit 5
U	SA4	Shared address bit 4
V	SA3	Shared address bit 3
W	SA2	Shared address bit 2
X	SA1	Shared address bit 1
Y	SA0	Shared address bit 0
Z	GND	System Ground

Contributor: [Rob Gill](#)

Source:  
Commodore 128 Programmers reference guide

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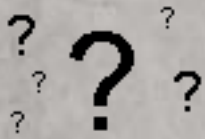
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# C16/+4 Expansion Bus

Available on Commodore C16, C116 and +4 computers.



(at the Computer)

50 PIN FEMALE EDGE (2 mm pitch) at the Computer.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 VDC
3	+5V	+5 VDC
4	/IRQ	Interrupt
5	R/W	Read/Write (1=Read, 0=Write)
6	C1HIGH	External Cartridge Chip Selects C1 High
7	C2LOW	External Cartridge Chip Selects C2 Low (reserved)
8	C2HIGH	External Cartridge Chip Selects C2 High (reserved)
9	/CS1	Chip Select Line 1
10	/CS0	Chip Select Line 0
11	/CAS	Column Address Strobe
12	MUX	DRAM address multiplex control signal
13	BA	Bus Available (Low=DMA)
14	D7	Data 7
15	D6	Data 6
16	D5	Data 5
17	D4	Data 4
18	D3	Data 3

19	D2	Data 2
20	D1	Data 1
21	D0	Data 0
22	AEC	Address Enable Code
23	EAI	External Audio In
24	PHI 2	Artificial Phi 2 signal
25	GND	Ground
A	GND	Ground
B	C1LOW	External Cartridge Chip Selects C1 Low
C	/RESET	Reset
D	/RAS	Row Address Strobe
E	PHI 0	Artificial Phi 0 Signal
F	A15	Address 15
H	A14	Address 14
J	A13	Address 13
K	A12	Address 12
L	A11	Address 11
M	A10	Address 10
N	A9	Address 9
P	A8	Address 8
R	A7	Address 7
S	A6	Address 6
T	A5	Address 5
U	A4	Address 4
V	A3	Address 3
W	A2	Address 2
X	A1	Address 1
Y	A0	Address 0
Z	n/c	Not connected
AA	n/c	Not connected
BB	n/c	Not connected
CC	GND	Ground



PHI 2: Address valid on the rising edge, data valid on the falling edge

Contributor: [Joakim Ögren](#), [Arwin Vosselman](#)

Sources:

*Usenet posting in comp.sys.cbm, Pinout specs for cbm machines needed by [Lonnie McClure](#)*

*SAMS Computerfacts CC8 Commodore 16*

*Article in C'T September 1986*

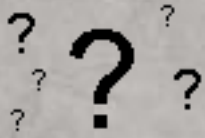
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# C64 Cartridge Expansion



(at the computer)

44 PIN FEMALE EDGE at the computer.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 Volts DC
3	+5V	+5 Volts DC
4	/IRQ	Interrupt Request
5	/CR/W	
6	DOTCLK	Dot Clock
7	I/O 1	
8	/GAME	Game
9	/EXROM	
10	I/O 2	
11	/ROML	ROM Low
12	BA	
13	/DMA	
14	CD7	Cartridge Data 7
15	CD6	Cartridge Data 7
16	CD5	Cartridge Data 7
17	CD4	Cartridge Data 7
18	CD3	Cartridge Data 7
19	CD2	Cartridge Data 7
20	CD1	Cartridge Data 7

21	CD0	Cartridge Data 7
22	GND	Ground
A	GND	Ground
B	/ROMH	ROM High
C	/RESET	Reset
D	/NMI	Non Maskable Interrupt
E	S02	
F	CA15	Cartridge Address 15
H	CA14	Cartridge Address 14
J	CA13	Cartridge Address 13
K	CA12	Cartridge Address 12
L	CA11	Cartridge Address 11
M	CA10	Cartridge Address 10
N	CA9	Cartridge Address 9
P	CA8	Cartridge Address 8
R	CA7	Cartridge Address 7
S	CA6	Cartridge Address 6
T	CA5	Cartridge Address 5
U	CA4	Cartridge Address 4
V	CA3	Cartridge Address 3
W	CA2	Cartridge Address 2
X	CA1	Cartridge Address 1
Y	CA0	Cartridge Address 0
Z	GND	Ground

Contributor: [Joakim Ögren](#), [Arwin Vosselman](#)

Source:  
Commodore 64 Programmer's Reference Guide

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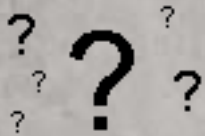
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# C64 RS232 User Port

Available on the Commodore C64/C128. Software emulated. The signals does not have true RS232 levels. It's TTL level, and RXD/TXD is inverted. It's just the normal User Port, used as a RS232 port.



(at the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	RS232	Description
A	GND	GND	Protective Ground
B+C	FLAG2+PB0	RxD	Receive Data (Must be applied to both pins!)
D	PB1	RTS	Ready To Send
E	PB2	DTR	Data Terminal Ready
F	PB3	RI	Ring Indicator
H	PB4	DCD	Data Carrier Detect
K	PB6	CTS	Clear To Send
L	PB7	DSR	Data Set Ready
M	PA2	TxD	Transmit Data
N	GND	GND	Signal Ground

Contributor: [Joakim Ögren](#), [Arwin Vosselman](#), [Mark Sokos](#)

Source:

Usenet posting in *comp.sys.cbm* - Help on modem -> c64 by [Lasher Glenn](#)

*Commodore 64 Programmer's Reference Guide*

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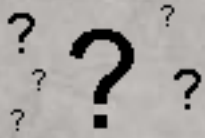
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# C64 User Port



(at the computer)

24 PIN MALE EDGE (DZM 12 DREH) at the computer.

Pin	Name	Description
1	GND	Ground
2	+5V	+5 VDC (100 mA max)
3	/RESET	Reset, will force a Cold Start. Also a reset output for devices.
4	CNT1	Counter 1, from CIA #1
5	SP1	Serial Port 1, from CIA #1
6	CNT2	Counter 2, from CIA #2
7	SP2	Serial Port 2, from CIA #2
8	/PC2	Handshaking line, from CIA #2
9	ATN	Serial Attention In
10	+9V AC	+9 VAC (+ phase) (100 mA max)
11	+9V AC	+9 VAC (- phase) (100 mA max)
12	GND	Ground
A	GND	Ground
B	/FLAG2	Flag 2
C	PB0	Data 0
D	PB1	Data 1
E	PB2	Data 2
F	PB3	Data 3
H	PB4	Data 4

J	PB5	Data 5
K	PB6	Data 6
L	PB7	Data 7
M	PA2	PA2
N	GND	Ground

*Contributor:* [Joakim Ögren](#), [Nikolas Engström](#), [Arwin Vosselman](#), *Jestin Nesselroad*

*Source:*

*Commodore 64 Programmer's Reference Guide*

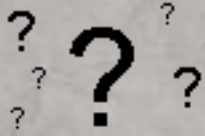
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# CD32 Expansion-port



(at the computer)

UNKNOWN 182 PIN CONNECTOR (SAME AS MCA) at the computer.

Pin	Name	Description	Comment
1	A31	Address 31	Probably not connected since 68EC020
2	A30	Address 30	Probably not connected since 68EC020
3	A29	Address 29	Probably not connected since 68EC020
4	A28	Address 28	Probably not connected since 68EC020
5	A27	Address 27	Probably not connected since 68EC020
6	A26	Address 26	Probably not connected since 68EC020
7	A25	Address 25	Probably not connected since 68EC020
8	A24	Address 24	
9	DGND	Data Ground	
10	VCC	+5 VDC	
11	A23	Address 23	
12	A22	Address 22	
13	A21	Address 21	
14	A20	Address 20	
15	A19	Address 19	
16	A18	Address 18	
17	A17	Address 17	
18	A16	Address 16	
19	DGND	Data Ground	
20	VCC	+5 VDC	

21	A15	Address 15	
22	A14	Address 14	
23	A13	Address 13	
24	A12	Address 12	
25	A11	Address 11	
26	A10	Address 10	
27	A9	Address 9	
28	A8	Address 8	
29	DGND	Data Ground	
30	VCC	+5 VDC	
31	A7	Address 7	
32	A6	Address 6	
33	A5	Address 5	
34	A4	Address 4	
35	A3	Address 3	
36	A2	Address 2	
37	A1	Address 1	
38	A0	Address 0	
39	DGND	Data Ground	
40	VCC	+5 VDC	
41	D31	Data 31	
42	D30	Data 30	
43	D29	Data 29	
44	D28	Data 28	
45	D27	Data 27	
46	D26	Data 26	
47	D25	Data 25	
48	D24	Data 24	
49	DGND	Data Ground	
50	VCC	+5 VDC	
51	D23	Data 23	
52	D22	Data 22	



53	D21	Data 21	
54	D20	Data 20	
55	D19	Data 19	
56	D18	Data 18	
57	D17	Data 17	
58	D16	Data 16	
59	DGND	Data Ground	
60	VCC	+5 VDC	
61	D15	Data 15	
62	D14	Data 14	
63	D13	Data 13	
64	D12	Data 12	
65	D11	Data 11	
66	D10	Data 10	
67	D9	Data 9	
68	D8	Data 8	
69	DGND	Data Ground	
70	VCC	+5 VDC	
71	D7	Data 7	
72	D6	Data 6	
73	D5	Data 5	
74	D4	Data 4	
75	D3	Data 3	
76	D2	Data 2	
77	D1	Data 1	
78	D0	Data 0	
79	DGND	Data Ground	
80	VCC	+5 VDC	
81	/IPL2	Interrupt Priority Level 2	
82	/IPL1	Interrupt Priority Level 1	
83	/IPL0	Interrupt Priority Level 0	
84			

85	/RST	Reset	
86	/HALT	Halt	
87	/ECS	ECS??	
88	/OCS	OCS??	
89	SIZE1	Size 1	Indicates number of bytes remaining to transfer
90	SIZE0	Size 0	Indicates number of bytes remaining to transfer
91	/AS	Address Strobe	
92	/DS	Data Strobe	
93	/R/W	Read/Write	
94	/BERR	Bus Error	
95			
96	/AVEC	Autovector Req	Autovector request during interrupt acknowledge
97	/DSACK1	Data Ack 1	Data transfer and size acknowledge
98	/DSACK0	Data Ack 0	Data transfer and size acknowledge
99	CPUCLK_A		
100			
101	DGND	Data Ground	
102	VCC	+5 VDC	
103	FC2	Function Codes 2	
104	FC1	Function Codes 1	
105	FC0	Function Codes 0	
106			
107			
108			
109			
110			
111	/CPU_BR	CPU bus request??	
112	/EXP_BG	Expansion bus granted??	
113	/CPU_BG	CPU bus granted??	
114	/EXP_BR	Expansion bus request??	
115			
116			

117	/PUNT		
118	/RESET	68020 RESET	
119	/INT2	Interrupt 2	Generate a level 2 interrupt
120	/INT6	Interrupt 2	Generate a level 6 interrupt
121	/KB_CLOCK	Keyboard clock	
122	/KB_DATA	Keyboard data	
123	/FIRE0	Fire Button 0??	
124	/FIRE1	Fire Button 1??	
125	/LED	Power On LED ??	
126	/ACTIVE	Disk active LED	
127	/RXD	Serial Receive	Serial data in
128	/TXD	Serial Transmit	Serial data out
129	/DKRD		Floppy interface (Paula?)
130	/DKWD		Floppy interface (Paula?)
131	SYSTEM		
132	/DKWE		Floppy interface (Paula?)
133	CONFIG_OUT		
134			
135	DGND	Data Ground	
136	+12V	+12V DC	
137	DGND	Data Ground	
138	+12V	+12V DC	
139	17MHZ		For FMV interface ??
140	EXT_AUDIO		For FMV interface ??
141	DA_DATA		For FMV interface ??
142	/MUTE		For FMV interface ??
143	DA_LRCLK		For FMV interface ??
144	DA_BCLK		For FMV interface ??
145	DGND	Data Ground	
146	VCC	+5 VDC	
147	DR	Digital Red	
148	DG	Digital Green	

149	DB	Digital Blue	
150	DI	Digital Intensity	
151	/PIXELSW_EXT		
152	/PIXELSW		
153	/BLANK		
154	PIXELCLK	Pixelclock	For manipulating RBG data
155	DGND	Data Ground	
156	VCC	+5 VDC	
157	/CSYNC	Composite sync	Not buffered.
158	CCK_B	Color clock ??	
159	/HSYNC	Horizontal sync	
160	/VSYNC	Vertical sync	
161	VGND	Video ground	
162	VGND	Video ground	
163	AR_EXT	Analog Red External	
164	AR	Analog Red	
165	AG_EXT	Analog Green External	
166	AG	Analog Green	
167	AB_EXT	Analog Blue External	
168	AB	Analog Blue	
169	VGND	Video ground	
170	VGND	Video ground	
171	/NTSC		
172	/XCLKEN	Enable External video clock	(Genlock)
173	XCLK	External video clock	(Genlock)
174	/EXT_VIDEO	External Video	Disable internal video interfaces
175	DGND	Data Ground	
176	VCC	+5 VDC	
177	AGND	Audio Ground	
178	+12V	+12V DC	
179	LEFT_EXT	Left sound External	
180	LEFT	Left sound	



181	RIGHT_EXT	Right sound External	
182	RIGHT	Right sound	

Contributor: [Joakim Ögren](#)

Source:

[CD32 expansion port info](#)

Usenet posting by [Anders Stenkvist](#)

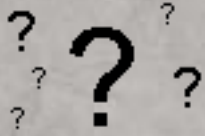
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# CDTV Diagnostic Slot



(at the computer)

80 PIN ??? CONNECTOR at the computer.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	VCC	+5 VDC
4	VCC	+5 VDC
5	/CFGOUT	Configout AutoConfig signal (not connected)
6	/CFGIN	Configin AutoConfig signal (grounded)
7	GND	Ground
8	CCKQ	3.58 MHz CCKQ clock (C3)
9	CDAC	7.16 MHz CDAC clock (90° before system clock)
10	CCK	3.58 MHz CCK clock (C1)
11	/OVR	Override (Disables /DTACK generation of Gary)
12	XRDY	External Ready (Generates wait states while low).
13	/INT2	Level 2 Interrupt
14	n/c	not connected
15	A5	Address Bus 5
16	/INT6	Level 6 Interrupt
17	A6	Address Bus 6
18	A4	Address Bus 4
19	GND	Ground
20	A3	Address Bus 3

21	A2	Address Bus 2
22	A7	Address Bus 7
23	A1	Address Bus 1
24	A8	Address Bus 8
25	/FC0	Processor Function Code Status (bit 0)
26	A9	Address Bus 9
27	/FC1	Processor Function Code Status (bit 1)
28	A10	Address Bus 10
29	/FC2	Processor Function Code Status (bit 2)
30	A11	Address Bus 11
31	GND	Ground
32	A12	Address Bus 12
33	A13	Address Bus 13
34	/IPL0	Interrupt Priority Level (bit 0)
35	A14	Address Bus 14
36	/IPL1	Interrupt Priority Level (bit 1)
37	A15	Address Bus 15
38	/IPL2	Interrupt Priority Level (bit 2)
39	A16	Address Bus 16
40	/BERR	Bus Error
41	A17	Address Bus 17
42	/VPA	Valid Peripheral Address (asserted by Gary)
43	GND	Ground
44	E	E Clock
45	/VMA	Valid Memory Address (asserted by Gary)
46	A18	Address Bus 18
47	/RST	Reset
48	A19	Address Bus 19
49	/HLT	Halt
50	A20	Address Bus 20
51	A22	Address Bus 22
52	A21	Address Bus 21

53	A23	Address Bus 23
54	/BR	Bus Request
55	GND	Ground
56	/BGACK	Bus Grant Acknowledge
57	D15	Data Bus 15
58	/BG	Bus Grant
59	D14	Data Bus 14
60	/DTACK	Data Transfer Acknowledge (normally asserted by Gary)
61	D13	Data Bus 13
62	R/W	Read/Write (high=read, low=write)
63	D12	Data Bus 12
64	/LDS	Lower Data Strobe
65	D11	Data Bus 11
66	/UDS	Upper Data Strobe
67	GND	Ground
68	/AS	Address Strobe
69	D0	Data Bus 0
70	D10	Data Bus 10
71	D1	Data Bus 1
72	D9	Data Bus 9
73	D2	Data Bus 2
74	D8	Data Bus 8
75	D3	Data Bus 3
76	D7	Data Bus 7
77	D4	Data Bus 4
78	D6	Data Bus 6
79	GND	Ground
80	D5	Data Bus 5

*Note: Pin 7-80 is equivalent with the Amiga 500's pin 13-86 at the 86 pin Amiga 500 connector.*

Contributor: [Joakim Ögren](#)



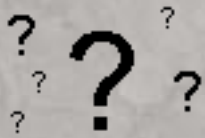
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*Darren Ewaniuk's CDTV Technical Information*

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*Document last modified: 2001-06-08*



# CDTV Expansion Slot

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29



(at the computer)

30 PIN ??? CONNECTOR at the computer.

Pin	Name	Description
1	GND	Ground
2	GND	Ground
3	VCC	+5 VDC
4	VCC	+5 VDC
5	SD1	Data Bus 1
6	SD0	Data Bus 0
7	SD3	Data Bus 3
8	SD2	Data Bus 2
9	SD5	Data Bus 5
10	SD4	Data Bus 4
11	SD7	Data Bus 7
12	SD6	Data Bus 6
13	/SDREQ	DMA Request
14	/INTX	Interrupt Request
15	/CSS	Chip Select
16	/SDACK	DMA Acknowledge

17	/IOR	I/O Read
18	/IOW	I/O Write
19	A8	Address Bus 8
20	7M	7.16 MHz System Clock
21	A6	Address Bus 6
22	A7	Address Bus 7
23	A4	Address Bus 4
24	A5	Address Bus 5
25	A2	Address Bus 2
26	A3	Address Bus 3
27	/IFRST	+5 VDC
28	A1	Address Bus 1
29	GND	Ground
30	GND	Ground

Contributor: [Joakim Ögren](#)

Source:

*Darren Ewaniuk's CDTV Technical Information*

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# Commodore PET Parallel User Port

## 24 PIN UNKNOWN CONNECTOR

```

                                1  1  1
    1  2  3  4  5  6  7  8  9  0  1  2
    =  =  =  =  =  =  =  =  =  =  =  =
    ### #####
    =  =  =  =  =  =  =  =  =  =  =  =
    A  B  C  D  E  F  H  J  K  L  M  N
  
```

Pin	Name
1	System Ground
2	TV Video
3	IEEE-SRQ
4	IEEE-EOI
5	Diagnostic Sense
6	Cass.1 Read
7	Cass.2 Read
8	Diag Tape Wrt.
9	TV Vertical
10	TV Horizontal
11	GND
12	GND
A	GND
B	CA1
C	PB0
D	PB1
E	PB2
F	PB3



H	PB4
J	PB5
K	PB6
L	PB7
M	PA2 (CB2)
N	GND

*Contributor:* [Joakim Ögren](#)

*Source:*  
[Commodore PET FAQ](#)

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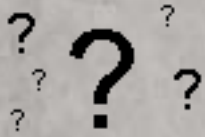
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*Document last modified:* 2000-07-07



# GameBoy Cartridge

Available on the Nintendo GameBoy.



(at the GameBoy)

UNKNOWN CONNECTOR at the GameBoy.

Pin	Name	Description
1	VCC	+5 VDC
2	?	? Connected on Gameboy, but not used on GamePaks.
3	/RESET	Reset
4	/WR	Write
5	?	? Used by paging PAL on high capacity GamePaks.
6	A0	Address 0
7	A1	Address 1
8	A2	Address 2
9	A3	Address 3
10	A4	Address 4
11	A5	Address 5
12	A6	Address 6
13	A7	Address 7
14	A8	Address 8
15	A9	Address 9
16	A10	Address 10
17	A11	Address 11
18	A12	Address 12

19	A13	Address 13
20	A14	Address 14
21	/CS	Chip Select
22	D0	Data 0
23	D1	Data 1
24	D2	Data 2
25	D3	Data 3
26	D4	Data 4
27	D5	Data 5
28	D6	Data 6
29	D7	Data 7
30	/RD	Read
31	?	? Connected on Gameboy, but not used on Game-Paks.
32	GND	Ground

Contributor: [Joakim Ögren](#)

Source:

*Nintendo GameBoy FAQ - Pinout by Peter Knight & Josef Mollers*

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*Document last modified: 2001-06-08*



# GameBoy Cartridge

Available on the Nintendo GameBoy.

UNKNOWN CONNECTOR at the GameBoy.

Pin	Name	Description
1	VCC	+5 VDC
2	?	? Connected on Gameboy, but not used on GamePaks.
3	/RESET	Reset
4	/WR	Write
5	?	? Used by paging PAL on high capacity GamePaks.
6	A0	Address 0
7	A1	Address 1
8	A2	Address 2
9	A3	Address 3
10	A4	Address 4
11	A5	Address 5
12	A6	Address 6
13	A7	Address 7
14	A8	Address 8
15	A9	Address 9
16	A10	Address 10
17	A11	Address 11
18	A12	Address 12
19	A13	Address 13
20	A14	Address 14
21	/CS	Chip Select
22	D0	Data 0



23	D1	Data 1
24	D2	Data 2
25	D3	Data 3
26	D4	Data 4
27	D5	Data 5
28	D6	Data 6
29	D7	Data 7
30	/RD	Read
31	?	? Connected on Gameboy, but not used on Game-Paks.
32	GND	Ground

Contributor: [Joakim Ögren](#)

Source:  
?

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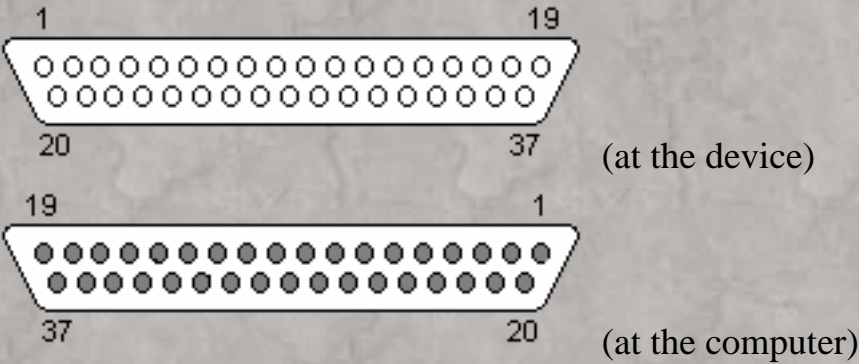
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








# GeekPort

The GeekPort is a connector available at Be's BeBox computers.  
This is a dream for all hobby engineers who like to connect the computer to the coffee machine.



37 PIN D-SUB MALE CONNECTOR at the device.  
37 PIN D-SUB FEMALE CONNECTOR at the computer.

Pin	Name	Description	Dir
1	GND	Ground	
2	A1	Digital A 1	↔
3	A3	Digital A 3	↔
4	A5	Digital A 5	↔
5	A7	Digital A 7	↔
6	GND	Ground	
7	+5V	+5 VDC	
8	GND	Ground	
9	+12V	+12 VDC	
10	GND	Ground	
11	-12V	-12 VDC	
12	GND	Ground	
13	+5V	+5 VDC	
14	GND	Ground	

15	B0	Digital B 0	
16	B2	Digital B 2	
17	B4	Digital B 4	
18	B6	Digital B 6	
19	GND	Ground	
20	A0	Digital A 0	
21	A2	Digital A 2	
22	A4	Digital A 4	
23	A6	Digital A 6	
24	AIref	Analog In Reference	
25	A2D1	Analog In 1	
26	A2D2	Analog In 2	
27	A2D3	Analog In 3	
28	A2D4	Analog In 4	
29	D2A1	Analog Out 1	
30	D2A2	Analog Out 2	
31	D2A3	Analog Out 3	
32	D2A4	Analog Out 4	
33	AOref	Analog Out Reference	
34	B1	Digital B 1	
35	B3	Digital B 3	
36	B5	Digital B 5	
37	B7	Digital B 7	

*Note: Direction is Computer relative Device.*

Contributor: [Joakim Ögren](#)

Source:

BeBox GeekPort DeviceKit at [Be's homepage](#)

BeBox GeekPort DeviceKit: Analog port

BeBox GeekPort DeviceKit: Digital port

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# MSX Expansion

```

49 47 45      5 3 1
+-----//-----+
| H H H  //H H H |
| =====//=====|
| H H H//  H H H |
+-----//-----+
50 48 46      6 4 2






























```





? ?  
? ? ?

(at the Computer)

50 PIN ?? at the Computer.

Pin	Name	Dir	Description
1	/CS1	→	Memory Read in addresses 4000-7FFF
2	/CS2	→	Memory Read in addresses 8000-BFFF
3	/CS12	→	Memory Read in addresses 4000-BFFF
4	/SLTSL	→	Low when Slot 2 (cartridge slot) is selected
5	n/c	-	Not connected.
6	/RFSH	→	Refresh signal from CPU
7	/WAIT	←	OC, Tells CPU to wait. Refresh signal is not maintained
8	/INT	←	OC, Requests a interrupt to CPU (call to addr 38h)
9	/M1	→	CPU fetches first part of instruction from memory.
10	/BUSDIR	←	NC, was used to control the data direction.
11	/IORQ	→	I/O request signal. (Address=Port)
12	/MREQ	→	Memory request signal. (Address=Address)
13	/WR	→	Write signal (strobe)
14	/RD	→	Read signal (strobe)

15	/RESET		Reset
16	n/c	-	Not connected.
17	A0		Address 0
18	A1		Address 1
19	A2		Address 2
20	A3		Address 3
21	A4		Address 4
22	A5		Address 5
23	A6		Address 6
24	A7		Address 7
25	A8		Address 8
26	A9		Address 9
27	A10		Address 10
28	A11		Address 11
29	A12		Address 12
30	A13		Address 13
31	A14		Address 14
32	A15		Address 15
33	D0		Data 0
34	D1		Data 1
35	D2		Data 2
36	D3		Data 3
37	D4		Data 4
38	D5		Data 5
39	D6		Data 6
40	D7		Data 7
41	GND		Ground
42	CLOCK		CPU clock, 3.579 MHz
43	GND		Ground
44	SW1	-	NC, Insert/remove detection for protection
45	+5V		+5 VDC (300mA max /slot)
46	SW2	-	NC, Insert/remove detection for protection

47	+5V		+5 VDC (300mA max /slot)
48	+12V		+12 VDC (50mA max /slot)
49	SOUNDIN		Sound input (-5dBm)
50	-12V		-12 VDC (50mA max /slot)

*Note: Direction is Computer relative Peripheral.*

*Contributor:* [Joakim Ögren](#)

*Source:*

*Mayer's SV738 X'press I/O map*

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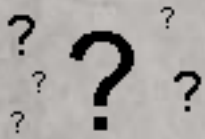
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# PC-Engine Cartridge

Available on the PC Engine.



(at the PC Engine)

UNKNOWN CONNECTOR at the PC Engine.

Pin	Name	Description
1	?	
2	?	
3	A18?	Address 18
4	A16	Address 16
5	A15	Address 15
6	A12	Address 12
7	A7	Address 7
8	A6	Address 6
9	A5	Address 5
10	A4	Address 4
11	A3	Address 3
12	A2	Address 2
13	A1	Address 1
14	A0	Address 0
15	D0	Data 0
16	D1	Data 1
17	D2	Data 2
18	GND	Ground



19	D3	Data 3
20	D4	Data 4
21	D5	Data 5
22	D6	Data 6
23	D7	Data 7
24	/CE	Chip Select
25	A10	Address 10
26	/OE	Output Enable
27	A11	Address 11
28	A9	Address 9
29	A8	Address 8
30	A13	Address 13
31	A14	Address 14
32	A17	Address 17
33	A19?	Address 19
34	R/W	Read/Write
35	?	
36	?	
37	?	
38	+5V	+5 VDC

*Pin 1 is the short pin on the left (if the card is to inserted forwards)*

*Pin 38 is the long pin on the right.*

Contributor: [Joakim Ögren](#)

Source:

Video Games FAQ (Part 3) - Pinout by [David Shadoff](#)

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# Psion Organiser II Connector Top Slot (D)

16 PIN UNKNOWN CONNECTOR on the PDA

Pin	Name	Description
1	SD7	Data Bit 7
2	SD0	Data Bit 0
3	SD6	Data Bit 6
4	SD1	Data Bit 1
5	SD5	Data Bit 5
6	SD2	Data Bit 2
7	SD4	Data Bit 4
8	SD3	Data Bit 3
9	GND	0 Volts
10	SCK	Undefined Control Line
11	SVB	External Power Input / Battery Output Voltage - 0.6 Volt
12	SS3	Slot Select 3
13	SCVV	+5 Volts
14	AC	External On/Clear
15	SOME	Undefined Control Line
16	SMR	Undefined Control Line

Contributor: [Joakim Ögren](#)

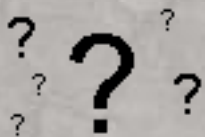
Source:  
Atari Falcon030 DSP pinout at [Technick.net](#)

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Available on the Nintendo SNES.

+-----//-----+																		
32	33	34	35	36	37	38	39	40	//	53	55	56	57	58	59	60	61	62
01	02	03	04	05	06	07	08	09	//	22	24	25	26	27	28	29	30	31
+-----//-----+																		



## UNKNOWN CONNECTOR at the SNES.

<http://www.hardwarebook.net/connector/cartridge/cartridgesnes.html> (1 of 3) [8/6/2002 15:12:46]



15	A2	Address 2
16	A1	Address 1
17	A0	Address 0
18	/IRQ	Interrupt
19	D0	Data 0
20	D1	Data 1
21	D2	Data 2
22	D3	Data 3
23	/READ	Read
24	CIC	?
25	CIC	?
26	/RAM ENABLE	RAM Enable
27	VCC	+5 VDC
28		
29		
30		
31		
32		
33		
34		
35		
36	GND	Ground
37	A12	Address 12
38	A13	Address 13
39	A14	Address 14
40	A15	Address 15
41	A16	Address 16
42	A17	Address 17
43	A18	Address 18
44	A19	Address 19
45	A20	Address 20
46	A21	Address 21

47	A22	Address 22
48	A23	Address 23
49	/ROM ENABLE	ROM Enable
50	D4	Data 4
51	D5	Data 5
52	D6	Data 6
53	D7	Data 7
54	/WRITE	Write
55	CIC	?
56	CIC	?
57	n/c	Not connected
58	VCC	+5 VDC
59		
60		
61		
62		

Contributor: [Joakim Ögren](#)

Source:

Video Games FAQ (Part 3) - Pinout by [Thomas Rolfes](#)

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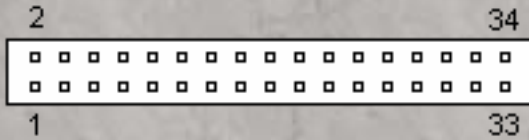
Document last modified: 2001-06-08



# SUN SROMBO

Available on SUN SPARCengine motherboards

Seems to be for SUN internal factory tests/programming



(at the motherboard)

34 PIN IDC MALE at the motherboard

Pin	Name
1	ADR19
2	VCC
3	ADR16
4	ADR18
5	ADR15
6	ADR17
7	ADR12
8	ADR14
9	ADR7
10	ADR13
11	ADR6
12	ADR8
13	ADR5
14	ADR9
15	ADR4
16	ADR11
17	ADR3
18	RD_L

19	ADR2
20	ADR10
21	ADR1
22	ROMBO_CS_L
23	ADR0
24	DAT7
25	DAT0
26	DAT6
27	DAT1
28	DAT5
29	DAT2
30	DAT4
31	GND
32	DAT3
33	NC
34	WR_L

Contributor: [Joakim Ögren](#)

Source:  
*SUN SPARCengine Ultra AXmp Manual*

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# SUN SROMBOLite

Available on SUN SPARCengine motherboards  
 Seems to be for SUN internal factory tests/programming

28 PIN IDC MALE at the motherboard

Pin	Name
1	+5V
2	GND
3	EB_RD_L
4	EB_WR_L
5	EB_SCC_CS_L
6	EB_LATCH
7	EB_RDY_L
8	EB_DAT<0>
9	EB_DAT<1>
10	EB_DAT<2>
11	EB_DAT<3>
12	BRST_L
13	EB_DAT<4>
14	EB_DAT<5>
15	EB_DAT<6>
16	EB_DAT<7>
17	ROMBO_CS_L
18	EB_ADR<0>
19	EB_ADR<1>
20	EB_ADR<2>
21	EB_ADR<3>

22	SYNC_SER_IRQ_L
23	EB_ADR<4>
24	EB_ADR<5>
25	EB_ADR<6>
26	EB_ADR<7>
27	+5V
28	GND

*Contributor:* [Joakim Ögren](#)

*Source:*  
*SUN SPARCengine CP 1500 Manual*

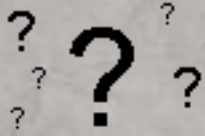
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# Spectravideo SVI318/328 Expansion Bus



(at the computer)

50 PIN MALE EDGE the computer.

Pin	Name	Dir	Description
1	+5v	→	Power, 300mA
2	/CNTRL2	←	Game adapter control signal
3	+12v	→	Power, 100mA
4	-12v	→	Power, 50mA
5	/CNTRL1	←	Game adapter control signal
6	/WAIT	←	Z80 WAIT
7	/RST	←	Z80 RST
8	CPU CLK	→	Buffered 3.58MHz system clock
9	A15	→	Buffered Address bus
10	A14	→	"
11	A13	→	"
12	A12	→	"
13	A11	→	"
14	A10	→	"
15	A9	→	"
16	A8	→	"
17	A7	→	"
18	A6	→	"
19	A5	→	"
20	A4	→	"

21	A3		"
22	A2		"
23	A1		"
24	A0		"
25	/RFSH		RAM expansion refresh
26	/EXCSR		Video-CPU write select
27	/M1		Z80 M1
28	/EXCSW		CPU-Video write select
29	/WR		Z80 WR
30	/MREQ		Z80 MREQ
31	/IORQ		Z80 IORQ
32	/RD		Z80 RD
33	D0	I/O	Buffered Data Bus
34	D1	I/O	"
35	D2	I/O	"
36	D3	I/O	"
37	D4	I/O	"
38	D5	I/O	"
39	D6	I/O	"
40	D7	I/O	"
41	CSOUND		Audio input signal
42	/INT		Z80 INT
43	/RAMDIS		Disable user RAM
44	/ROMDIS		Disable basic ROM
45	/BK32		Enable bank 32 Memory (8000-ffff)
46	/BK31		Enable bank 31 Memory (0000-7FFF)
47	/BK22		Enable bank 22 Memory (8000-FFFF)
48	/BK21		Enable bank 21 Memory (0000-7FFF)
49	GND	-	System Ground
50	GND	-	System Ground

Contributor: [Rob Gill](#)

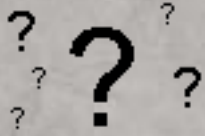


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# Spectravideo SVI318/328 Game Cartridge



(at the computer)

30 PIN FEMALE EDGE at the computer.

Pin	Name
1	+5v
2	+5v
3	A7
4	A12
5	A6
6	A13
7	A5
8	A8
9	A4
10	A9
11	A3
12	A11
13	A10
14	A2
15	A0
16	A1
17	D0
18	D7
19	D1
20	D6

21	D2
22	D5
23	D3
24	D4
25	CCS3
26	CCS4
27	CCS1
28	CCS2
29	GND
30	GND

*Contributor:* [\*Rob Gill\*](#)

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*SVI 328 mk II user manual*

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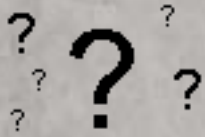
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*Document last modified:* 2001-06-07



# TG-16 Cartridge

Available on the TG-16.



(at the TG-16)

UNKNOWN CONNECTOR at the TG-16.

Pin	Name	Description
1	?	
2	?	
3	A18?	Address 18
4	A16	Address 16
5	A15	Address 15
6	A12	Address 12
7	A7	Address 7
8	A6	Address 6
9	A5	Address 5
10	A4	Address 4
11	A3	Address 3
12	A2	Address 2
13	A1	Address 1
14	A0	Address 0
15	D7	Data 7
16	D6	Data 6
17	D5	Data 5
18	GND	Ground



19	D4	Data 4
20	D3	Data 3
21	D2	Data 2
22	D1	Data 1
23	D0	Data 0
24	/CE	Chip Select
25	A10	Address 10
26	/OE	Output Enable
27	A11	Address 11
28	A9	Address 9
29	A8	Address 8
30	A13	Address 13
31	A14	Address 14
32	A17	Address 17
33	A19?	Address 19
34	R/W	Read/Write
35	?	
36	?	
37	?	
38	+5V	+5 VDC

*Pin 1 is the short pin on the left (if the card is to inserted forwards)*

*Pin 38 is the long pin on the right.*

Contributor: [Joakim Ögren](#)

Source:

Video Games FAQ (Part 3) - Pinout by [David Shadoff](#)

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

# TI-99/4A Card Slot

60 PIN UNKNOWN CONNECTOR on the computer

59      Left      1  
Front ===== Rear  
60      Right      2

Pin	Name	Dir	Description
1	+8V		+5V 3-T regulator voltage supply (about +8V)
2	+8V		+5V 3-T regulator voltage supply (about +8V)
3	GND		Ground
4	READYA		System ready (10K pull-up to +5V)
5	GND		Ground
6	RESET*		System reset (active low)
7	GND		Ground
8	SCLK	nc	System clock (not connected)
9	LCP*	nc	CPU indicator 1=TI99 0=2nd generation (not connected)
10	AUDIO		Input audio (=AUDIOIN)
11	RDBENA*		Active low: enable flex cable data bus drivers (1K pull-up)
12	PCBEN	H	PCB enable for burn-in (always High)
13	HOLD*	H	Active low CPU hold request (always High)
14	IAQHA	nc	IAQ [or] HOLDA (logical or)
15	SENILA*	H	Interrupt level A sense enable (always High)
16	SENILB*	H	Interrupt level B sense enable (always High)
17	INTA*		Active low interrupt level A (=EXTINT*)
18	LOAD*	nc	Unmaskable interrupt (not connected)
19	D7		Data bit 7 (LSB)
20	GND		Ground
21	D5		Data bit 5

22	D6		Data bit 6
23	D3		Data bit 3
24	D4		Data bit 4
25	D1		Data bit 1
26	D2		Data bit 2
27	GND		Ground
28	D0		Data bit 0 (MSB)
29	A14		Address bit 14
30	A15		Address bit 15 (LSB). Also CRU output bit.
31	A12		Address bit 12
32	A13		Address bit 13
33	A10		Address bit 10
34	A11		Address bit 11
35	A8		Address bit 8
36	A9		Address bit 9
37	A6		Address bit 6
38	A7		Address bit 7
39	A4		Address bit 4
40	A5		Address bit 5
41	A2		Address bit 2
42	A3		Address bit 3
43	A0		Address bit 0 (MSB)
44	A1		Address bit 1
45	AMB	H	Extra address bit. Always High.
46	AMA	H	Extra address bit. Always High.
47	GND		Ground
48	AMC	H	Extra address bit. Always High.
49	GND		Ground
50	CLKOUT*		Inversion of phase 3 clock (=PHI3*)
51	CRUCLK*		Inversion of TMS9900 CRUCLOCK pin
52	DBIN		Active high = read memory
53	GND		Ground

54	WE*		Write Enable (derived from TMS9900 WE* pin)
55	CRUIN		CRU input bit to TMS9900
56	MEMEN*		Memory access enable (active low)
57	-12V		-12 Volts 3-T regulator supply voltage (about -16V)
58	-12V		-12 Volts 3-T regulator supply voltage (about -16V)
59	+12V		+12 Volts 3-T regulator supply voltage (about +16V)
60	+12V		+12 Volts 3-T regulator supply voltage (about +16V)

Direction is computer relative world.

#### Notes:

- Signals buffered by 74LS244 in connection card: A0-A15, DBIN, MEMEN\*, WE\*, CLRCLK\*, RESET\*, CLKOUT.
- Unbuffered signals: CRUIN, INTA\*, AUDIOIN, READY
- Data bus is buffered by two 74LS245 (one at each end of the cable), driven by RDBENA (direction set by DBIN).
- All signals must be re-buffered on each card.
- Always High lines (AMA, AMB, AMC, SENILA\*, SENILB\*, PCBEN, HOLD\*) are pulled up to +5 Volts by 47 Ohms resistors.

Contributor: [Joakim Ögren](#)

#### Source:

TI-99/4A Card Slot pinout at [Technick.net](#)

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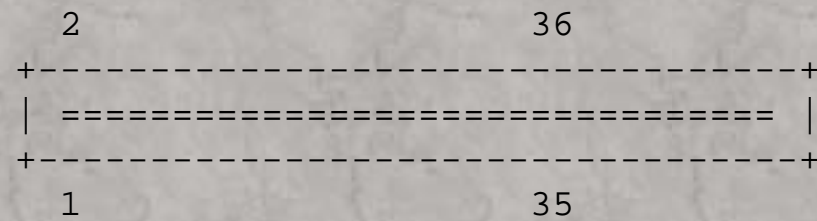
Document last modified: 2001-06-08





# TI-99/4A Cartridge Port

Available on TI-99/4A computers. On the top



Pin	Name	Dir	Description
1	RESET	IN	Resets the system (active high)
2	GND	-	Signal ground
3	D7	IN/OUT	Data bus, bit 7 (least significant)
4	CRUCLK*	OUT	Inversion of TMS9900 CRUCLOCK pin
5	D6	IN/OUT	
6	CRUIN	IN	CRU input to TMS9900
7	D5	IN/OUT	
8	A15	OUT	Address bus, bit 15 / also CRU output bit
9	D4	IN/OUT	
10	A13	OUT	
11	D3	IN/OUT	
12	A12	OUT	
13	D2	IN/OUT	
14	A11	OUT	
15	D1	IN/OUT	
16	A10	OUT	
17	D0	IN/OUT	Data bus, bit 0 (most significant)
18	A9	OUT	
19	VCC	-	+5 Volts power supply

20	A8	OUT	
21	GS*	OUT	Grom select. Active low is addr in >9800-9FFF
22	A7	OUT	
23	A14	OUT	Address bus, bit 14. Select mode: low=data / high=addr
24	A3	OUT	
25	DBIN	OUT	Active high = read memory
26	A6	OUT	
27	GRC	OUT	GROM clock: color burst of VDP 9918A
28	A5	OUT	
29	VDD	-	-5 Volts power supply
30	A4	OUT	
31	GR	IN	Active high = GROM ready
32	WE*	OUT	Active low = write enable (derived from TMS9900 WE*)
33	VSS	-	
34	ROMG*	OUT	Active low if addr in >6000-7FFF
35	GND	-	Ground
36	GND	-	Ground

Contributor: [Joakim Ögren](#)

Source:  
?

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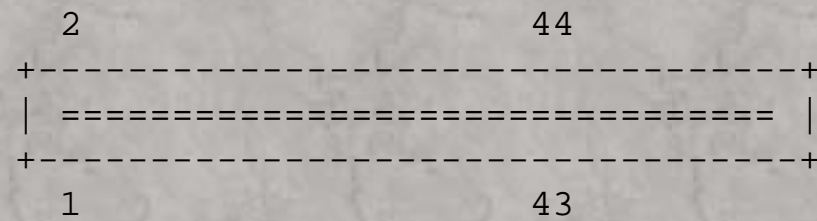
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Document last modified: 2000-07-09



# TI-99/4A Side Port

Available on TI-99/4A computers. On the right side



Pin	Name	Dir	Description
1	VCC	-	+5 Volts power supply
2	SBE	OUT	Low if addr in >9000-94xx (sound port)
3	RESET*	OUT	System reset (active low)
4	EXTINT*	IN	External interrupt (active low)
5	A5	OUT	Address bus, bit 5
6	A10	OUT	-
7	A4	OUT	-
8	A11	OUT	-
9	DBIN	OUT	Active high = read memory
10	A3	OUT	-
11	A12	OUT	-
12	READY	IN	Active high = memory is ready
13	LOAD*	IN	Unmaskable interrupt (=> BLWP @>FFFC)
14	A8	OUT	-
15	A13	OUT	-
16	A14	OUT	-
17	A7	OUT	-
18	A9	OUT	-
19	A15	OUT	Address bus, lsb. Also CRU output bit.

20	A2	OUT	-
21	GND	-	Ground
22	CRUCLK*	OUT	Inversion of TMS9900 CRUCLOCK pin
23	GND	-	Ground
24	PHI3*	OUT	Inversion of phase 3 clock
25	GND	-	Ground
26	WE*	OUT	Write Enable (derived from TMS9900 WE* pin)
27	GND	-	Ground
28	MBE*	OUT	Active low if addr in >4000-5FFF (card ROMs)
29	A6	OUT	-
30	A1	OUT	-
31	A0	OUT	Address bus, bit 0 (most significant)
32	MEMEN*	OUT	Memory access enable (active low)
33	CRUIN	IN	CRU input bit to TMS9900
34	D7	IN/OUT	Data bus, bit 7 (least significant)
35	D4	IN/OUT	-
36	D6	IN/OUT	-
37	D0	IN/OUT	Data bus, bit 0 (most significant)
38	D5	IN/OUT	-
39	D2	IN/OUT	-
40	D1	IN/OUT	-
41	IAQ	IN	Interrupt acknowledged by TMS9900
42	D3	IN/OUT	-
43	VDD	-	-5 Volts power supply
44	AUDIOIN	IN	To sound generator AUDIO IN pin

Contributor: [Joakim Ögren](#)

Source:  
?

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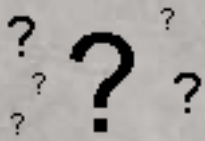
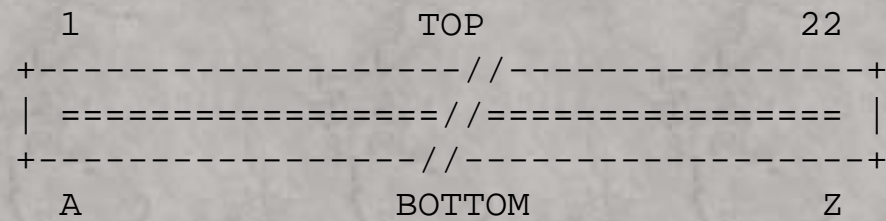
Document last modified: 2000-07-09





# Vic 20 Memory Expansion

Available on Commodore Vic 20 computers. On the left side.



(at the Computer)

UNKNOWN CONNECTOR at the Computer.

Pin	Name	Description
A	GND	Ground
B	CA0	Address 0
C	CA1	Address 1
D	CA2	Address 2
E	CA3	Address 3
F	CA4	Address 4
H	CA5	Address 5
J	CA6	Address 6
K	CA7	Address 7
L	CA8	Address 8
M	CA9	Address 9
N	CA10	Address 10
P	CA11	Address 11
R	CA12	Address 12

S	CA13	Address 13
T	I/O 2	Decoded I/O block 2, starting at \$9130
U	I/O 3	Decoded I/O block 3, starting at \$9140
V	S02	Phase 2 System Clock
W	/NMI	Non maskable Interrupt
X	/RESET	6502 Reset
Y	n/c	Not connected
Z	GND	Ground
1	GND	Ground
2	CD0	Data 0
3	CD1	Data 1
4	CD2	Data 2
5	CD3	Data 3
6	CD4	Data 4
7	CD5	Data 5
8	CD6	Data 6
9	CD7	Data 7
10	/BLK 1	BLK 1 (Memory location \$2000 - \$3fff)
11	/BLK 2	BLK 2 (Memory location \$4000 - \$5fff)
12	/BLK 3	BLK 3 (Memory location \$6000 - \$7fff)
13	/BLK 5	BLK 5 (Memory location \$a000 - \$bfff)
14	RAM 1	RAM 1 (Memory location \$0400 - \$07ff)
15	RAM 2	RAM 2 (Memory location \$0800 - \$0bff)
16	RAM 3	RAM 3 (Memory location \$0c00 - \$0fff)
17	V R/W	Read/Write from Vic chip (1=R, 0=W)
18	C R/W	Read/Write from CPU (1=R, 0=W)
19	/IRQ	6502 Interrupt Request
20	n/c	Not connected
21	+5V	+5 VDC
22	GND	Ground

Contributor: [Joakim Ögren](#)

*Source:*

*Inside your Vic 20 by [Ward Shrake](#)*

*"The Vic Revealed" by Nick Hampshire, 1982, Hayden Book Co, Inc.*

*"Vic20 Programmer's Reference Guide", 1992, Commodore Business, Machines, Inc. and Howard W. Sams & Company, Inc.*

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# Alcatel HC600/800/1000

1 3 5 7 9 11 13 15  
I I I I I I I I

O

O 17

I I I I I I I I  
2 4 6 8 10 12 14 16

17 PIN UNKNOWN CONNECTOR on the phone

Pin	Description
1	Vbat_ext
2	EMMI_PAE
3	Mic
4	EMMI_OPE
5	GND
6	EXT_EMET
7	SCL_E
8	EXT_RECDIT
9	SDA_E
10	GND
11	GND
12	DC_IN (charge)
13	Speaker
14	MARCHE
15	DC_IN (charge)
16	GND
17	Antenna+internal switch (int/ext)

Contributor: [Joakim Ögren](#)



*Source:*

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# Ericsson 218/337/318/388

## UNKNOWN CONNECTOR

Pin	Dir	Description
1		Voice
2		+5V=External Power, 0V=Battery
3		Ext Speak control
4	-	Analog GND
5		Voice
6		+5V=POWER ON, 0V=POWER OFF
7		Charger control
8	-	Digital/DC GND
9		0V=normal,+5V=test, +12V=test+flash
10		Hook
11		TTL serial in
12		TTL serial out
13		0V for aprox 1 sec = POWER ON/OFF
14		DC Power supply

Direction is phone relative world.

Contributor: [Joakim Ögren](#)

Source:

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# Ericsson 628/788

## UNKNOWN CONNECTOR

Pin	Description
1	Audio Out
2	Audio In
3	Accessory Sense. GND to enable External Mic and Speaker (Analog)
4	Audio Signal GND
5	Portable handsfree In.
6	Music Mute Out, High when phone is used.
7	In Flash Memory Voltage and Service Voltage, In 0V=normal, +5V=test, +12V=test+flash
8	Logic Out, Status On. Sources over 100mA
9	Data Out from Mobile Station. Debug messages appear here at 112KBaud when in debug mode.
10	Digital Ground and DC return
11	Data in
12	DC in for battery charging, DC out for accessory power

Contributor: [Joakim Ögren](#)

Source:

Ericsson 628/788 pinout at [Technick.net](#)

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# Ericsson 688/888

## UNKNOWN CONNECTOR

Pin	Description
1	+ external power supply (7.2Volt - 600mA)
2	RS232 input (TTL)
3	GND (digital)
4	RS232 output (TTL)
5	+5V output
6	Test. Switch phone off and provide +5V and switch back on. (set comms at 9600, n,8,1)
7	Mute
8	Internal/external mic and ear (0=External - open=Internal)
9	GND (analogic)
10	? Related to Mic/Speak
11	BF in
12	BF out

Contributor: [Joakim Ögren](#)

Source:

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# Motorola 6200/7500/8200/8400/8700

ANT- (O) | | | | | | | | | |  
 10 9 8 7 6 5 4 3 2 1  
 Top of phone (screen)

Pin	Signal Description
1	Audio Ground
2	Ext b+
3	T Data
4	C Data
5	R Data
6	Logic Ground
7	Audio Out - on/off
8	Audio In
9	Manual Test
10	Battery Feedback

Contributor: [Joakim Ögren](#)

Source:

Motorola 6200/7500/8200/8400/8700 pinout at [Technick.net](#)

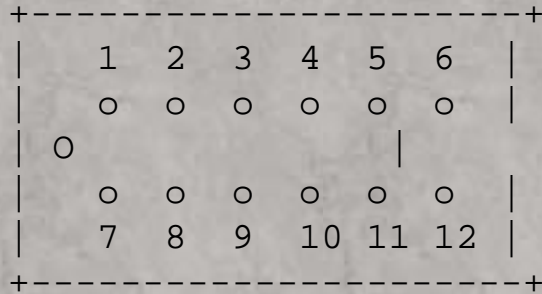
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# NEC P3



Pin	Description
1	Audio out (EAR)
2	Audio out (EAR/SPEAKER)
3	Audio out (SPEAKER)
4	SDATA (Serial Data)
5	No Connect
6	VCC (+8V)
7	No Connect
8	Audio in (MIC)
9	GND
10	BUSY
11	SCLK (Serial Clock)
12	GND

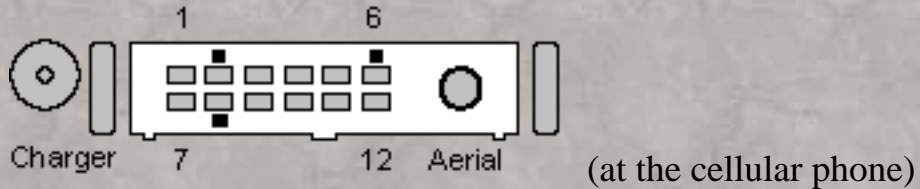
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# Nokia 1610



NOKIA SPECIAL at the cellular phone.

Pin	Name	Description
1	GND	Charger/System Ground
2	V_OUT	Accessory Output Supply. (3.4V...10V - 50mA)
3	XMIC	External Microphone Input and Accessory Identification
4	NC	Not Connected
5	NC	Not Connected
6	MBUS	Serial Control Bus
7	NC	Not Connected
8	SGND	Signal Ground
9	XEAR	External Speaker and Mute Control
10	Hook	Hook Signal
11	NC	Not Connected
12	V_IN	Charging Supply Voltage (Max 16V)

## XMIC: External Microphone Input and Accessory Identification

U low	U high	Description
1.15 V	1.4 V	Compact Handsfree Unit Connected
1.7 V	2.05	Headset Adapter Connected

## MBUS: Serial Control Bus

U low	U high	Description
0.0 V	0.5 V	Logic Low Level
2.4 V	3.2 V	Logic High Level

## XEAR: External Speaker and Mute Control

U low	U high	Description
0.0 V	0.5 V	Mute ON (HF Speaker Mute)
1.0 V	1.7 V	Mute OFF (HF Speaker Active)

## Hook: Hook Signal

U low	U high	Description
0.0 V	0.5 V	Hook Off (Handset in Use)
2.4 V	3.2 V	Hook On (Handset in Use)

Contributor: [Joakim Ögren](#)

Source:

Nokia 1610 pinout at [Technick.net](#)

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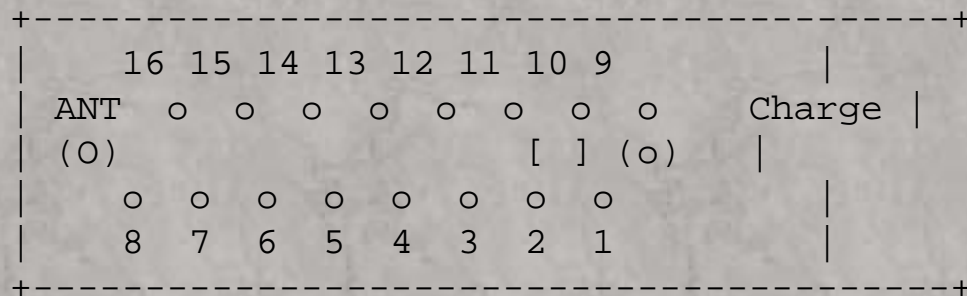
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# Nokia 2110



Pin	Name	Description
1	GND	Digital ground
2	MIC/JCONN	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection control signal
3	AGND	Analogue ground for accessories
4	TDA	Transmitted DBUS data to the accessories
5	M2BUS	Serial Bidirectional data and control between the handportable and accessories
6	HOOK/RXD2	Hook indication. HP has a 100KE pull-up resistor
7	PHFS/TXD2	Handsfree device power on/off, data to flash programming device
8	VCHAR	Battery charging voltage
9	GND	Digital ground
10	EAR/HFPWR	External Audio output to accessories or handsfree speaker
11	DSYNC	DBUS data bit sync clock
12	RDA	DBUS recieved data from the accessories
13	BENA	Power supply to headset adapter
14	VF	Programming voltage for FLASH
15	DCLK	DBUS data clock
16	VCHAR	Battery charging voltage

Contributor: [Joakim Ögren](#)

*Source:*

*Nokia 2110 pinout at [Technick.net](http://Technick.net)*

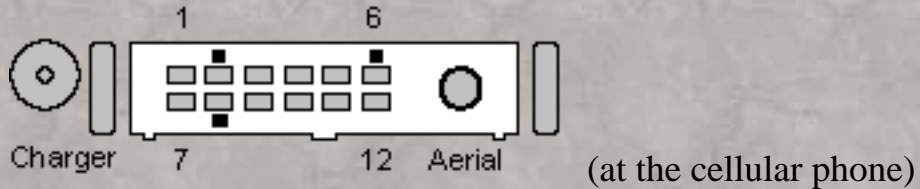
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# Nokia 31xx/81xx



NOKIA SPECIAL at the cellular phone.

Pin	Name	Description
1	GND	Charger/System Ground
2	V_OUT	Accessory Output Supply. (3.4V...10V - 50mA)
3	XMIC	External Microphone Input and Accessory Identification
4	EXT_RF	External RF Control Input
5	TX	FBUS Transmit
6	MBUS	Serial Control Bus
7	BENA	Not Connected
8	SGND	Signal Ground
9	XEAR	External Speaker and Mute Control
10	Hook	Hook Signal
11	RX	FBUS Receive
12	V_IN	Charging Supply Voltage (Max 16V)

## XMIC: External Microphone Input and Accessory Identification

U low	U high	Description
1.15 V	1.4 V	Compact Handsfree Unit Connected
1.7 V	2.05	Headset Adapter Connected
2.22 V	2.56 V	Infra Red Link Connected

## EXT\_RF: External RF Control Input

U low	U high	Description
0.0 V	0.5 V	External RF in use
2.4 V	3.2 V	Internal Antenna in use

## MBUS: Serial Control Bus

U low	U high	Description
0.0 V	0.5 V	Logic Low Level
2.4 V	3.2 V	Logic High Level

## XEAR: External Speaker and Mute Control

U low	U high	Description
0.0 V	0.5 V	Mute ON (HF Speaker Mute)
1.0 V	1.7 V	Mute OFF (HF Speaker Active)

## Hook: Hook Signal

U low	U high	Description
0.0 V	0.5 V	Hook Off (Handset in Use)
2.4 V	3.2 V	Hook On (Handset in Use)

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Source:

Nokia 31xx/81xx pinout at [Technick.net](#)

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# Nokia 5110/6110



1 Ch 2 3 9 (at the cellular phone)

NOKIA SPECIAL at the cellular phone.

Pin	Description
1	VIN CHARGER INPUT VOLTAGE 8.4V 0.8A
2	CHRG CTRL CHARGER CONTROL PWM 32Khz
3	XMIC MIC INPUT 60mV - 1V
4	SGND SIGNAL GROUND
5	XEAR EAR OUTPUT 80mV - 1V
6	MBUS 9600 B/S
7	FBUS_RX 9.6 - 230.4 KB/S
8	FBUS_TX 9.6 - 230.4 KB/S
9	L_GND CHARGER / LOGIC GND

Contributor: [Joakim Ögren](#)

Source:

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# Panasonic G500

## UNKNOWN CONNECTOR

Pin	Name	Dir	Description
1	GND	---	Ground
2	TX_Audio	-->	?
3	AGND	---	Audio_Ground
4	HF_ON (L=ON)	-->	L=H/F ON
5	AOP_Sense	<--	Data Adaptor Select
6	Serial_Up	<--	UART up (9600,33.8kbps)
7	Serial_Down	-->	UART down
8	External_Power	<--	POWER FOR CHARGING
9	Ground		
10	RX_Audio	<--	
11	Radio_Mute	-->	L=MUTE
12	HF_Sense	<--	L=H/F MODE
13	Reserved		L=FLASH WRITE ENABLE
14	Ignition	<--	H=ON
15	Logic_Power	-->	H=HANDSET ON
16	PAON	-->	Power Amplifier Control Signal

Contributor: [Joakim Ögren](#)

Source:

Panasonic G500 pinout at [Technick.net](#)

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# Phillips Fizz/Spark

## UNKNOWN CONNECTOR

Pin	Description
1	GROUND
2	GROUND
3	HANDS FREE ON/OFF
4	MUTE
5	TX
6	RX
7	RTS
8	REPROGRAMMING
9	ON HOOK CHARGER (APPROX 13V? TO 14V)
10	AUX MIC
11	AUX SPEAKER
12	GROUND
13	+VCC for Car Charger
14	+VCC for Car Charger

Contributor: [Joakim Ögren](#)

Source:

Philips Fizz/Spark pinout at [Technick.net](#)

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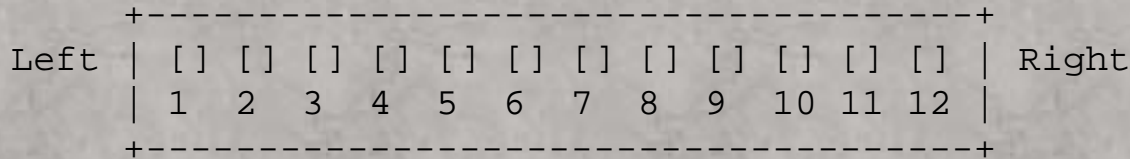
Document last modified: 2001-06-08





# Siemens C25/S25

Top



Pin	Name	Dir	Description
1	GND	-	Ground
2	SELF-SERVICE	in/out	Recognition/control battery charger
3	LOAD	in	Charging voltage
4	BATTERY	out	Battery (S25 only)
5	DATA OUT	out	Data sent (S25 only)
6	DATA IN	in	Data received (S25 only)
7	Z_CLK	-	Recognition/control accessories
8	Z_DATA	-	Recognition/control accessories
9	MICG	-	Ground for microphone
10	MIC	in	Microphone input
11	AUD	out	Loudspeaker
12	AUDG	-	Ground for external speaker

Contributor: [Joakim Ögren](#)

Source:

Siemens C25/S25 pinout at [Technick.net](#)

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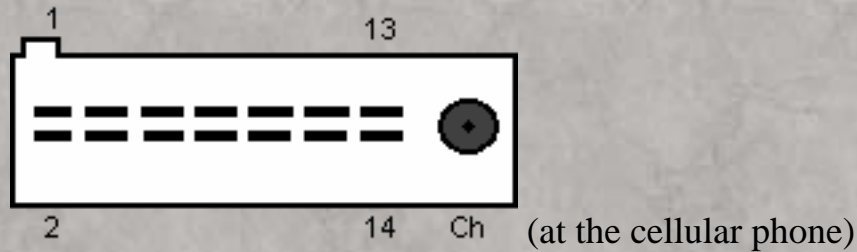
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# Sony CMD 1000



SONY SPECIAL at the cellular phone.

Pin	Description
1	Power (+ 9V)
2	Battery charge
3	Handsfree sos
4	Handsfree extern (10K resistor to +9 to enable handsfree functions)
5	TXE
6	RXE
7	Ignition (10K resistor to +9 to illuminate the display continuously)
8	Antenna extern (10K resistor to ground to enable external microphone and antenna)
9	Audio 1
10	Audio 2 (loudspeaker amplifier output)
11	Microphone (use electrect microfoon and 46 db preamp.)
12	Audio ground (do not connect to 13 and 14 )
13	Ground (supply)
14	Ground (supply)

Contributor: [Joakim Ögren](#)

Source:  
Sony CMD1000 pinout at [Technick.net](#)

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# 144 pin SO DIMM

SO SIMM=Small Outline Single Inline Memory Module

**NOT  
DRAWN  
YET...**



(at the computer)

144 PIN SO SIMM at the computer.

Pin	Normal	ECC	Description
1	VSS	VSS	Ground
2	VSS	VSS	Ground
3	DQ0	DQ0	Data 0
4	DQ32	DQ32	Data 32
5	DQ1	DQ1	Data 1
6	DQ33	DQ33	Data 33
7	DQ2	DQ2	Data 2
8	DQ34	DQ34	Data 34
9	DQ3	DQ3	Data 3
10	DQ35	DQ35	Data 35
11	VCC	VCC	+5 VDC
12	VCC	VCC	+5 VDC
13	DQ4	DQ4	Data 4
14	DQ36	DQ36	Data 36
15	DQ5	DQ5	Data 5
16	DQ37	DQ37	Data 37
17	DQ6	DQ6	Data 6
18	DQ38	DQ38	Data 38

19	DQ7	DQ7	Data 7
20	DQ39	DQ39	Data 39
21	VSS	VSS	Ground
22	VSS	VSS	Ground
23	/CAS0	/CAS0	Column Address Strobe 0
24	/CAS4	/CAS4	Column Address Strobe 4
25	/CAS1	/CAS1	Column Address Strobe 1
26	/CAS5	/CAS5	Column Address Strobe 5
27	VCC	VCC	+5 VDC
28	VCC	VCC	+5 VDC
29	A0	A0	Address 0
30	A3	A3	Address 3
31	A1	A1	Address 1
32	A4	A4	Address 4
33	A2	A2	Address 2
34	A5	A5	Address 5
35	VSS	VSS	Ground
36	VSS	VSS	Ground
37	DQ8	DQ8	Data 8
38	DQ40	DQ40	Data 40
39	DQ9	DQ9	Data 9
40	DQ41	DQ41	Data 41
41	DQ10	DQ10	Data 10
42	DQ42	DQ42	Data 42
43	DQ11	DQ11	Data 11
44	DQ43	DQ43	Data 43
45	VCC	VCC	+5 VDC
46	VCC	VCC	+5 VDC
47	DQ12	DQ12	Data 12
48	DQ44	DQ44	Data 44
49	DQ13	DQ13	Data 13
50	DQ45	DQ45	Data 45



51	DQ14	DQ14	Data 14
52	DQ46	DQ46	Data 46
53	DQ15	DQ15	Data 15
54	DQ47	DQ47	Data 47
55	VSS	VSS	Ground
56	VSS	VSS	Ground
57	n/c	CB0	
58	n/c	CB4	
59	n/c	CB1	
60	n/c	CB5	
61	DU	DU	Don't use
62	DU	DU	Don't use
63	VCC	VCC	+5 VDC
64	VCC	VCC	+5 VDC
65	DU	DU	Don't use
66	DU	DU	Don't use
67	/WE	/WE	Read/Write
68	n/c	n/c	Not connected
69	/RAS0	/RAS0	Row Address Strobe 0
70	n/c	n/c	Not connected
71	/RAS1	/RAS1	Row Address Strobe 1
72	n/c	n/c	Not connected
73	/OE	/OE	
74	n/c	n/c	Not connected
75	VSS	VSS	Ground
76	VSS	VSS	Ground
77	n/c	CB2	
78	n/c	CB6	
79	n/c	CB3	
80	n/c	CB7	
81	VCC	VCC	+5 VDC
82	VCC	VCC	+5 VDC

83	DQ16	DQ16	Data 16
84	DQ48	DQ48	Data 48
85	DQ17	DQ17	Data 17
86	DQ49	DQ49	Data 49
87	DQ18	DQ18	Data 18
88	DQ50	DQ50	Data 50
89	DQ19	DQ19	Data 19
90	DQ51	DQ51	Data 51
91	VSS	VSS	Ground
92	VSS	VSS	Ground
93	DQ20	DQ20	Data 20
94	DQ52	DQ52	Data 52
95	DQ21	DQ21	Data 21
96	DQ53	DQ53	Data 53
97	DQ22	DQ22	Data 22
98	DQ54	DQ54	Data 54
99	DQ23	DQ23	Data 23
100	DQ55	DQ55	Data 55
101	VCC	VCC	+5 VDC
102	VCC	VCC	+5 VDC
103	A6	A6	Address 6
104	A7	A7	Address 7
105	A8	A8	Address 8
106	A11	A11	Address 11
107	VSS	VSS	Ground
108	VSS	VSS	Ground
109	A9	A9	Address 9
110	A12	A12	Address 12
111	A10	A10	Address 10
112	A13	A13	Address 13
113	VCC	VCC	+5 VDC
114	VCC	VCC	+5 VDC

115	/CAS2	/CAS2	Column Address Strobe 2
116	/CAS6	/CAS6	Column Address Strobe 6
117	/CAS3	/CAS3	Column Address Strobe 3
118	/CAS7	/CAS7	Column Address Strobe 7
119	VSS	VSS	Ground
120	/VSS	/VSS	Ground
121	DQ24	DQ24	Data 24
122	DQ56	DQ56	Data 56
123	DQ25	DQ25	Data 25
124	DQ57	DQ57	Data 57
125	DQ26	DQ26	Data 26
126	DQ58	DQ58	Data 58
127	DQ27	DQ27	Data 27
128	DQ59	DQ59	Data 59
129	VCC	VCC	+5 VDC
130	VCC	VCC	+5 VDC
131	DQ28	DQ28	Data 28
132	DQ60	DQ60	Data 60
133	DQ29	DQ29	Data 29
134	DQ61	DQ61	Data 61
135	DQ30	DQ30	Data 30
136	DQ62	DQ62	Data 62
137	DQ31	DQ31	Data 31
138	DQ63	DQ63	Data 63
139	VSS	VSS	Ground
140	VSS	VSS	Ground
141	SDA	SDA	
142	SCL	SCL	
143	VCC	VCC	+5 VDC
144	VCC	VCC	+5 VDC

Contributor: [Joakim Ögren](#), [Mark Brown](#)

*Source:*

*Various productsheets at [IBM Memory Products](#)*

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*Document last modified: 2001-06-07*





# 168 pin DRAM DIMM (Unbuffered)

DIMM=Dual Inline Memory Module

**NOT  
DRAWN  
YET...**



(at the computer)

168 PIN DIMM at the computer.

Front Side (left side 1-42, right side 43-84)

Back Side (left side 85-126, right side 127-168)

## Front, Left

Pin	Non-Parity?	Parity?	72 ECC?	80 ECC?	Description
1	VSS	VSS	VSS	VSS	Ground
2	DQ0	DQ0	DQ0	DQ0	Data 0
3	DQ1	DQ1	DQ1	DQ1	Data 1
4	DQ2	DQ2	DQ2	DQ2	Data 2
5	DQ3	DQ3	DQ3	DQ3	Data 3
6	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
7	DQ4	DQ4	DQ4	DQ4	Data 4
8	DQ5	DQ5	DQ5	DQ5	Data 5
9	DQ6	DQ6	DQ6	DQ6	Data 6
10	DQ7	DQ7	DQ7	DQ7	Data 7
11	DQ8	DQ8	DQ8	DQ8	Data 8
12	VSS	VSS	VSS	VSS	Ground
13	DQ9	DQ9	DQ9	DQ9	Data 9
14	DQ10	DQ10	DQ10	DQ10	Data 10

15	DQ11	DQ11	DQ11	DQ11	Data 11
16	DQ12	DQ12	DQ12	DQ12	Data 12
17	DQ13	DQ13	DQ13	DQ13	Data 13
18	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
19	DQ14	DQ14	DQ14	DQ14	Data 14
20	DQ15	DQ15	DQ15	DQ15	Data 15
21	n/c	CB0	CB0	CB0	Parity/Check Bit Input/Output 0
22	n/c	CB1	CB1	CB1	Parity/Check Bit Input/Output 1
23	VSS	VSS	VSS	VSS	Ground
24	n/c	n/c	n/c	CB8	Parity/Check Bit Input/Output 8
25	n/c	n/c	n/c	CB9	Parity/Check Bit Input/Output 9
26	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
27	/WE0	/WE0	/WE0	/WE0	Read/Write Input
28	/CAS0	/CAS0	/CAS0	/CAS0	Column Address Strobe 0
29	/CAS1	/CAS1	/CAS1	/CAS1	Column Address Strobe 1
30	/RAS0	/RAS0	/RAS0	/RAS0	Row Address Strobe 0
31	/OE0	/OE0	/OE0	/OE0	Output Enable
32	VSS	VSS	VSS	VSS	Ground
33	A0	A0	A0	A0	Address 0
34	A2	A2	A2	A2	Address 2
35	A4	A4	A4	A4	Address 4
36	A6	A6	A6	A6	Address 6
37	A8	A8	A8	A8	Address 8
38	A10	A10	A10	A10	Address 10
39	A12	A12	A12	A12	Address 12
40	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
41	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
42	DU	DU	DU	DU	Don't Use

## Front, Right

Pin	Non-Parity?	Parity?	72 ECC?	80 ECC?	Description
43	VSS	VSS	VSS	VSS	Ground
44	/OE2	/OE2	/OE2	/OE2	
45	/RAS2	/RAS2	/RAS2	/RAS2	Row Address Strobe 2
46	/CAS2	/CAS2	/CAS2	/CAS2	Column Address Strobe 2
47	/CAS3	/CAS3	/CAS3	/CAS3	Column Address Strobe 3
48	/WE2	/WE2	/WE2	/WE2	Read/Write Input
49	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
50	n/c	n/c	n/c	CB10	Parity/Check Bit Input/Output 10
51	n/c	n/c	n/c	CB11	Parity/Check Bit Input/Output 11
52	n/c	CB2	CB2	CB2	Parity/Check Bit Input/Output 2
53	n/c	CB3	CB3	CB3	Parity/Check Bit Input/Output 3
54	VSS	VSS	VSS	VSS	Ground
55	DQ16	DQ16	DQ16	DQ16	Data 16
56	DQ17	DQ17	DQ17	DQ17	Data 17
57	DQ18	DQ18	DQ18	DQ18	Data 18
58	DQ19	DQ19	DQ19	DQ19	Data 19
59	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
60	DQ20	DQ20	DQ20	DQ20	Data 20
61	n/c	n/c	n/c	n/c	Not connected
62	DU	DU	DU	DU	Don't Use
63	n/c	n/c	n/c	n/c	Not connected
64	VSS	VSS	VSS	VSS	Ground
65	DQ21	DQ21	DQ21	DQ21	Data 21
66	DQ22	DQ22	DQ22	DQ22	Data 22
67	DQ23	DQ23	DQ23	DQ23	Data 23
68	VSS	VSS	VSS	VSS	Ground
69	DQ24	DQ24	DQ24	DQ24	Data 24
70	DQ25	DQ25	DQ25	DQ25	Data 25
71	DQ26	DQ26	DQ26	DQ26	Data 26
72	DQ27	DQ27	DQ27	DQ27	Data 27



73	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
74	DQ28	DQ28	DQ28	DQ28	Data 28
75	DQ29	DQ29	DQ29	DQ29	Data 29
76	DQ30	DQ30	DQ30	DQ30	Data 30
77	DQ31	DQ31	DQ31	DQ31	Data 31
78	VSS	VSS	VSS	VSS	Ground
79	n/c	n/c	n/c	n/c	Not connected
80	n/c	n/c	n/c	n/c	Not connected
81	n/c	n/c	n/c	n/c	Not connected
82	SDA	SDA	SDA	SDA	Serial Data
83	SCL	SCL	SCL	SCL	Serial Clock
84	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC

## Back, Left

Pin	Non-Parity?	Parity?	72 ECC?	80 ECC?	Description
85	VSS	VSS	VSS	VSS	Ground
86	DQ32	DQ32	DQ32	DQ32	Data 32
87	DQ33	DQ33	DQ33	DQ33	Data 33
88	DQ34	DQ34	DQ34	DQ34	Data 34
89	DQ35	DQ35	DQ35	DQ35	Data 35
90	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
91	DQ36	DQ36	DQ36	DQ36	Data 36
92	DQ37	DQ37	DQ37	DQ37	Data 37
93	DQ38	DQ38	DQ38	DQ38	Data 38
94	DQ39	DQ39	DQ39	DQ39	Data 39
95	DQ40	DQ40	DQ40	DQ40	Data 40
96	VSS	VSS	VSS	VSS	Ground
97	DQ41	DQ41	DQ41	DQ41	Data 41
98	DQ42	DQ42	DQ42	DQ42	Data 42
99	DQ43	DQ43	DQ43	DQ43	Data 43



100	DQ44	DQ44	DQ44	DQ44	Data 44
101	DQ45	DQ45	DQ45	DQ45	Data 45
102	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
103	DQ46	DQ46	DQ46	DQ46	Data 46
104	DQ47	DQ47	DQ47	DQ47	Data 47
105	n/c	CB4	CB4	CB4	Parity/Check Bit Input/Output 4
106	n/c	CB5	CB5	CB5	Parity/Check Bit Input/Output 5
107	VSS	VSS	VSS	VSS	Ground
108	n/c	n/c	n/c	CB12	Parity/Check Bit Input/Output 12
109	n/c	n/c	n/c	CB13	Parity/Check Bit Input/Output 13
110	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
111	DU	DU	DU	DU	Don't Use
112	/CAS4	/CAS4	/CAS4	/CAS4	Column Address Strobe 4
113	/CAS5	/CAS5	/CAS5	/CAS5	Column Address Strobe 5
114	/RAS1	/RAS1	/RAS1	/RAS1	Row Address Strobe 1
115	DU	DU	DU	DU	Don't Use
116	VSS	VSS	VSS	VSS	Ground
117	A1	A1	A1	A1	Address 1
118	A3	A3	A3	A3	Address 3
119	A5	A5	A5	A5	Address 5
120	A7	A7	A7	A7	Address 7
121	A9	A9	A9	A9	Address 9
122	A11	A11	A11	A11	Address 11
123	A13	A13	A13	A13	Address 13
124	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
125	DU	DU	DU	DU	Don't Use
126	DU	DU	DU	DU	Don't Use

## Back, Right

Pin	Non-Parity?	Parity?	72 ECC?	80 ECC?	Description

127	VSS	VSS	VSS	VSS	Ground
128	DU	DU	DU	DU	Don't Use
129	/RAS3	/RAS3	/RAS3	/RAS3	Column Address Strobe 3
130	/CAS6	/CAS6	/CAS6	/CAS6	Column Address Strobe 6
131	/CAS7	/CAS7	/CAS7	/CAS7	Column Address Strobe 7
132	DU	DU	DU	DU	Don't Use
133	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
134	n/c	n/c	n/c	CB14	Parity/Check Bit Input/Output 14
135	n/c	n/c	n/c	CB15	Parity/Check Bit Input/Output 15
136	n/c	CB6	CB6	CB6	Parity/Check Bit Input/Output 6
137	n/c	CB7	CB7	CB7	Parity/Check Bit Input/Output 7
138	VSS	VSS	VSS	VSS	Ground
139	DQ48	DQ48	DQ48	DQ48	Data 48
140	DQ49	DQ49	DQ49	DQ49	Data 49
141	DQ50	DQ50	DQ50	DQ50	Data 50
142	DQ51	DQ51	DQ51	DQ51	Data 51
143	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
144	DQ52	DQ52	DQ52	DQ52	Data 52
145	n/c	n/c	n/c	n/c	Not connected
146	DU	DU	DU	DU	Don't Use
147	n/c	n/c	n/c	n/c	Not connected
148	VSS	VSS	VSS	VSS	Ground
149	DQ53	DQ53	DQ53	DQ53	Data 53
150	DQ54	DQ54	DQ54	DQ54	Data 54
151	DQ55	DQ55	DQ55	DQ55	Data 55
152	VSS	VSS	VSS	VSS	Ground
153	DQ56	DQ56	DQ56	DQ56	Data 56
154	DQ57	DQ57	DQ57	DQ57	Data 57
155	DQ58	DQ58	DQ58	DQ58	Data 58
156	DQ59	DQ59	DQ59	DQ59	Data 59
157	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC
158	DQ60	DQ60	DQ60	DQ60	Data 60

159	DQ61	DQ61	DQ61	DQ61	Data 61
160	DQ62	DQ62	DQ62	DQ62	Data 62
161	DQ63	DQ63	DQ63	DQ63	Data 63
162	VSS	VSS	VSS	VSS	Ground
163	CK3	CK3	CK3	CK3	
164	n/c	n/c	n/c	n/c	Not connected
165	SA0	SA0	SA0	SA0	Serial Address 0
166	SA1	SA1	SA1	SA1	Serial Address 1
167	SA2	SA2	SA2	SA2	Serial Address 2
168	VCC	VCC	VCC	VCC	+5 VDC or +3.3 VDC

Contributor: [Joakim Ögren](#), [Mark Brown](#)

Source:

Various productsheets at [IBM Memory Products](#)

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Document last modified: 2001-06-07





# 168 pin SDRAM DIMM (Unbuffered)

DIMM=Dual Inline Memory Module

**NOT  
DRAWN  
YET...**

(at the computer)

168 PIN DIMM at the computer.

Front Side (left side 1-42, right side 43-84)

Back Side (left side 85-126, right side 127-168)

## Front, Left

Pin	Non-Parity	72 ECC?	80 ECC?	Description
1	VSS	VSS	VSS	Ground
2	DQ0	DQ0	DQ0	Data 0
3	DQ1	DQ1	DQ1	Data 1
4	DQ2	DQ2	DQ2	Data 2
5	DQ3	DQ3	DQ3	Data 3
6	VDD	VDD	VDD	+5 VDC or +3.3 VDC
7	DQ4	DQ4	DQ4	Data 4
8	DQ5	DQ5	DQ5	Data 5
9	DQ6	DQ6	DQ6	Data 6
10	DQ7	DQ7	DQ7	Data 7
11	DQ8	DQ8	DQ8	Data 8
12	VSS	VSS	VSS	Ground
13	DQ9	DQ9	DQ9	Data 9
14	DQ10	DQ10	DQ10	Data 10



15	DQ11	DQ11	DQ11	Data 11
16	DQ12	DQ12	DQ12	Data 12
17	DQ13	DQ13	DQ13	Data 13
18	VDD	VDD	VDD	+5 VDC or +3.3 VDC
19	DQ14	DQ14	DQ14	Data 14
20	DQ15	DQ15	DQ15	Data 15
21	n/c	CB0	CB0	Parity/Check Bit Input/Output 0
22	n/c	CB1	CB1	Parity/Check Bit Input/Output 01
23	VSS	VSS	VSS	Ground
24	n/c	n/c	CB8	Parity/Check Bit Input/Output 8
25	n/c	n/c	CB9	Parity/Check Bit Input/Output 9
26	VDD	VDD	VDD	+5 VDC or +3.3 VDC
27	/WE	/WE	/WE	Read/Write
28	DQMB0	DQMB0	DQMB0	Byte Mask signal 0
29	DQMB1	DQMB1	DQMB1	Byte Mask signal 1
30	/S0	/S0	/S0	Chip Select 0
31	DU	DU	DU	Don't Use
32	VSS	VSS	VSS	Ground
33	A0	A0	A0	Address 0
34	A2	A2	A2	Address 2
35	A4	A4	A4	Address 4
36	A6	A6	A6	Address 6
37	A8	A8	A8	Address 8
38	A10/AP	A10/AP	A10/AP	Address 10
39	BA1	BA1	BA1	Bank Address 1
40	VDD	VDD	VDD	+5 VDC or +3.3 VDC
41	VDD	VDD	VDD	+5 VDC or +3.3 VDC
42	CK0	CK0	CK0	Clock signal 0

## Front, Right

Pin	Non-Parity	72 ECC?	80 ECC?	Description
43	VSS	VSS	VSS	Ground
44	DU	DU	DU	Don't Use
45	/S2	/S2	/S2	Chip Select 2
46	DQMB2	DQMB2	DQMB2	Byte Mask signal 2
47	DQMB3	DQMB3	DQMB3	Byte Mask signal 3
48	DU	DU	DU	Don't Use
49	VDD	VDD	VDD	+5 VDC or +3.3 VDC
50	n/c	n/c	CB10	Parity/Check Bit Input/Output 10
51	n/c	n/c	CB11	Parity/Check Bit Input/Output 11
52	n/c	CB2	CB2	Parity/Check Bit Input/Output 2
53	n/c	CB3	CB3	Parity/Check Bit Input/Output 3
54	VSS	VSS	VSS	Ground
55	DQ16	DQ16	DQ16	Data 16
56	DQ17	DQ17	DQ17	Data 17
57	DQ18	DQ18	DQ18	Data 18
58	DQ19	DQ19	DQ19	Data 19
59	VDD	VDD	VDD	+5 VDC or +3.3 VDC
60	DQ20	DQ20	DQ20	Data 20
61	n/c	n/c	n/c	Not connected
62	Vref,NC	Vref,NC	Vref,NC	
63	CKE1	CKE1	CKE1	Clock Enable Signal 1
64	VSS	VSS	VSS	Ground
65	DQ21	DQ21	DQ21	Data 21
66	DQ22	DQ22	DQ22	Data 22
67	DQ23	DQ23	DQ23	Data 23
68	VSS	VSS	VSS	Ground
69	DQ24	DQ24	DQ24	Data 24
70	DQ25	DQ25	DQ25	Data 25
71	DQ26	DQ26	DQ26	Data 26
72	DQ27	DQ27	DQ27	Data 27

73	VDD	VDD	VDD	+5 VDC or +3.3 VDC
74	DQ28	DQ28	DQ28	Data 28
75	DQ29	DQ29	DQ29	Data 29
76	DQ30	DQ30	DQ30	Data 30
77	DQ31	DQ31	DQ31	Data 31
78	VSS	VSS	VSS	Ground
79	CK2	CK2	CK2	Clock signal 2
80	n/c	n/c	n/c	Not connected
81	n/c	n/c	n/c	Not connected
82	SDA	SDA	SDA	Serial Data
83	SCL	SCL	SCL	Serial Clock
84	VDD	VDD	VDD	+5 VDC or +3.3 VDC

## Back, Left

Pin	Non-Parity	72 ECC?	80 ECC?	Description
85	VSS	VSS	VSS	Ground
86	DQ32	DQ32	DQ32	Data 32
87	DQ33	DQ33	DQ33	Data 33
88	DQ34	DQ34	DQ34	Data 34
89	DQ35	DQ35	DQ35	Data 35
90	VDD	VDD	VDD	+5 VDC or +3.3 VDC
91	DQ36	DQ36	DQ36	Data 36
92	DQ37	DQ37	DQ37	Data 37
93	DQ38	DQ38	DQ38	Data 38
94	DQ39	DQ39	DQ39	Data 39
95	DQ40	DQ40	DQ40	Data 40
96	VSS	VSS	VSS	Ground
97	DQ41	DQ41	DQ41	Data 41
98	DQ42	DQ42	DQ42	Data 42
99	DQ43	DQ43	DQ43	Data 43



100	DQ44	DQ44	DQ44	Data 44
101	DQ45	DQ45	DQ45	Data 45
102	VDD	VDD	VDD	+5 VDC or +3.3 VDC
103	DQ46	DQ46	DQ46	Data 46
104	DQ47	DQ47	DQ47	Data 47
105	n/c	CB4	CB4	Parity/Check Bit Input/Output 4
106	n/c	CB5	CB5	Parity/Check Bit Input/Output 5
107	VSS	VSS	VSS	Ground
108	n/c	n/c	CB12	Parity/Check Bit Input/Output 12
109	n/c	n/c	CB13	Parity/Check Bit Input/Output 13
110	VDD	VDD	VDD	+5 VDC or +3.3 VDC
111	/CAS	/CAS	/CAS	Column Address Strobe
112	DQMB4	DQMB4	DQMB4	Byte Mask signal 4
113	DQMB5	DQMB5	DQMB5	Byte Mask signal 5
114	/S1	/S1	/S1	Chip Select 1
115	/RAS	/RAS	/RAS	Row Address Strobe
116	VSS	VSS	VSS	Ground
117	A1	A1	A1	Address 1
118	A3	A3	A3	Address 3
119	A5	A5	A5	Address 5
120	A7	A7	A7	Address 7
121	A9	A9	A9	Address 9
122	BA0	BA0	BA0	Bank Address 0
123	A11	A11	A11	Address 11
124	VDD	VDD	VDD	+5 VDC or +3.3 VDC
125	CK1	CK1	CK1	Clock signal 1
126	A12	A12	A12	Address 12

## Back, Right

Pin	Non-Parity	72 ECC?	80 ECC?	Description



127	VSS	VSS	VSS	Ground
128	CKE0	CKE0	CKE0	Clock Enable Signal 0
129	/S3	/S3	/S3	Chip Select 3
130	DQMB6	DQMB6	DQMB6	Byte Mask signal 6
131	DQMB7	DQMB7	DQMB7	Byte Mask signal 7
132	A13	A13	A13	Address 13
133	VDD	VDD	VDD	+5 VDC or +3.3 VDC
134	n/c	n/c	CB14	Parity/Check Bit Input/Output 14
135	n/c	n/c	CB15	Parity/Check Bit Input/Output 15
136	n/c	CB6	CB6	Parity/Check Bit Input/Output 6
137	n/c	CB7	CB7	Parity/Check Bit Input/Output 7
138	VSS	VSS	VSS	Ground
139	DQ48	DQ48	DQ48	Data 48
140	DQ49	DQ49	DQ49	Data 49
141	DQ50	DQ50	DQ50	Data 50
142	DQ51	DQ51	DQ51	Data 51
143	VDD	VDD	VDD	+5 VDC or +3.3 VDC
144	DQ52	DQ52	DQ52	Data 52
145	n/c	n/c	n/c	Not connected
146	Vref,NC	Vref,NC	Vref,NC	
147	n/c	n/c	n/c	Not connected
148	VSS	VSS	VSS	Ground
149	DQ53	DQ53	DQ53	Data 53
150	DQ54	DQ54	DQ54	Data 54
151	DQ55	DQ55	DQ55	Data 55
152	VSS	VSS	VSS	Ground
153	DQ56	DQ56	DQ56	Data 56
154	DQ57	DQ57	DQ57	Data 57
155	DQ58	DQ58	DQ58	Data 58
156	DQ59	DQ59	DQ59	Data 59
157	VDD	VDD	VDD	+5 VDC or +3.3 VDC
158	DQ60	DQ60	DQ60	Data 60

159	DQ61	DQ61	DQ61	Data 61
160	DQ62	DQ62	DQ62	Data 62
161	DQ63	DQ63	DQ63	Data 63
162	VSS	VSS	VSS	Ground
163	CK3	CK3	CK3	Clock signal 3
164	n/c	n/c	n/c	Not connected
165	SA0	SA0	SA0	Serial address 0
166	SA1	SA1	SA1	Serial address 1
167	SA2	SA2	SA2	Serial address 2
168	VDD	VDD	VDD	+5 VDC or +3.3 VDC

Contributor: [Joakim Ögren](#)

Source:

Various productsheets at [IBM Memory Products](#)

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# 30 pin SIMM

SIMM=Single Inline Memory Module.



(at the computer)

30 PIN SIMM at the computer.

Pin	Name	Description
1	VCC	+5 VDC
2	/CAS	Column Address Strobe
3	DQ0	Data 0
4	A0	Address 0
5	A1	Address 1
6	DQ1	Data 1
7	A2	Address 2
8	A3	Address 3
9	GND	Ground
10	DQ2	Data 2
11	A4	Address 4
12	A5	Address 5
13	DQ3	Data 3
14	A6	Address 6
15	A7	Address 7
16	DQ4	Data 4
17	A8	Address 8

18	A9	Address 9
19	A10	Address 10
20	DQ5	Data 5
21	/WE	Write Enable
22	GND	Ground
23	DQ6	Data 6
24	A11	Address 11
25	DQ7	Data 7
26	QP	Data Parity Out
27	/RAS	Row Address Strobe
28	/CASP	Something Parity ????
29	DP	Data Parity In
30	VCC	+5 VDC

*Note: SIMM above is a 4MBx9.*

*QP & DP is N/C on SIMMs without parity.*

*A9 is N/C on 256kB.*

*A10 is N/C on 256kB & 1MB. A11 is N/C on 256kB, 1MB & 4MB.*

*Contributor: [Joakim Ögren](#), [Helfried Behrendt](#)*

*Source:*

*[comp.sys.ibm.pc.hardware.\\* FAQ Part 4](#), maintained by [Ralph Valentino](#)*

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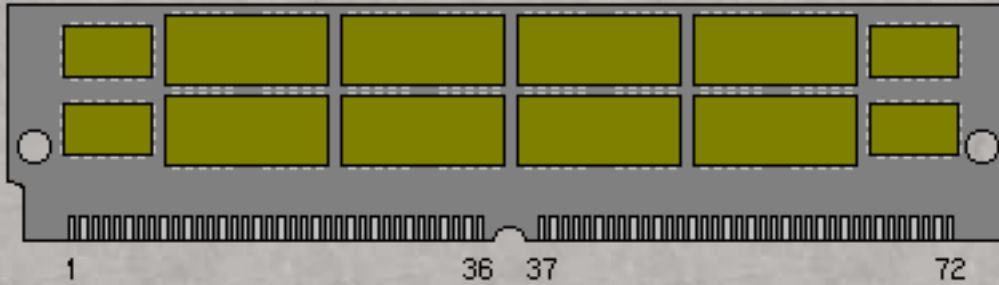




# 72 pin ECC SIMM

SIMM=Single Inline Memory Module

ECC=Error Correcting Code.



(at the computer)

72 PIN SIMM at the computer.

Pin	ECC	Optimized	Description
1	VSS	VSS	Ground
2	DQ0	DQ0	Data 0
3	DQ1	DQ1	Data 1
4	DQ2	DQ2	Data 2
5	DQ3	DQ3	Data 3
6	DQ4	DQ4	Data 4
7	DQ5	DQ5	Data 5
8	DQ6	DQ6	Data 6
9	DQ7	DQ7	Data 7
10	VCC	VCC	+5 VDC
11	PD5	PD5	Presence Detect 5
12	A0	A0	Address 0
13	A1	A1	Address 1
14	A2	A2	Address 2
15	A3	A3	Address 3

16	A4	A4	Address 4
17	A5	A5	Address 5
18	A6	A6	Address 6
19	n/c	n/c	Not connected
20	DQ8	DQ8	Data 8
21	DQ9	DQ9	Data 9
22	DQ10	DQ10	Data 10
23	DQ11	DQ11	Data 11
24	DQ12	DQ12	Data 12
25	DQ13	DQ13	Data 13
26	DQ14	DQ14	Data 14
27	DQ15	DQ15	Data 15
28	A7	A7	Address 7
29	DQ16	DQ16	Data 16
30	VCC	VCC	+5 VDC
31	A8	A8	Address 8
32	A9	A9	Address 9
33	n/c	n/c	Not connected
34	/RAS1	/RAS1	Row Address Strobe 1
35	DQ17	DQ17	Data 17
36	DQ18	DQ18	Data 18
37	DQ19	DQ19	Data 19
38	DQ20	DQ20	Data 20
39	VSS	VSS	Ground
40	/CAS0	/CAS0	Column Address Strobe 0
41	A10	A10	Address 10
42	A11	A11	Address 11
43	/CAS1	/CAS1	Column Address Strobe 1
44	/RAS0	/RAS0	Row Address Strobe 0
45	/RAS1	/RAS1	Row Address Strobe 1
46	DQ21	DQ21	Data 21
47	/WE	/WE	Read/Write

48	/ECC	/ECC	
49	DQ22	DQ22	Data 22
50	DQ23	DQ23	Data 23
51	DQ24	DQ24	Data 24
52	DQ25	DQ25	Data 25
53	DQ26	DQ26	Data 26
54	DQ27	DQ27	Data 27
55	DQ28	DQ28	Data 28
56	DQ29	DQ29	Data 29
57	DQ30	DQ30	Data 30
58	DQ31	DQ31	Data 31
59	VCC	VCC	+5 VDC
60	DQ32	DQ32	Data 32
61	DQ33	DQ33	Data 33
62	DQ34	DQ34	Data 34
63	DQ35	DQ35	Data 35
64	n/c	DQ36	Data 36
65	n/c	DQ37	Data 37
66	n/c	DQ38	Data 38
67	PD1	PD1	Presence Detect 1
68	PD2	PD2	Presence Detect 2
69	PD3	PD3	Presence Detect 3
70	PD4	PD4	Presence Detect 4
71	n/c	DQ39	Data 39
72	VSS	VSS	Ground

Contributor: [Joakim Ögren](#)

Source:

Various productsheets at [IBM Memory Products](#)

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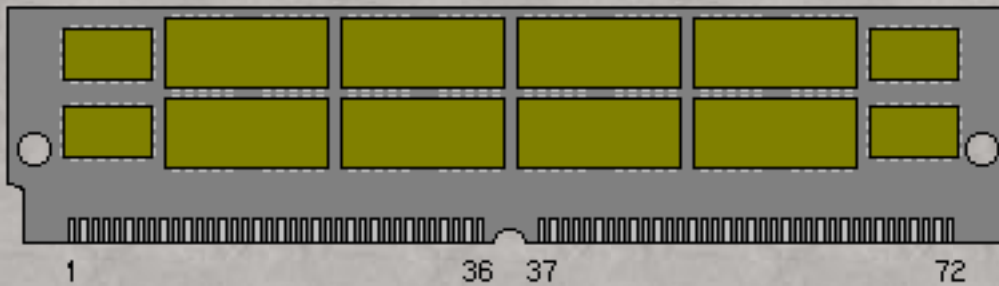
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# 72 pin SIMM

SIMM=Single Inline Memory Module



(at the computer)

72 PIN SIMM at the computer.

Pin	Non-Parity	Parity	Description
1	VSS	VSS	Ground
2	DQ0	DQ0	Data 0
3	DQ16	DQ16	Data 16
4	DQ1	DQ1	Data 1
5	DQ17	DQ17	Data 17
6	DQ2	DQ2	Data 2
7	DQ18	DQ18	Data 18
8	DQ3	DQ3	Data 3
9	DQ19	DQ19	Data 19
10	VCC	VCC	+5 VDC
11	n/c	n/c	Not connected
12	A0	A0	Address 0
13	A1	A1	Address 1
14	A2	A2	Address 2
15	A3	A3	Address 3
16	A4	A4	Address 4



17	A5	A5	Address 5
18	A6	A6	Address 6
19	A10	A10	Address 10
20	DQ4	DQ4	Data 4
21	DQ20	DQ20	Data 20
22	DQ5	DQ5	Data 5
23	DQ21	DQ21	Data 21
24	DQ6	DQ6	Data 6
25	DQ22	DQ22	Data 22
26	DQ7	DQ7	Data 7
27	DQ23	DQ23	Data 23
28	A7	A7	Address 7
29	A11	A11	Address 11
30	VCC	VCC	+5 VDC
31	A8	A8	Address 8
32	A9	A9	Address 9
33	/RAS3	/RAS3	Row Address Strobe 3
34	/RAS2	/RAS2	Row Address Strobe 2
35	n/c	PQ3	Parity bit 3 (for the 3rd byte, bits 16-23)
36	n/c	PQ1	Parity bit 1 (for the 1st byte, bits 0-7)
37	n/c	PQ2	Parity bit 2 (for the 2nd byte, bits 8-15)
38	n/c	PQ4	Parity bit 4 (for the 4th byte, bits 24-31)
39	VSS	VSS	Ground
40	/CAS0	/CAS0	Column Address Strobe 0
41	/CAS2	/CAS2	Column Address Strobe 2
42	/CAS3	/CAS3	Column Address Strobe 3
43	/CAS1	/CAS1	Column Address Strobe 1
44	/RAS0	/RAS0	Row Address Strobe 0
45	/RAS1	/RAS1	Row Address Strobe 1
46	n/c	n/c	Not connected
47	/WE	/WE	Read/Write
48	n/c	n/c	Not connected

49	DQ8	DQ8	Data 8
50	DQ24	DQ24	Data 24
51	DQ9	DQ9	Data 9
52	DQ25	DQ25	Data 25
53	DQ10	DQ10	Data 10
54	DQ26	DQ26	Data 26
55	DQ11	DQ11	Data 11
56	DQ27	DQ27	Data 27
57	DQ12	DQ12	Data 12
58	DQ28	DQ28	Data 28
59	VCC	VCC	+5 VDC
60	DQ29	DQ29	Data 29
61	DQ13	DQ13	Data 13
62	DQ30	DQ30	Data 30
63	DQ14	DQ14	Data 14
64	DQ31	DQ31	Data 31
65	DQ16	DQ16	Data 16
66	n/c	n/c	Not connected
67	PD1	PD1	Presence Detect 1
68	PD2	PD2	Presence Detect 2
69	PD3	PD3	Presence Detect 3
70	PD4	PD4	Presence Detect 4
71	n/c	n/c	Not connected
72	VSS	VSS	Ground

## Size:

PD2	PD1	Size
GND	GND	4 or 64 MB
GND	NC	2 or 32 MB
NC	GND	1 or 16 MB

NC	NC	8 MB
----	----	------

## Accesstime:

PD4	PD3	Accesstime
GND	GND	50, 100 ns
GND	NC	80 ns
NC	GND	70 ns
NC	NC	60 ns

*Notes: A9 is a N/C on 256k and 512k modules.*

*A10 is a N/C on 256k, 512k, 1M and 4M modules.*

*RAS1/RAS3 are N/C on 256k, 1M and 4M modules.*

*Contributor: [Joakim Ögren](#), [Mark Brown](#), [Karsten Wenke](#), [SOYO Computer Inc](#)*

*Source:*

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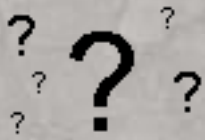
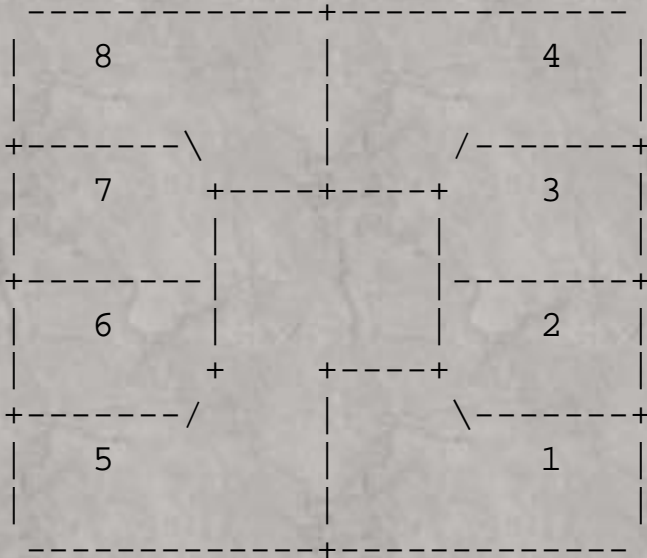
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# SmartCard AFNOR



(at the card)

UNKNOWN CONNECTOR at the card.

Pin	Name	Description
1	VCC	+5 VDC
2	R/W	Read/Write
3	CLOCK	Clock
4	RESET	Reset
5	GND	Ground
6	VPP	+21 VDC
7	I/O	In/Out
8	FUSE	Fuse

Contributor: [Joakim Ögren](#)



*Source:*

*Telecard/Smartcard Technical Spec & Info by [Stephane Bausson](#)*

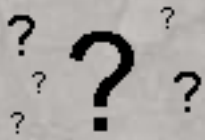
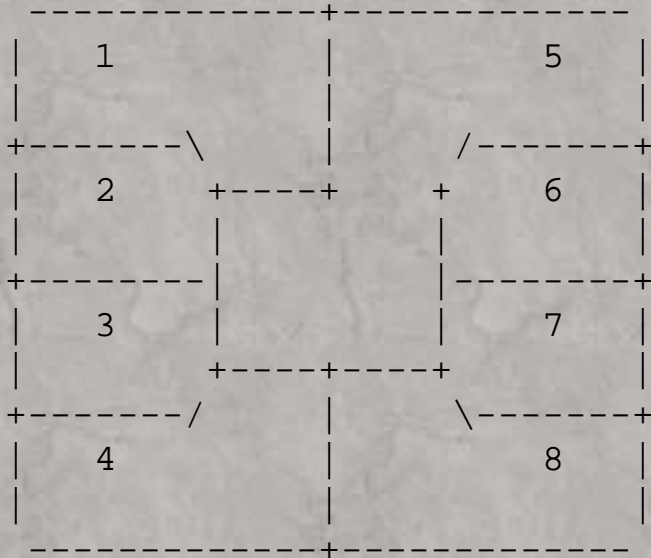
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# SmartCard ISO

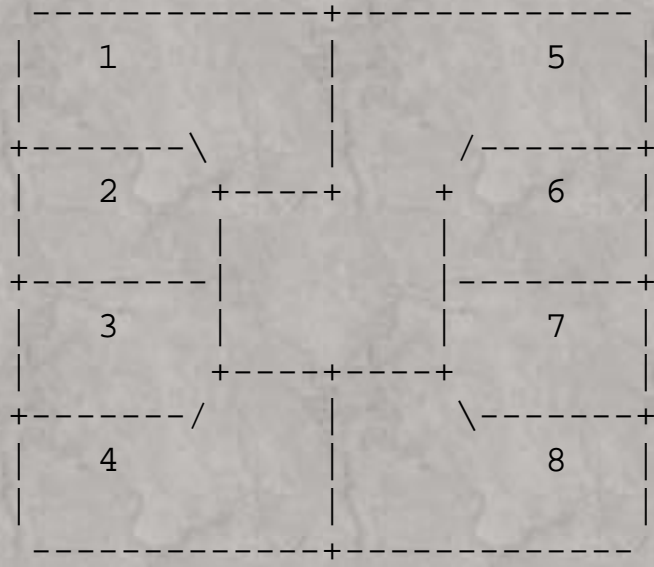


(at the card)

UNKNOWN CONNECTOR at the card.

Pin	Name	Description
1	VCC	+5 VDC
2	R/W	Read/Write
3	CLOCK	Clock
4	RESET	Reset
5	GND	Ground
6	VPP	+21 VDC
7	I/O	In/Out
8	FUSE	Fuse

# SmartCard ISO 7816-2



Pin	Name	Description
1	VCC	+5 VDC
2	RESET	Reset
3	CLOCK	Clock
4	n/c	Not connected
5	GND	Ground
6	n/c	Not connected
7	I/O	In/Out
8	n/c	Not connected

Contributor: [Joakim Ögren](#)

Source:

Telecard/Smartcard Technical Spec & Info by [Stephane Bausson](#)

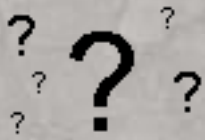
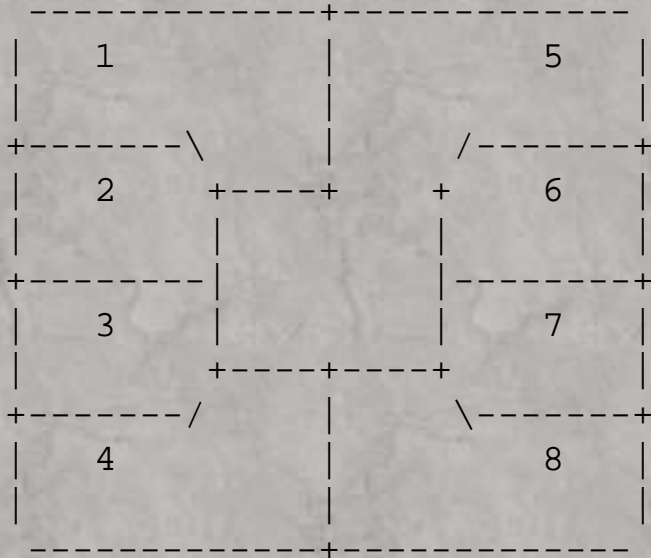
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# SmartCard ISO 7816-2



(at the card)

UNKNOWN CONNECTOR at the card.

Pin	Name	Description
1	VCC	+5 VDC
2	RESET	Reset
3	CLOCK	Clock
4	n/c	Not connected
5	GND	Ground
6	n/c	Not connected
7	I/O	In/Out
8	n/c	Not connected

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# 72 pin SO DIMM

SO DIMM=Small Outline Dual Inline Memory Module

**NOT  
DRAWN  
YET...**



(at the computer)

72 PIN SO DIMM at the computer.

Pin	Non-Parity	Parity	Description
1	VSS	VSS	Ground
2	DQ0	DQ0	Data 0
3	DQ1	DQ1	Data 1
4	DQ2	DQ2	Data 2
5	DQ3	DQ3	Data 3
6	DQ4	DQ4	Data 4
7	DQ5	DQ5	Data 5
8	DQ6	DQ6	Data 6
9	DQ7	DQ7	Data 7
10	VCC	VCC	+5 VDC
11	PD1	PD1	Presence Detect 1
12	A0	A0	Address 0
13	A1	A1	Address 1
14	A2	A2	Address 2
15	A3	A3	Address 3
16	A4	A4	Address 4
17	A5	A5	Address 5
18	A6	A6	Address 6

19	A10	A10	Address 10
20	n/c	PQ8	Data 8 (Parity 1)
21	DQ9	DQ9	Data 9
22	DQ10	DQ10	Data 10
23	DQ11	DQ11	Data 11
24	DQ12	DQ12	Data 12
25	DQ13	DQ13	Data 13
26	DQ14	DQ14	Data 14
27	DQ15	DQ15	Data 15
28	A7	A7	Address 7
29	A11	A11	Address 11
30	VCC	VCC	+5 VDC
31	A8	A8	Address 8
32	A9	A9	Address 9
33	/RAS3	RAS3	Row Address Strobe 3
34	/RAS2	RAS2	Row Address Strobe 2
35	DQ16	DQ16	Data 16
36	n/c	PQ17	Data 17 (Parity 2)
37	DQ18	DQ18	Data 18
38	DQ19	DQ19	Data 19
39	VSS	VSS	Ground
40	/CAS0	CAS0	Column Address Strobe 0
41	/CAS2	CAS2	Column Address Strobe 2
42	/CAS3	CAS3	Column Address Strobe 3
43	/CAS1	CAS1	Column Address Strobe 1
44	/RAS0	RAS0	Row Address Strobe 0
45	/RAS1	RAS1	Row Address Strobe 1
46	A12	A12	Address 12
47	/WE	WE	Read/Write
48	A13	A13	Address 13
49	DQ20	DQ20	Data 20
50	DQ21	DQ21	Data 21

51	DQ22	DQ22	Data 22
52	DQ23	DQ23	Data 23
53	DQ24	DQ24	Data 24
54	DQ25	DQ25	Data 25
55	n/c	PQ26	Data 26 (Parity 3)
56	DQ27	DQ27	Data 27
57	DQ28	DQ28	Data 28
58	DQ29	DQ29	Data 29
59	DQ31	DQ31	Data 31
60	DQ30	DQ30	Data 30
61	VCC	VCC	+5 VDC
62	DQ32	DQ32	Data 32
63	DQ33	DQ33	Data 33
64	DQ34	DQ34	Data 34
65	n/c	PQ35	Data 35 (Parity 4)
66	PD2	PD2	Presence Detect 2
67	PD3	PD3	Presence Detect 3
68	PD4	PD4	Presence Detect 4
69	PD5	PD5	Presence Detect 1
70	PD6	PD6	Presence Detect 6
71	PD7	PD7	Presence Detect 7
72	VSS	VSS	Ground

Contributor: [Joakim Ögren](#), [Mark Brown](#), [Jim Burd](#)

Source:

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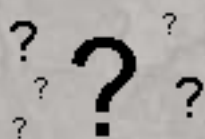
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# CDTV Memory Card

```
1111111111222222222233333333334
1234567890123456789012345678901234567890
+-----+
| 0000000000000000000000000000000000000000 |
+-----+
```



(at the computer)

40 PIN ??? CONNECTOR at the computer.

Pin	Name	Description
1	D0	Data Bus 0
2	D1	Data Bus 1
3	D2	Data Bus 2
4	D3	Data Bus 3
5	D4	Data Bus 4
6	D5	Data Bus 5
7	D6	Data Bus 6
8	D7	Data Bus 7
9	D8	Data Bus 8
10	D9	Data Bus 9
11	D10	Data Bus 10
12	D11	Data Bus 11
13	D12	Data Bus 12
14	D13	Data Bus 13
15	D14	Data Bus 14

16	D15	Data Bus 15
17	A1	Address Bus 1
18	A2	Address Bus 2
19	A3	Address Bus 3
20	A4	Address Bus 4
21	A5	Address Bus 5
22	A6	Address Bus 6
23	A7	Address Bus 7
24	A8	Address Bus 8
25	A9	Address Bus 9
26	A10	Address Bus 10
27	A11	Address Bus 11
28	A12	Address Bus 12
29	A13	Address Bus 13
30	A14	Address Bus 14
31	A15	Address Bus 15
32	A16	Address Bus 16
33	A17	Address Bus 17
34	R/W	Read/Write (High=Read)
35	/CSMCOD	Chip Select Odd Bytes
36	/CSMCEN	Chip Select Even Bytes
37	VCC	+5 Volts DC
38	GND	Ground
39	A18	Address Bus 18 (Short J16 to connect A18 to processor bus)
40	A19	Address Bus 19 (Short J17 to connect A19 to processor bus)

*Note: Address space=\$E00000-\$E7FFFF*

*Contributor: [Joakim Ögren](#)*

*Source:  
Darren Ewaniuk's CDTV Technical Information*

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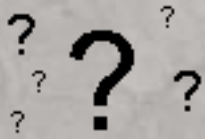


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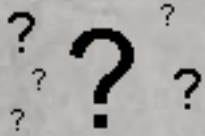
Developed by SanDisk.

Is compatible with PC-Card ATA with a simple passive adapter.

See [PC-Card ATA](#) for more information.



(at the controller)



(at the peripherals)

50 PIN ??? MALE at the controller.

50 PIN ??? FEMALE at the peripherals.

Pin	Name	Description
1	GND	Ground
2	D3	Data 3
3	D4	Data 4
4	D5	Data 5
5	D6	Data 6
6	D7	Data 7
7	/CE1	Card Enable 1
8	A10	Address 10
9	/OE	Output Enable
10	A9	Address 9
11	A8	Address 8
12	A7	Address 7



13	VCC	+5V
14	A6	Address 6
15	A5	Address 5
16	A4	Address 4
17	A3	Address 3
18	A2	Address 2
19	A1	Address 1
20	A0	Address 0
21	D0	Data 0
22	D1	Data 1
23	D2	Data 2
24	/WP:/IOIS16	Write Protect : IOIS16
25	/CD2	Card Detect 2
26	/CD1	Card Detect 1
27	D0	Data 0
28	D0	Data 0
29	D0	Data 0
30	D0	Data 0
31	D0	Data 0
32	/CE2	Card Enable 2
33	/VS1	Refresh
34	/IORD	I/O Read
35	/IOWR	I/O Write
36	/WE	Write Enable
37	/READY:/RDY:/IREQ	Ready : Busy : IREQ
38	VCC	+5V
39	CSEL	
40	/VS2	RFU
41	RESET	Reset
42	/WAIT	Wait
43	/INPACK	
44	/REG	Register Select

45	/BVD2:SPKR	Battery Voltage Detect 2 : SPKR
46	/BVD1:STSCHG	Battery Voltage Detect 1 : STSCHG
47	D8	Data 8
48	D9	Data 9
49	D10	Data 10
50	GND	Ground

Contributor: [Joakim Ögren](#)

Source:

*SanDisk's CompactFlash ABC at [SanDisk's homepage](#)*

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*Document last modified: 2001-06-08*



# Power Mac L2 Cache

PowerMac 7200, 7500, 8500, 9500

160 PIN UNKNOWN CONNECTOR

Pin	Name
1	+5 V
2	GND
3	D0
4	D2
5	D4
6	D6
7	GND
8	D8
9	D10
10	D12
11	D14
12	GND
13	+5 V
14	GND
15	D16
16	D18
17	D20
18	D22
19	GND
20	D24
21	D26
22	D28

23	D30
24	GND
25	+5 V
26	GND
27	T0
28	T2
29	T4
30	T6
31	GND
32	T8
33	T10
34	T12
35	T14
36	GND
37	+5 V
38	GND
39	CLK
40	GND
41	/TOEN
42	/TWEN
43	/ADV
44	A12
45	CSIZ(1)
46	A14
47	A16
48	A18
49	A20
50	GND
51	A22
52	A24
53	A26
54	A28



55	GND
56	+5 V
57	GND
58	D32
59	D34
60	D36
61	D38
62	GND
63	D40
64	D42
65	D44
66	D46
67	GND
68	+5 V
69	GND
70	D48
71	D50
72	D52
73	D54
74	GND
75	D56
76	D58
77	D60
78	D62
79	GND
80	+5 V
81	+3.3 V
82	GND
83	D1
84	D3
85	D5
86	D7

87	GND
88	D9
89	D11
90	D13
91	D15
92	GND
93	+3.3 V
94	GND
95	D17
96	D19
97	D21
98	D23
99	GND
100	D25
101	D27
102	D29
103	D31
104	GND
105	+3.3 V
106	GND
107	T1
108	T3
109	T5
110	T7
111	GND
112	T9
113	T11
114	T13
115	T15
116	GND
117	+3.3 V
118	GND

119	CPRES
120	A11
121	/DOEN
122	/DWEN
123	/ADSC
124	/CSIZ(2)
125	GND
126	A13
127	A15
128	A17
129	A19
130	GND
131	A21
132	A23
133	A25
134	A27
135	GND
136	+3.3 V
137	D33
138	D35
139	D35
140	D37
141	D39
142	GND
143	D41
144	D43
145	D45
146	D47
147	GND
148	+3.3 V
149	GND
150	D49

151	D51
152	D53
153	D55
154	GND
155	D57
156	D59
157	D61
158	D63
159	GND
160	+3.3 V

*Contributor:* [Joakim Ögren](#)

*Source:*  
[Apple Tech Info Library 18547: Power Macintosh 7200, 7500, 8500, 9500 Pinouts](#) at [Apple TIL homepage](#)

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*Document last modified:* 2001-06-08





# Atari ACSI DMA

Used to connect Laser printers or Harddrives.

**NOT  
DRAWN  
YET...**



(at the Computer)

**NOT  
DRAWN  
YET...**



(at the Devices)

19 PIN D-SUB ?? at the Computer.

19 PIN D-SUB ?? at the Devices.

Pin	Name	Description
1	D0	Data 0
2	D1	Data 1
3	D2	Data 2
4	D3	Data 3
5	D4	Data 4
6	D5	Data 5
7	D6	Data 6
8	D7	Data 7
9	/CS	Chip Select
10	IRQ	Interrupt Request
11	GND	Ground
12	/RST	Reset
13	GND	Ground
14	ACK	Acknowledge

15	GND	Ground
16	A1	?
17	GND	Ground
18	R/W	Read/Write
19	REQ	Data Request

*Contributor:* [Joakim Ögren](#), [Lawrence Wright](#), [Steve & Sally Blair](#)

*Source:*  
?

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*Document last modified:* 2001-06-07



# Triplite OmniPro 675 UPS

Unknown connector

Pin	Description
1	Common/Negative
2	External inverter shutdown, positive side
3	line fail, normaly open contact
4	return/external inverter shutdown negative side
5	line fail, normaly closed contact
6	low battery, positive side (2 minute warning)

Contributor: [Joakim Ögren](#)

Source:

[Triplite OmniPro 675 UPS pinout](#) at [The Pin-Out directory](#)

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# UPS YUNTO P Series (250/500/750/1250)



(at the UPS)

9 PIN D-SUB FEMALE at the UPS.

Pin	Name	Dir	Description
1	Battery Mode	out	This pin is shorted to PIN 5 (ground) if the mains power supply fails or is out of tolerance. (NORMALLY OPEN)
2	-	-	-
3	-	-	-
4	-	-	-
5	Ground	-	Ground terminal and common root of contacts at PIN 1, 8 and 9
6	-	-	-
7	UPS shut-down	IN	If a positive signal level (+5V to +12V DC) is applied, the UPS system switches off (PIN 5 is ground)
8	Battery Capacity Low	OUT	This pin is shorted to PIN 5 (ground) if the batteries have been discharged to such an extent that the remaining stored energy time is less than 2 minutes. (NORMALLY OPEN)
9	Battery Mode	OUT	The connection between this pin and PIN 5 (ground) is disconnected if the main power supply fails or is out of tolerance. (NORMALLY CLOSED)

*Note: Direction is relative to UPS.*

Contributor: [Joakim Ögren](#)

Source:  
?



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*Document last modified: 2000-07-09*



# Apple AUI (AAUI)

0.050-inch-spaced ribbon contact connector.

Pin	Name	Description
1	FN Pwr	Power (+12V @ 2.1W or +5V @ 1.9W)
2	DI-A	Data In circuit A
3	DI-B	Data In circuit B
4	VCC	Voltage Common
5	CI-A	Control In circuit A
6	CI-B	Control In circuit B
7	+5V	+5 volts (from host)
8	+5V	Secondary +5 volts (from host)
9	DO-A	Data Out circuit A
10	DO-B	Data Out circuit B
11	VCC	Secondary Voltage Common
12	NC	Reserved
13	NC	Reserved
14	FN Pwr	Secondary +12V @ 2.1W or +5V @ 1.9W
Shell	Protective Gnd	Protective Ground

Available on Macintosh Quadra computers, Apple Ethernet NB Card, and LaserWriter IIg printers?

Contributor: [Joakim Ögren](#)

Source:

[Apple Tech Info Library 8863](#) at [Apple TIL homepage](#)

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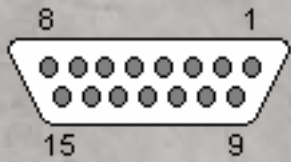
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Document last modified: 2001-06-07



# AUI

Is the directions right???



(at the Ethernet card)

15 PIN D-SUB FEMALE at the Ethernet card.

Pin	Description
1	control in circuit shield
2	control in circuit A
3	data out circuit A
4	data in circuit shield
5	data in circuit A
6	voltage common
7	?
8	control out circuit shield
9	control in circuit B
10	data out circuit B
11	data out circuit shield
12	data in circuit B
13	voltage plus
14	voltage shield
15	?

Contributor: [Joakim Ögren](#)

Source:

[Tommy's pinout Collection](#) by [Tommy Johnson](#)

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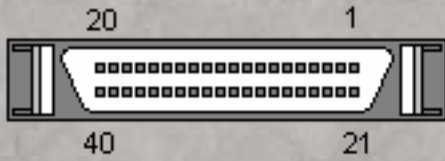
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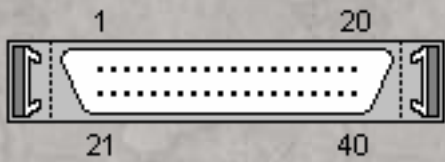




# Media Independent Interface (MII)



(at the network device).



























(at the transceiver).

40 PIN HI-DENSITY D-SUB FEMALE at the network device.

40 PIN HI-DENSITY D-SUB MALE at the transceiver.

Pin	Name	Dir	Description
1	V	→	+5 Vdc/ 3.3 Vdc
2	MDIO	↔	MII Data Input/Output
3	MDC	→	MII Data Clock
4	RxD	←	Rx Data
5	RxD	←	Rx Data
6	RxD	←	Rx Data
7	RxD	←	Rx Data
8	Rx_DV	←	Rx Data Valid
9	Rx_CLK	←	Rx Clock
10	Rx_ER	←	Rx Error
11	Tx_ER	→	Tx Error
12	Tx_CLK	←	Tx Clock
13	Tx_EN	→	Tx Enable
14	TxD	→	Tx Data
15	TxD	→	Tx Data
16	TxD	→	Tx Data

17	TxD		Tx Data
18	COL		Collision
19	CRS		Carrier Sense
20	V		+5 Vdc/ +3.3 Vdc
21	V		+5 Vdc/ +3.3 Vdc
22	GND		Ground
23	GND		Ground
24	GND		Ground
25	GND		Ground
26	GND		Ground
27	GND		Ground
28	GND		Ground
29	GND		Ground
30	GND		Ground
31	GND		Ground
32	GND		Ground
33	GND		Ground
34	GND		Ground
35	GND		Ground
36	GND		Ground
37	GND		Ground
38	GND		Ground
39	GND		Ground
40	V		+5 Vdc/ +3.3 Vdc

*Note: Direction is DTE (Network device) relative DCE (Transciever).*

*Contributor:* [Joakim Ögren](#), [Mark S Stephenson](#)

*Source:*

[Ethernet \(IEEE802.3\) page](#) at [Connectivity Knowledge Platform \(Made IT\)](#)

*A Tech Doc* at [Cisco Systems](#)

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Document last modified: 2001-06-08*



# SUN AUI

26 PIN HI-DENSITY D-SUB FEMALE at the motherboard.

26 PIN HI-DENSITY D-SUB MALE at the cable.

Available on the SUN SPARCEngine 5 motherboard

Pin	Name
1	Transmit -
2	Receive +
3	Collision -
4	AUI Power
5	N/C
6	N/C
7	N/C
8	N/C
9	N/C
10	N/C
11	N/C
12	N/C
13	N/C
14	Transmit +
15	Receive -
16	Collision +
17	Ground
18	N/C
19	N/C
20	N/C
21	N/C



22	N/C
23	Ground
24	Ground
25	N/C
26	Ground

*Contributor:* [Joakim Ögren](#)

*Source:*  
[SUN SPARCEngine 5 manual](#) at [SUN manuals site](#)

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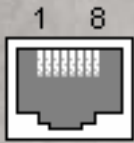
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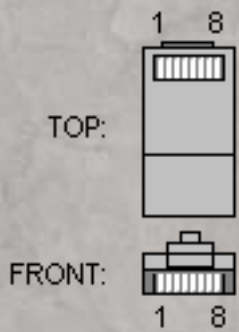


# Ethernet 10/100Base-T

Same connector and pinout for both 10Base-T and 100Base-TX.



(at the network interface cards/hubs)



(at the cables)

RJ45 FEMALE CONNECTOR at the network interface cards/hubs.

RJ45 MALE CONNECTOR at the cables.

Pin	Name	Description
1	TX+	Transmit Data+
2	TX-	Transmit Data-
3	RX+	Receive Data+
4	n/c	Not connected
5	n/c	Not connected
6	RX-	Receive Data-
7	n/c	Not connected
8	n/c	Not connected

*Note: TX & RX are swapped on Hub's.*

Contributor: [Joakim Ögren](#), [Jeffrey R. Broido](#)

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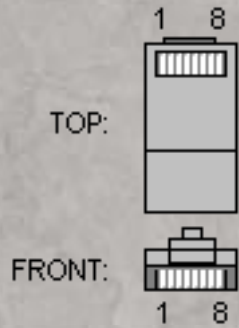


# Ethernet 1000Base-T

1000 Base-T uses all pairs for bidirectional traffic in the RJ45 connector. Cables used should be of Category 5e(nhanced), even though Category 5 cables usually works too.



(at the network interface cards/hubs)



(at the cables)

RJ45 FEMALE CONNECTOR at the network interface cards/hubs.

RJ45 MALE CONNECTOR at the cables.

Pin	Name	Description
1	BI_DA+	Bi-directional pair A +
2	BI_DA-	Bi-directional pair A -
3	BI_DB+	Bi-directional pair B +
4	BI_DC+	Bi-directional pair C +
5	BI_DC-	Bi-directional pair C -
6	BI_DB-	Bi-directional pair B -
7	BI_DD+	Bi-directional pair D +
8	BI_DD-	Bi-directional pair D -

Contributor: [Niklas Edmundsson](#),



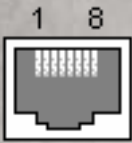
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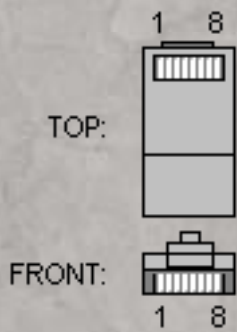


# Ethernet 100Base-T4

100Base-T4 uses all four pairs. 100Base-TX only uses two pairs.



(at the network interface cards/hubs)



(at the cables)

RJ45 FEMALE CONNECTOR at the network interface cards/hubs.

RJ45 MALE CONNECTOR at the cables.

Pin	Name	Description
1	TX_D1+	Tranceive Data+
2	TX_D1-	Tranceive Data-
3	RX_D2+	Receive Data+
4	BI_D3+	Bi-directional Data+
5	BI_D3-	Bi-directional Data-
6	RX_D2-	Receive Data-
7	BI_D4+	Bi-directional Data+
8	BI_D4-	Bi-directional Data-

*Note: TX & RX are swapped on Hub's. Don't know about Bi-directional data.*

Contributor: [Joakim Ögren](#), [Kim Scholte](#)

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# Network Information

## Networking standards

### 10Base-T (Standard Ethernet)

- Speed: 10 Mbit/s
- Connectors: RJ45
- Cables: Twisted Pair (category 3)
- Wiring scheme: EIA/TIA 568B
- Maximum cable length: 100 m
- Star Topology

### 100Base-T (Fast Ethernet)

- Speed: 100 Mbit/s
- Connectors: RJ45
- Cables: Twisted Pair (category 5)
- Wiring scheme: EIA/TIA 568B
- Maximum cable length: 100 m
- Star Topology

### 1000Base-T (Gigabit Ethernet)

- Speed: 1000 Mbit/s
- Connectors: RJ45
- Cables: Twisted Pair (category 5 Enhanced)
- Wiring scheme: EIA/TIA 568B
- Maximum cable length: 100 m
- Star Topology

### 10Base-2 (Thin Ethernet)

- Speed: 10 Mbit/s
- Connectors: BNC



- Cables: RG58 (50 ohm)
- Maximum cable segment length: 185 m
- Maximum devices per cable segment: 30
- Minimum distance between devices: 0.3 m?
- Bus Topology
- Terminators in each end: 50 ohm

## 10Base-5 (Thick Ethernet)

- Speed: 10 Mbit/s
- Connectors: N-Type
- Cables: RG8
- Wiring scheme: EIA/TIA 568B
- Maximum cable length: 500 m
- Maximum devices per cable segment: 100
- Minimum distance between devices: 2.5 m
- Bus Topology
- Terminators in each end: 50 ohm

## TokenRing

- Speed: 4 or 16 Mbit/s
- Connectors: RJ45 or IBM Data Connector
- Cables: Twisted Pair (category 3)
- Maximum ring length: 168m at 16Mbit/s, 360 m at 4Mbit/s
- Maximum cable length: Depends on ring length and network layout
- Maximum devices per network: 72 (UTP) or 250-260 (Type1)
- Token based ring Topology (physical star, logical ring)

## Cabeling

### Twisted Pair

Category type	Bandwidth	Typical speed
Category 3	16 MHz	16 Mbit/s
Category 4	20 MHz	20 Mbit/s
Category 5	125 MHz	100 Mbit/s
Category 5 Enhanced	125 MHz	100 Mbit/s (1000Mbit/s with 1000BaseT)

*Contributors:* [Joakim Ögren](#)

*Source:*  
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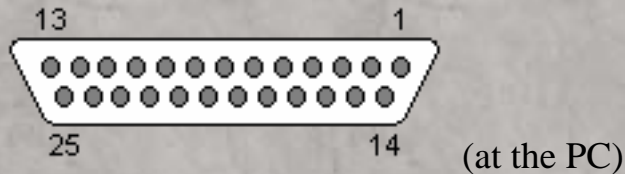
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


# ECP Parallel

ECP = Extended Capabilities Port



25 PIN D-SUB FEMALE at the PC.

Pin	Name	Dir	Description
1	nStrobe	→	Strobe
2	data0	↔	Address, Data or RLE Data Bit 0
3	data1	↔	Address, Data or RLE Data Bit 1
4	data2	↔	Address, Data or RLE Data Bit 2
5	data3	↔	Address, Data or RLE Data Bit 3
6	data4	↔	Address, Data or RLE Data Bit 4
7	data5	↔	Address, Data or RLE Data Bit 5
8	data6	↔	Address, Data or RLE Data Bit 6
9	data7	↔	Address, Data or RLE Data Bit 7
10	/nAck	←	Acknowledge
11	Busy	←	Busy
12	PError	←	Paper End
13	Select	←	Select
14	/nAutoFd	→	Autofeed
15	/nFault	←	Error
16	/nInit	→	Initialize
17	/nSelectIn	→	Select In
18	GND	—	Signal Ground

19	GND		Signal Ground
20	GND		Signal Ground
21	GND		Signal Ground
22	GND		Signal Ground
23	GND		Signal Ground
24	GND		Signal Ground
25	GND		Signal Ground

*Note: Direction is Computer relative Device.*

*Contributor: [Joakim Ögren](#), [Marco Furter](#)*

*Source:  
Microsoft MSDN Library: [Extended Capabilities Port Specs](#)*

*Info: [Microsoft MSDN Library](#)*

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# ECP Parallel (technical)

This file is designed to give a basic overview of the port found in most newer PC computers called ECP Parallel port.

This file is not intended to be a thorough coverage of the standard. It is for informational purposes only, and is intended to give designers and hobbyists sufficient information to design their own ECP compatible devices.

## Signal Descriptions:

### **nStrobe**

This signal registers data or address into the slave on the asserting edge during .

### **data 0-7**

Contains address, data or RLE data. Can be used in both directions.

### **nAck**

Valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.

### **Busy**

This signal deasserts to indicate that the peripheral can accept data. In forward direction this handshakes with nStrobe. In the reverse direction this signal indicates that the data is RLE compressed by being low.

### **PError**

Used to acknowledge a change in the direction of transfer. High=Forward.

### **Select**

Printer is online.

## nAutoFd

Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data.

## nFault

Generates an error interrupt when asserted.

## nInit

Sets the transfer direction. High=Reverse, Low=Forward.

## nSelectIn

Low in ECP mode.

*Contributor:* [Joakim Ögren](#), [Rob Gill](#)

*Source:*

*Microsoft MSDN Library: Extended Capabilities Port Specs*

*Info:* [Microsoft MSDN Library](#)

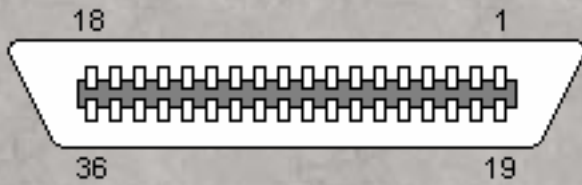
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















# IEEE1284-B



(at the Printer)

36 PIN CENTRONICS FEMALE at the Printer.

Pin	Name	Dir	Description
1	nStrobe	→	Strobe
2	data0	↔	Address, Data or RLE Data Bit 0
3	data1	↔	Address, Data or RLE Data Bit 1
4	data2	↔	Address, Data or RLE Data Bit 2
5	data3	↔	Address, Data or RLE Data Bit 3
6	data4	↔	Address, Data or RLE Data Bit 4
7	data5	↔	Address, Data or RLE Data Bit 5
8	data6	↔	Address, Data or RLE Data Bit 6
9	data7	↔	Address, Data or RLE Data Bit 7
10	/nAck	←	Acknowledge
11	Busy	←	Busy
12	PErr	←	Paper End
13	Select	←	Select
14	/nAutoFd	→	Autofeed
15	GND	—	Signal Ground
16	GND	—	Signal Ground
17	GND	—	Signal Ground
18	GND	—	Signal Ground
19	GND	—	Signal Ground

20	GND		Signal Ground
21	GND		Signal Ground
22	GND		Signal Ground
23	GND		Signal Ground
24	GND		Signal Ground
25	GND		Signal Ground
26	GND		Signal Ground
27	GND		Signal Ground
28	GND		Signal Ground
29	GND		Signal Ground
30	GND		Signal Ground
31	/nInit		Initialize
32	/nFault		Error
33	GND		Signal Ground
34	GND		Signal Ground
35	GND		Signal Ground
36	/nSelectIn		Select In

*Note: Direction is Computer relative Device.*

Contributor: [Joakim Ögren](#)

Source:  
?

Info: [Microsoft MSDN Library](#)

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














# IEEE1284-C

36 PIN HI-DENSITY CENTRONICS???

Pin	Name	Dir	Description
1	Busy	←	Busy
2	Select	←	Select
3	/nAck	←	Acknowledge
4	/nFault	←	Error
5	PError	←	Paper End
6	data0	↔	Address, Data or RLE Data Bit 0
7	data1	↔	Address, Data or RLE Data Bit 1
8	data2	↔	Address, Data or RLE Data Bit 2
9	data3	↔	Address, Data or RLE Data Bit 3
10	data4	↔	Address, Data or RLE Data Bit 4
11	data5	↔	Address, Data or RLE Data Bit 5
12	data6	↔	Address, Data or RLE Data Bit 6
13	data7	↔	Address, Data or RLE Data Bit 7
14	/nInit	→	Initialize
15	nStrobe	→	Strobe
16	/nSelectIn	→	Select In
17	/nAutoFd	→	Autofeed
18	GND	—	Signal Ground
19	GND	—	Signal Ground
20	GND	—	Signal Ground
21	GND	—	Signal Ground
22	GND	—	Signal Ground
23	GND	—	Signal Ground
24	GND	—	Signal Ground

25	GND		Signal Ground
26	GND		Signal Ground
27	GND		Signal Ground
28	GND		Signal Ground
29	GND		Signal Ground
30	GND		Signal Ground
31	GND		Signal Ground
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35	GND		Signal Ground
36	GND		Signal Ground

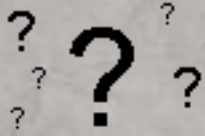
*Note: Direction is Computer relative Device.*

*Contributor: [Joakim Ögren](#), [Marco Furter](#)*

*Source:*



# MSX Parallel



(at the Computer)

14 PIN CENTRONICS FEMALE at the Computer.

Pin	Name	Dir	Description
1	/STB	→	Strobe
2	PDB0	→	Data 0
3	PDB1	→	Data 1
4	PDB2	→	Data 2
5	PDB3	→	Data 3
6	PDB4	→	Data 4
7	PDB5	→	Data 5
8	PDB6	→	Data 6
9	PDB7	→	Data 7
10	n/c	-	
11	BUSY	←	Printer is busy
12	n/c	-	
13	n/c	-	
14	GND	-	Signal Ground

*Note: Direction is Computer relative Printer.*

Contributor: [Joakim Ögren](#)

Source:  
Mayer's SV738 X'press I/O map

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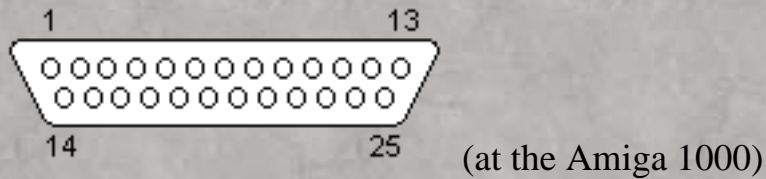
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





# Parallel (Amiga 1000)



25 PIN D-SUB MALE at the Amiga 1000.

Pin	Name	Dir	Description
1	/STROBE	→	Strobe
2	D0	↔	Data Bit 0
3	D1	↔	Data Bit 1
4	D2	↔	Data Bit 2
5	D3	↔	Data Bit 3
6	D4	↔	Data Bit 4
7	D5	↔	Data Bit 5
8	D6	↔	Data Bit 6
9	D7	↔	Data Bit 7
10	/ACK	←	Acknowledge
11	BUSY	↔	Busy
12	POUT	↔	Paper Out
13	SEL	↔	Select (Shared with RS232 RING-indicator)
14	GND	—	Signal Ground
15	GND	—	Signal Ground
16	GND	—	Signal Ground
17	GND	—	Signal Ground
18	GND	—	Signal Ground
19	GND	—	Signal Ground
20	GND	—	Signal Ground

21	GND		Signal Ground
22	GND		Signal Ground
23	+5V		+5 Volts DC (10 mA max)
24	n/c	-	Not connected.
25	/RESET		Reset

*Note: Direction is Computer relative Peripheral.*

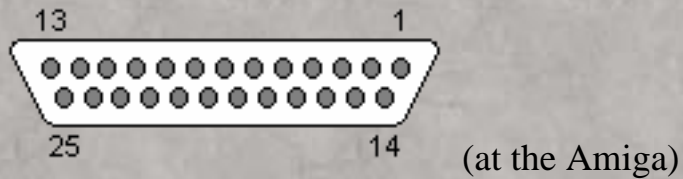
*Contributor: [Joakim Ögren](#)*

*Source:  
Amiga 4000 User's Guide from Commodore*

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



# Parallel (Amiga)



25 PIN D-SUB FEMALE at the Amiga.

Pin	Name	Dir	Description
1	/STROBE	→	Strobe
2	D0	↔	Data Bit 0
3	D1	↔	Data Bit 1
4	D2	↔	Data Bit 2
5	D3	↔	Data Bit 3
6	D4	↔	Data Bit 4
7	D5	↔	Data Bit 5
8	D6	↔	Data Bit 6
9	D7	↔	Data Bit 7
10	/ACK	←	Acknowledge
11	BUSY	↔	Busy
12	POUT	↔	Paper Out
13	SEL	↔	Select (Shared with RS232 RING-indicator)
14	+5V PULLUP	→	+5 Volts DC (10 mA max)
15	n/c	-	Not connected.
16	/RESET	→	Reset
17	GND	—	Signal Ground
18	GND	—	Signal Ground
19	GND	—	Signal Ground
20	GND	—	Signal Ground

21	GND		Signal Ground
22	GND		Signal Ground
23	GND		Signal Ground
24	GND		Signal Ground
25	GND		Signal Ground

*Note: Direction is Computer relative Peripheral.*

*Contributor:* [Joakim Ögren](#)

*Source:*  
*Amiga 4000 User's Guide from Commodore*

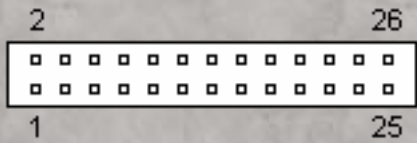
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# Parallel (Olivetti M10)









Available on an old portable computer called Olivetti M10.



(at the Computer)

26 PIN IDC MALE at the Computer.

Pin	Name	Dir	Description
1	/STROBE		Strobe
2	D0		Data Bit 0
3	D1		Data Bit 1
4	D2		Data Bit 2
5	D3		Data Bit 3
6	D4		Data Bit 4
7	D5		Data Bit 5
8	D6		Data Bit 6
9	D7		Data Bit 7
10	/ACK		Acknowledge
11	BUSY		Busy
12	PE		Paper End
13	SELIN		Select In
14	GND		Signal Ground
15	GND		Signal Ground
16	GND		Signal Ground
17	GND		Signal Ground
18	GND		Signal Ground

19	GND		Signal Ground
20	GND		Signal Ground
21	GND		Signal Ground
22	GND		Signal Ground
23	GND		Signal Ground
24	GND		Signal Ground
25	RESETGND		Reset Ground
26	/RESET		Reset

*Note: Direction is Computer relative Device.*

*Contributor: [Joakim Ögren](#), [Filippo Fiani](#)*

*Source:*  
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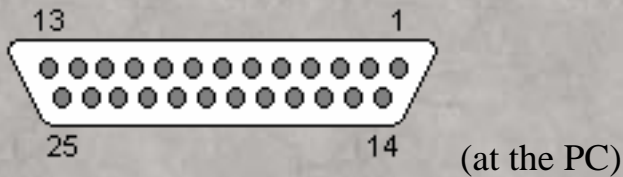
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




# Parallel (PC)



25 PIN D-SUB FEMALE at the PC.

Pin	Name	Dir	Description
1	/STROBE	→	Strobe
2	D0	→	Data Bit 0
3	D1	→	Data Bit 1
4	D2	→	Data Bit 2
5	D3	→	Data Bit 3
6	D4	→	Data Bit 4
7	D5	→	Data Bit 5
8	D6	→	Data Bit 6
9	D7	→	Data Bit 7
10	/ACK	←	Acknowledge
11	BUSY	←	Busy
12	PE	←	Paper End
13	SEL	←	Select
14	/AUTOFD	→	Autofeed
15	/ERROR	←	Error
16	/INIT	→	Initialize
17	/SELIN	→	Select In
18	GND	—	Signal Ground
19	GND	—	Signal Ground
20	GND	—	Signal Ground

21	GND		Signal Ground
22	GND		Signal Ground
23	GND		Signal Ground
24	GND		Signal Ground
25	GND		Signal Ground

*Note: Direction is Computer relative Device.*

*Contributor: [Joakim Ögren](#), [Petr Krc](#)*

*Source:  
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

























# Parallel (SUN)

Available on SUN SPARCengine motherboards

26 PIN HI-DENSITY D-SUB CONNECTOR

Pin	Name	Dir	Description
1	/STROBE		Strobe
2	D0		Data Bit 0
3	D1		Data Bit 1
4	D2		Data Bit 2
5	D3		Data Bit 3
6	D4		Data Bit 4
7	D5		Data Bit 5
8	D6		Data Bit 6
9	D7		Data Bit 7
10	/ACK		Acknowledge
11	BUSY		Busy
12	PE		Paper End
13	SEL		Select
14	/AUTOFD		Autofeed
15	/ERROR		Error
16	/RESET		Reset
17	/SELIN		Select In
18	GND		Signal Ground
19	GND		Signal Ground
20	GND		Signal Ground
21	GND		Signal Ground
22	GND		Signal Ground

23	GND		Signal Ground
24	GND		Signal Ground
25	GND		Signal Ground
26	GND		Signal Ground

*Note: Direction is Computer relative Device.*

*Contributor: [Joakim Ögren](#)*

*Source:*

*[SUN SPARCengine 5 manual](#) at [SUN manuals site](#)*

*SUN SPARCengine Ultra 20 OEM Manual*

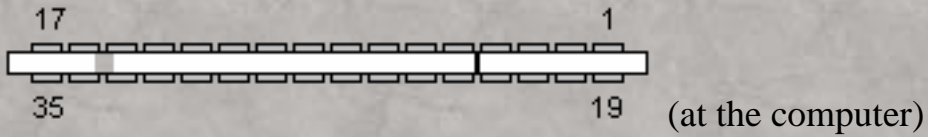
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# Amstrad CPC6128 Printer Port



34 PIN FEMALE EDGE at the computer.

Pin	Name	Description
1	/STROBE	Strobe
2	D0	Data 0
3	D1	Data 1
4	D2	Data 2
5	D3	Data 3
6	D4	Data 4
7	D5	Data 5
8	D6	Data 6
9	GND	Ground
10	n/c	Not connected
11	BUSY	Busy
12	n/c	Not connected
13	n/c	Not connected
14	GND	Ground
15	n/c	Not connected
16	n/c	Not connected
17	n/c	Not connected
16	GND	Ground
17	n/c	Not connected
19	GND	Ground

20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	n/c	Not connected
28	GND	Ground
29	n/c	Not connected
30	n/c	Not connected
31	n/c	Not connected
32	n/c	Not connected
33	GND	Ground
34	n/c	Not connected
35	n/c	Not connected

*Note: Pin 18 does not exist*

*Contributor:* [Joakim Ögren](#), [Agnello Guarracino](#)

*Source:*

*Amstrad CPC6128 User Instructions Manual*

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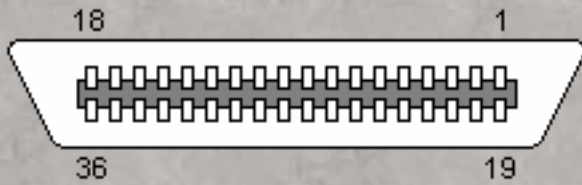
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





# Centronics



(at the Printer)

36 PIN CENTRONICS FEMALE at the Printer.

Pin	Name	Dir	Description
1	/STROBE	←	Strobe
2	D0	↔	Data Bit 0
3	D1	↔	Data Bit 1
4	D2	↔	Data Bit 2
5	D3	↔	Data Bit 3
6	D4	↔	Data Bit 4
7	D5	↔	Data Bit 5
8	D6	↔	Data Bit 6
9	D7	↔	Data Bit 7
10	/ACK	→	Acknowledge
11	BUSY	→	Busy
12	POUT	→	Paper Out
13	SEL	→	Select
14	/AUTOFEED	←	Autofeed
15	n/c	-	Not used
16	0 V	—	Logic Ground
17	CHASSIS GND	—	Shield Ground
18	+5 V PULLUP	→	+5 V DC (50 mA max)
19	GND	—	Signal Ground (Strobe Ground)

20	GND		Signal Ground (Data 0 Ground)
21	GND		Signal Ground (Data 1 Ground)
22	GND		Signal Ground (Data 2 Ground)
23	GND		Signal Ground (Data 3 Ground)
24	GND		Signal Ground (Data 4 Ground)
25	GND		Signal Ground (Data 5 Ground)
26	GND		Signal Ground (Data 6 Ground)
27	GND		Signal Ground (Data 7 Ground)
28	GND		Signal Ground (Acknowledge Ground)
29	GND		Signal Ground (Busy Ground)
30	/GNDRESET		Reset Ground
31	/RESET		Reset
32	/FAULT		Fault (Low when offline)
33	0 V		Signal Ground
34	n/c	-	Not used
35	+5 V		+5 V DC
36	/SLCT IN		Select In (Taking low or high sets printer on line or off line respectively)

*Note: Direction is Printer relative Computer.*

*Contributor: [Joakim Ögren](#), [Peter Korsgaard](#), [Petr Krc](#)*

*Source:  
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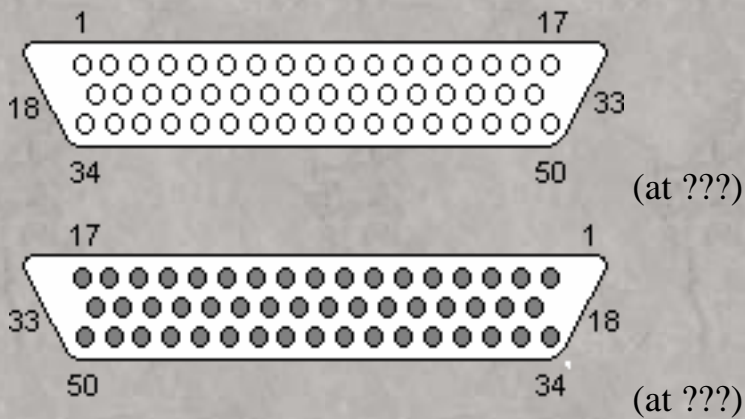
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# Dataproducts D-Sub 50 Parallel



50 PIN D-SUB MALE at ???.

50 PIN D-SUB FEMALE at ???.

Pin	Return	Dir	Description	Active State
22	6	←	Ready	High
21	5	←	On Line	High
23	7	←	Demand	High
38	37	→	Data Strobe	High
19	3	→	Data 1	n/a
20	4	→	Data 2	n/a
1	2	→	Data 3	n/a
41	40	→	Data 4	n/a
34	18	→	Data 5	n/a
43	42	→	Data 6	n/a
36	35	→	Data 7	n/a
28	44	→	Data 8	n/a
29	13	→	Parity	n/a
50	32	←	Ident 0	n/a
49	16	←	Ident 1	n/a

46	47		Interface Verify	Low
12	39		+5 VDC (Test)	High
27	11		Parity Error	High
25	9		Bottom of Form	High
24	8		Top of Form	High
30	14		Paper Instruction	High
31	15		Buffer Clear	High
26	10		Paper Moving	High
48	17		Paper Moving	High
47	33		Not VFU	High

*Note: Direction is Host (Computer) relative Peripheral (Printer).*

*Note: Return is Ground signal for Unbalanced and the Negative Signal for Balanced.*

*Contributor: [Joakim Ögren](#)*

*Source:*

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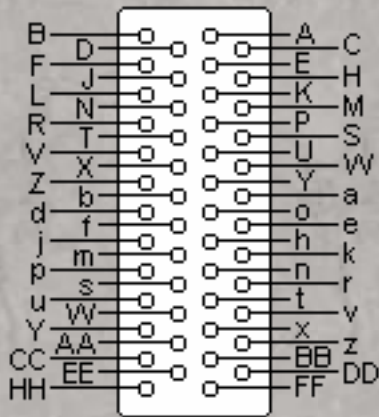
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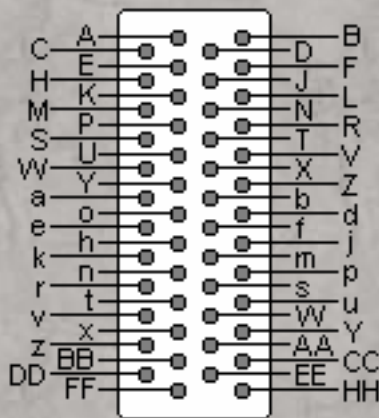




# Dataproducts M/50 Parallel



(at ???)





















(at ???)

50 PIN M/50 MALE at ???.

50 PIN M/50 FEMALE at ???.

Pin	Return	Dir	Description	Active State
CC	EE	←	Ready	High
Y	AA	←	On Line	High
E	C	←	Demand	High
j	m	→	Data Strobe	High
B	D	→	Data 1	n/a
F	J	→	Data 2	n/a
L	N	→	Data 3	n/a

R	T		Data 4	n/a
V	X		Data 5	n/a
Z	b		Data 6	n/a
n	k		Data 7	n/a
u	w		Data 8	n/a
z	BB		Parity	n/a
d	f		Ident 0	n/a
a	c		Ident 1	n/a
v	x		Interface Verify	Low
HH	K		+5 VDC (Test)	High
r	t		Parity Error	High
M	P		Bottom of Form	High
S	U		Top of Form	High
p	s		Paper Instruction	High
A	H		Buffer Clear	High
W	Y		Paper Moving	High
FF	DD		Paper Moving	High
e	h		Not VFU	High

*Note: Direction is Host (Computer) relative Peripheral (Printer).*

*Note: Return is Ground signal for Unbalanced and the Negative Signal for Balanced.*

Contributor: [Joakim Ögren](#)

Source:

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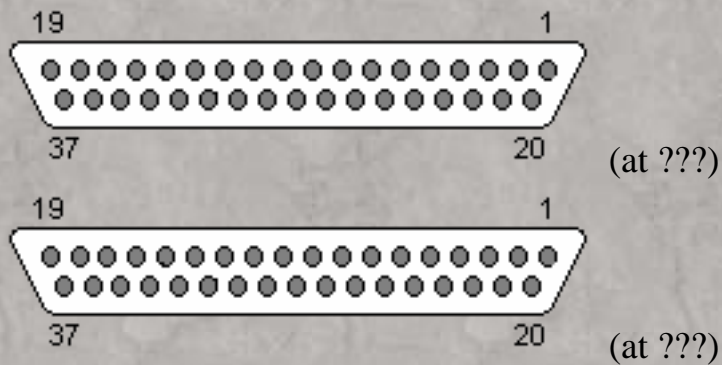
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







# DEC Printer



37 PIN D-SUB FEMALE at ???.

37 PIN D-SUB MALE at ???.

Pin	Name	Dir	Description
1	DAT<3>	→	Data Bit 3
2			Not available
3			Not available
4			Not available
5	DAT<6>	→	Data Bit 6
6	DAT<7>	→	Data Bit 7
7			Not available
8	Strobe	→	Data Bit 1
9			Not available
10			Not available
11			Not available
12	On Line	←	Strobe
13			Not available
14	Connection	→	Connection
15			Not available
16			Not available

17	DAVFU		DAVFU
18	Demand		Data Bit 0
19			Not available
20	DAT<1>		Data Bit 2
21			Not available
22	DAT<2>		Data Bit 2
23	DAT<4>		Data Bit 4
24	DAT<5>		Data Bit 5
25			Not available
26	DAT<0>		Data Bit 2
27	Ground		Ground
28	Ground DAT<0>		Ground Data Bit 0
29	Ground DAT<1>		Ground Data Bit 1
30	Ground DAT<2>		Ground Data Bit 2
31	Ground DAT<3>		Ground Data Bit 3
32	Ground DAT<4>		Ground Data Bit 4
33	Ground DAT<5>		Ground Data Bit 5
34	Ground DAT<6>		Ground Data Bit 6
35	Ground DAT<7>		Ground Data Bit 7
36			Not available
37			Not available

*Note: Direction is Host (Computer) relative Peripheral (Printer).*

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*Source:*  
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*Document last modified:* 2001-06-07





# IndyCam Digital Video Port

## 60 PIN UNKNOWN CONNECTOR

```

      15                      1
      oooooooooooooooooo
30  oooooooooooooooooo  16
45  oooooooooooooooooo  31
      oooooooooooooooooo
      60                      46
  
```

Pin	Name
1	(Reserved)
2	(Reserved)
3	(Reserved)
4	(Reserved)
5	(Reserved)
6	(Reserved)
7	SERIAL CONTROL DATA
8	(Reserved)
9	SERIAL CONTROL CLOCK
10	(Reserved)
11	(Reserved)
12	CLOCK GROUND
13	CLOCK
14	(Reserved)
15	(Reserved)
16	(Reserved)
17	(Reserved)
18	(Reserved)

19	(Reserved)
20	(Reserved)
21	(Reserved)
22	+12
23	+5
24	-12
25	(Reserved)
26	(Reserved)
27	DATA(7) GROUND
28	DATA(7)
29	DATA(6) GROUND
30	DATA(6)
31	DATA(3)
32	DATA(3) GROUND
33	DATA(4)
34	DATA(4) GROUND
35	DATA(5)
36	DATA(5) GROUND
37	(Reserved)
38	(Reserved)
39	(Reserved)
40	(Reserved)
41	(Reserved)
42	(Reserved)
43	(Reserved)
44	(Reserved)
45	(Reserved)
46	DATA(0)
47	DATA(0) GROUND
48	DATA(1)
49	DATA(1) GROUND
50	DATA(2)

51	DATA(2) GROUND
52	(Reserved)
53	(Reserved)
54	(Reserved)
55	(Reserved)
56	(Reserved)
57	(Reserved)
58	(Reserved)
59	(Reserved)
60	(Reserved)

*Contributor:* [Joakim Ögren](#)

*Source:*  
*SGI Indy Workstation Owner's Guide*

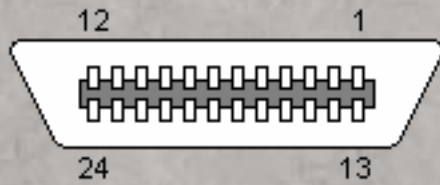
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# IEEE488



(at the Devices)

24 PIN CENTRONICS FEMALE at the Devices.

Also known as GPIB (General Purpose Interface Bus)

Pin	Name	Description	Source
1	DIO1	Data Bit 1	Talker
2	DIO2	Data Bit 2	Talker
3	DIO3	Data Bit 3	Talker
4	DIO4	Data Bit 4	Talker
5	EOI	End Or Indentity	Talker/Controller
6	DAV	Data Valid	Controller
7	NRFD	Not Ready For Data	Listener
8	NDAC	No Data Accepted	Listener
9	IFC	Interface Clear	Controller
10	SRQ	Service Request	Talker
11	ATN	Attention	Controller
12		Shield	-
13	DIO5	Data Bit 5	Talker
14	DIO6	Data Bit 6	Talker
15	DIO7	Data Bit 7	Talker
16	DIO8	Data Bit 8	Talker
17	REN	Remote Enabled	Controller
18		Ground DAV	-



19	Ground NRFD	-
20	Ground NDAC	-
21	Ground IFC	-
22	Ground SRQ	-
23	Ground ATN	-
24	Logical Ground	-

## Data Lines:

Name	Description
DIO1 to DIO8	Data Input Output

## Handshake Lines:

Name	Description
DAV	Data Valid
NRFD	Not Ready For Data
NDAC	Not Data Accepted

## Interface Management Lines:

Name	Description
ATN	Attention
IFC	Interface Clear
REN	Remote Enable
SRQ	Service Request
EOI	End or Identify

Contributor: [Joakim Ögren](#)

Source:

[Commodore PET FAQ](#)

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# 3.5" Power

Used for floppies.

Name according to the ATX standard: Floppy Drive Connector.

**NOT  
DRAWN  
YET...**



(at the powersupply cable)





**NOT  
DRAWN  
YET...**



(at the peripheral)

UNKNOWN CONNECTOR at the powersupply cable.

UNKNOWN CONNECTOR at the peripheral.

Pin	Name		Color	Description
1	+5V		Red	+5 VDC
2	GND		Black	+5 V Ground
3	GND		Black	+12 V Ground (Same as +5 V Ground)
4	+12V		Yellow	+12 VDC

Recommended wiresize according to the ATX standard: 20 AWG

At cables: AMP 171822-4

Contributor: [Joakim Ögren](#)

Source:

?

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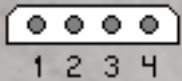
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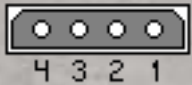
## 5.25" Power

Used for harddisks & 5.25" peripherals.

Name according to the ATX standard: Peripheral Connector.







(at the powersupply cable)



(at the peripheral)

UNKNOWN CONNECTOR at the powersupply cable.

UNKNOWN CONNECTOR at the peripheral.

Pin	Name		Color	Description
1	+12V		Yellow	+12 VDC
2	GND		Black	+12 V Ground (Same as +5 V Ground)
3	GND		Black	+5 V Ground
4	+5V		Red	+5 VDC

Recommended wiresize according to the ATX standard: 18 AWG

At cables: AMP 1-480424-0 or Molex 8981-04P

At peripherals: AMP 61314-1

Contributor: [Joakim Ögren](#), [Eric Sprigg](#), [Sven Gunnar Bilen](#), [Scott Lindenthaler](#)

Source:  
?

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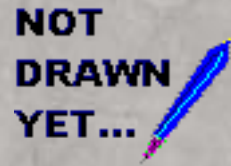
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# AT Backup Battery



(at the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	BATT+	Battery+
2	key	Key
3	GND	Ground
4	GND	Ground

Contributor: [Joakim Ögren](#)

Source:  
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# AT LED/Keylock

**NOT  
DRAWN  
YET...** 

(at the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	LED	LED Power
2	GND	Ground
3	GND	Ground
4	KS	Key Switch
5	GND	Ground

Contributor: [Joakim Ögren](#)

Source:  
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# Motherboard CPU Cooling fan

1 2 3

. . .

3 PIN IDC MALE at the motherboard

Pin	Name
1	GND
2	+12V
3	GND

Contributor: [Rob Gill](#)

Source:  
*ASUS Motherboard Manual*

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# Motherboard IrDA

For motherboards with a IrDA compliant Infrared Module connector.

1 2 3 4 5  
• • • • •

5 PIN IDC MALE at the motherboard.

Pin	Name	Description
1	+5v	Power
2	n/c	Not connected
3	IRRX	IR Module data received
4	GND	System GND
5	IRTX	IR Module data transmit

Contributor: [Rob Gill](#)

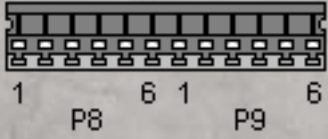
Source:  
*ASUS motherboard manual*

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# Motherboard Power



(at the Computer)

**NOT  
DRAWN  
YET...**



(at the Powersupply cables)

2x MOLEX 15-48-0106 CONNECTOR at the Computer.



2x MOLEX 90331-0001 CONNECTOR at the Powersupply cables.

## P8

Pin	Name		Color	Description
1	PG		Orange	Power Good, +5 VDC when all voltages has stabilized.
2	+5V		Red	+5 VDC (or n/c)
3	+12V		Yellow	+12 VDC
4	-12V		Blue	-12 VDC
5	GND		Black	Ground
6	GND		Black	Ground

## P9

Pin	Name		Color	Description
1	GND		Black	Ground
2	GND		Black	Ground
3	-5V		White or Yellow	-5 VDC
4	+5V		Red	+5 VDC

5	+5V		Red	+5 VDC
6	+5V		Red	+5 VDC

*Note: Pins part number is 08-50-0276, Product specification is PS-90331.*

*Contributor: [Joakim Ögren](#), [Bill Shepherd](#)*

*Source:  
?*

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# PC Speaker

**NOT  
DRAWN  
YET...**



(at the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	-SP	-Speaker
2	key	Key
3	GND	Ground
4	+SP5V	+Speaker +5 VDC

Contributor: [Joakim Ögren](#)

Source:  
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# Turbo LED

**NOT  
DRAWN  
YET...**



(at the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	+5V	+5 VDC
2	/HS	HighSpeed
3	+5V	+5 VDC

Contributor: [Joakim Ögren](#)

Source:  
?

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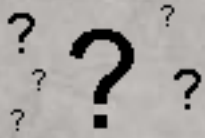
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# Amiga 2000 Power Supply



(at the motherboard)

UNKNOWN CONNECTOR at the motherboard.

Pin	Name
1	+5V
2	+5V
3	+5V
4	+5V
5	GND1
6	GND2
7	GND3
8	GND4
9	+12V
10	KEY
11	-12V
12	+5V USER
13	-5V
14	TICK

You will be able to tell the orientation with the help of pin 10, it is missing.

*Note: TICK is NOT found on PC power supplies*

Contributor: [Joakim Ögren](#)

*Source:*

*Amiga Power Supply pinouts at [National Amiga](#)*

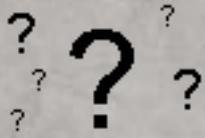
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# Amiga 3000 Power Supply



(at the motherboard)

UNKNOWN CONNECTOR at the motherboard.

Pin	Name
1	+VID
2	+5V
3	+5V
4	+5V
6	GND
7	GND
8	GND
9	GND
10	GND
11	-5V
12	+5V USER
13	TICK
14	-12V/-12V USER
15	+12V/+12V USER

Contributor: [Joakim Ögren](#)

Source:

Amiga Power Supply pinouts at [National Amiga](#)

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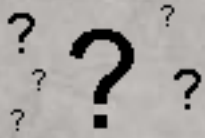
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# Amiga 3000T Power Supply



(at the motherboard)

UNKNOWN CONNECTOR at the motherboard.

Pin	Name
1	TICK
2	-12V
3	-5V
4	GND
5	GND
6	GND
7	GND
8	GND
9	+5V
10	+5V
11	+5V
12	+5V
13	FAIL
14	+12V
15	+12V
16	+5V USER
17	GND
18	GND
19	GND
20	GND

21	+5V
22	+5V
23	+5V
24	+5V

*Contributor:* [Joakim Ögren](#)

*Source:*  
*Amiga Power Supply pinouts at* [National Amiga](#)

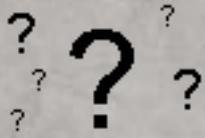
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# Amiga 500/600/1200 Power Supply



(at the motherboard)

UNKNOWN CONNECTOR at the motherboard.

Pin	Name
1	+5V
2	Shield Ground
3	+12V
4	Signal Ground
5	-12V

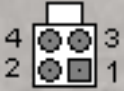
Contributor: [Joakim Ögren](#)

Source:  
Amiga Power Supply pinouts at [National Amiga](#)

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# ATX +12V Power Supply







(at the motherboard)



(at the cable)

4 PIN MOLEX 39-29-9042 at the motherboard

4 PIN MOLEX 39-01-2040 at the cable

Pin	Name		Color	Description
1	COM		Black	Ground
2	COM		Black	Ground
3	+12VDC		Yellow	+12 VDC
4	+12VDC		Orange	+3.3 VDC

Recommended wiresize 20 AWG

Contributor: [Joakim Ögren](#)

Source:

[ATX Spec v2.03](#) at [Platform Development Support](#)

[ATX/ATX12V Power Supply Design Guide](#) at [Platform Development Support](#)

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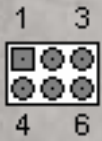
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# ATX Aux Power Supply

To be used for motherboards requiring 250W or 300W



(at ???)

6 PIN MOLEX 90331-0010 at ???

Pin	Name		Color	Description
1	COM		Black	Ground
2	COM		Black	Ground
3	COM		Black	Ground
4	3.3V		Orange	+3.3 VDC
5	3.3V		Orange	+3.3 VDC
6	5V		Red	+5 VDC

Recommended wiresize 16 AWG

Contributor: [Joakim Ögren](#)

Source:

[ATX Spec v2.03](#) at [Platform Development Support](#)

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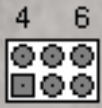
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# ATX Optional Power



(at the motherboard)



(at the cable)

6 PIN MOLEX 39-30-1060 at the motherboard

6 PIN MOLEX 39-01-2060 at the cable

Pin	Name			Color	Description
1	FanM			White	Fan Monitor
2	FanC			White/Blue	Fan Control
3	3.3V Sense			White/Brown	3.3V Sense Line
4	1394R			White/Black	IEEE-1394 Ground
5	1394V			White/Red	IEEE-1394 Voltage?
6	Reserved			n/a	

Contributor: [Joakim Ögren](#)

Source:

[ATX Spec v2.03](#) at [Platform Development Support](#)

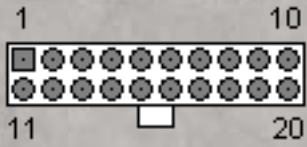
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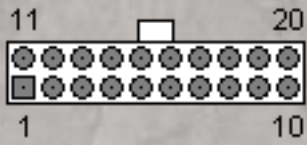
Document last modified: 2001-06-08



# ATX Power Supply



(at the motherboard)







(at the cable)

20 PIN MOLEX 39-29-9202 at the motherboard

20 PIN MOLEX 39-01-2200 at the cable

Pin	Name		Color	Description
1	3.3V		Orange	+3.3 VDC
2	3.3V		Orange	+3.3 VDC
3	COM		Black	Ground
4	5V		Red	+5 VDC
5	COM		Black	Ground
6	5V		Red	+5 VDC
7	COM		Black	Ground
8	PWR_OK		Gray	Power Ok (+5V & +3.3V is ok)
9	5VSB		Purple	+5 VDC Standby Voltage (max 10mA)
10	12V		Yellow	+12 VDC
11	3.3V		Orange	+3.3 VDC
12	-12V		Blue	-12 VDC
13	COM		Black	Ground
14	/PS_ON		Green	Power Supply On (active low)
15	COM		Black	Ground
16	COM		Black	Ground

17	COM		Black	Ground
18	-5V		White	-5 VDC
19	5V		Red	+5 VDC
20	5V		Red	+5 VDC

18 AWG is recommended for all wires except pin 11, which should be 22 AWG  
For 300W configurations 16 AWG is recommended.

Contributor: [Joakim Ögren](#)

Source:

[ATX Spec v2.03](#) at [Platform Development Support](#)

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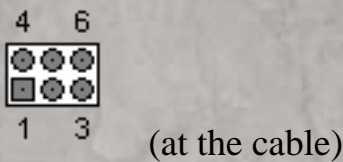
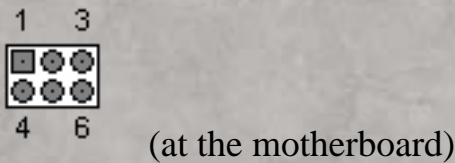
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# SFX Optional Power



6 PIN MOLEX 39-30-1060 at the motherboard  
6 PIN MOLEX 39-01-2060 at the cable

Pin	Name		Color	Description
1	Reserved		n/a	
2	Fan On/Off		White/Blue	Fan Control
3	Reserved		n/a	
4	Reserved		n/a	
5	Reserved		n/a	
6	Reserved		n/a	

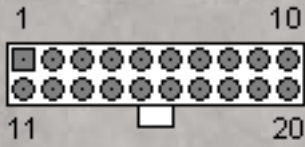
Contributor: [Joakim Ögren](#)

Source:  
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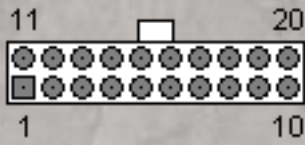
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# SFX Power Supply



(at the motherboard)



(at the cable)

20 PIN MOLEX 39-29-9202 at the motherboard

20 PIN MOLEX 39-01-2200 at the cable

Same as ATX except that -5VDC is removed from pin 18

Pin	Name		Color	Description
1	3.3V		Orange	+3.3 VDC
2	3.3V		Orange	+3.3 VDC
3	COM		Black	Ground
4	5V		Red	+5 VDC
5	COM		Black	Ground
6	5V		Red	+5 VDC
7	COM		Black	Ground
8	PWR_OK		Gray	Power Ok (+5V & +3.3V is ok)
9	5VSB		Purple	+5 VDC Standby Voltage (max 10mA)
10	12V		Yellow	+12 VDC
11	3.3V		Orange	+3.3 VDC
12	-12V		Blue	-12 VDC
13	COM		Black	Ground
14	/PS_ON		Green	Power Supply On (active low)
15	COM		Black	Ground

16	COM		Black	Ground
17	COM		Black	Ground
18	res			Reserved
19	5V		Red	+5 VDC
20	5V		Red	+5 VDC

18 AWG is recommended for all wires except pin 11, which should be 22 AWG  
For 300W configurations 16 AWG is recommended.

Contributor: [Joakim Ögren](#)

Source:  
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# WTX 12V CPU (P3)

8 PIN MOLEX 39-29-9082 CONNECTOR at the Motherboard

8 PIN MOLEX 39-01-2080 CONNECTOR at the cable

Pin	Name		Color	Description	AWG
1	12Vdig		White	+12 VDC (Digital)	18
2	12Vdig		White	+12 VDC (Digital)	18
3	12Vdig		White	+12 VDC (Digital)	18
4	12Vdigsen			Sense +12 VDC (Digital) (Optional?)	
5	com		Black	Ground	18
6	com		Black	Ground	18
7	com		Black	Ground	18
8	12Vdigsenrtn			Ground Sense +12 VDC (Digital) (Optional?)	

Contributor: [Joakim Ögren](#)

Source:

WTX Power Supply Design Guidelines at [WTX Website](#)

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# WTX 12V CPU (P4/P5)

12 PIN MOLEX 39-29-9062 CONNECTOR at the Motherboard

12 PIN MOLEX 39-30-1060 CONNECTOR at the cable

Pin	Name		Color	Description	AWG
1	12Vcpu#		White	+12 VDC (CPU)	18
2	12Vcpu#		White	+12 VDC (CPU)	18
3	12Vcpu#		White	+12 VDC (CPU)	18
4	com		Black	Ground	18
5	com		Black	Ground	18
6	com		Black	Ground	18

Contributor: [Joakim Ögren](#)

Source:

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
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# WTX Additional (P2)

22 PIN MOLEX 39-29-9222 CONNECTOR at the Motherboard

22 PIN MOLEX 39-01-2220 CONNECTOR at the cable

Pin	Name		Color	Description	AWG
1	5Vsense		Red	Sense +5 VDC	22
2	3.3Vsense		Orange	Sense +3.3 VDC	22
3	res			reserved	
4	com		Black	Ground	18
5	com		Black	Ground	18
6	12Vio		Yellow	+12 VDC (I/O)	18
7	-12V		Blue	-12 VDC	18
8	I2C clk			I2C Clock (optional?)	?
9	FanC		Purple	Fan Control	22
10	PS-OK		Grey	PoweSupply Ok	22
11	res			reserved	
12	5Vsensertn		Black	Ground Sense +5 VDC	22
13	3.3Vsensertn		Black	Ground Sense +3.3 VDC	22
14	res			reserved	
15	com		Black	Ground	18
16	12Vio		Yellow	+12 VDC (I/O)	18
17	12Vio		Yellow	+12 VDC (I/O)	18
18	sleep		White	Sleep	18
19	I2C data			I2C Data (Optional?)	?
20	FanM		Brown	Fan Monitor	22
21	PS-on		Green	PowerSupply On	22
22	res			reserved	

*Contributor:* [Joakim Ögren](#)

*Source:*

*WTX Power Supply Design Guidelines at* [WTX Website](#)

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# WTX Main (P1)

24 PIN MOLEX 39-29-9242 CONNECTOR at the Motherboard

24 PIN MOLEX 39-01-2240 CONNECTOR at the Cable

Pin	Name		Color	Description	AWG
1	3.3V		Orange	+3.3 VDC	18
2	3.3V		Orange	+3.3 VDC	18
3	3.3V		Orange	+3.3 VDC	18
4	3.3V		Orange	+3.3 VDC	18
5	3.3V		Orange	+3.3 VDC	18
6	com		Black	Ground	18
7	com		Black	Ground	18
8	com		Black	Ground	18
9	com		Black	Ground	18
10	com		Black	Ground	18
11	5V		Red	+5 VDC	18
12	5V		Red	+5 VDC	18
13	3.3V		Orange	+3.3 VDC	18
14	3.3V		Orange	+3.3 VDC	18
15	3.3V		Orange	+3.3 VDC	18
16	3.3V		Orange	+3.3 VDC	18
17	3.3Vaux		Brown	+3.3 VDC Auxiliary	20
18	com		Black	Ground	18
19	com		Black	Ground	18
20	com		Black	Ground	18
21	com		Black	Ground	18
22	5Vsb		Purple	+5 VDC Standby	20
23	5V		Red	+5 VDC	18



24	5V		Red	+5 VDC	18
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Contributor: [Joakim Ögren](#)

Source:  
WTX Power Supply Design Guidelines at [WTX Website](#)

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# Apple Macintosh Classic Internal Power

## 14 PIN UNKNOWN CONNECTOR

Available at location J12 on the Apple Macintosh Classic logic board?

Pin	Name
1	+12 volts
2	+ 5 volts
3	+ 5 volts
4	/VSYNC
5	/HSYNC
6	VIDOUT
7	Sound
8	-12 volts
9	PWM (Brightness control signal)
10	Ground
11	Ground
12	Ground
13	Ground
14	Ground

Contributor: [Joakim Ögren](#)

Source:

[Apple Tech Info Library 6532: Macintosh Classic, Internal Power Connector Pinouts](#) at [Apple TIL homepage](#)

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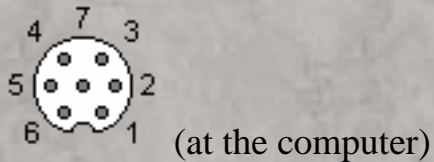
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# C64 Power Supply

Available at the Commodore 64.



7 PIN DIN 'O' FEMALE at the computer.

Pin	Name
1	Shield Ground
2	Shield Ground
3	Shield Ground
4	Not connected
5	+5v In
6	9Vac in
7	9Vac in

Contributor: [Rob Gill](#)

Source:  
*Commodore 64 Programmers Reference Guide*

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# SUN Power

18 PIN MOLEX 39-29-9182 CONNECTOR at the motherboard

Available on the SUN SPARCengine 5 motherboard

Pin	Description
1	+12
2	-12
3	+5
4	+5
5	+5
6	+5
7	+5
8	+5
9	Power off
10	Ground
11	Ground
12	Ground
13	Ground
14	Ground
15	Ground
16	AC Outlet
17	Fan
18	Power on

Contributor: [Joakim Ögren](#)

Source:  
[SUN SPARCengine 5 manual](#) at [SUN manuals site](#)



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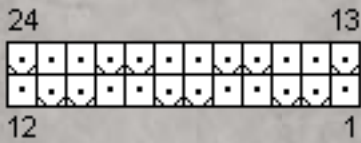
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# Sun Aux Power

Available on SUN SPARCengine motherboards



(at the motherboard)

24 PIN MOLEX 39-29-9242 at the Motherboard

Pin	Name
1	+3.3V
2	GND
3	+3.3V
4	GND
5	+3.3V
6	GND
7	+3.3V
8	GND
9	PWR_SENSE_3.3V
10	GND
11	PWR_SENSE_GND
12	+12V
13	+5V
14	GND
15	+5V
16	GND
17	+5V
18	GND

19	+5V
20	GND
21	PWR_SENSE_5V
22	GND
23	PWR_SENSE_GND
24	-12V

Contributor: [Joakim Ögren](#)

Source:  
*SUN SPARCEngine Ultra AXmp Manual*

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# Apple 300/1200 Modem

## 9 PIN D-SUB CONNECTOR

Pin	Name	Description
1	n/c	Not connected
2	DSR	Data Set Ready
3	GND	Ground
4	n/c	Not connected
5	RxD	Receive Data
6	DTR	Data Terminal Ready
7	DCD	Output from modem
8	GND	Ground
9	TxD	Transmit Data

Contributor: [Joakim Ögren](#)

Source:

[Technote HW19: Pinouts](#) at [Apple Technical Notes](#)

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# Apple Duo Dock Modem Adapter Card

## 10 PIN UNKNOWN CONNECTOR

Pin	Name	Description
1	LINET/R	Line/talk receive
2	DAA GND	Modem DAA ground
3	DAA GND	Modem DAA ground
4	DAA GND	Modem DAA ground
5	/RA DVR	Modem relay A driver
6	DAA ID IN	ID input
7	/RING3 DET	Ring detect signal
8	/RBDVR	Modem relay B driver
9	DAA CNTL	Modem DAA control
10	+5 V MODEM	+5 V power

When the PowerBook Duo computer is housed in the Duo Dock, you cannot access the integral modem via the RJ-11 connector on the PowerBook Duo's rear panel. A modem adapter card provides the connection. It plugs into the side of the Duo Dock's main logic board, using a 10-pin header connector. The card supplies the RJ-11 hook up, which is accessed on the rear panel of the Duo Dock. The adapter card interfaces with the modem card in the PowerBook Duo computer via its 10-pin connector, printed circuit traces, and the 152-pin expansion connector.

Contributor: [Joakim Ögren](#)

Source:  
[Apple Tech Info Library 12929: Duo Dock/Duo Dock II, External Pinouts](#) at [Apple TIL homepage](#)

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# Apple ImageWriter Serial

## 25 PIN D-SUB CONNECTOR

Pin	Name	Dir	Description
1	GND		Ground
2	SD		Send Data
3	RD		Receive Data
4	RTS		Request To Send
7	GND		Ground
14	FAULT-		False when deselected
20	DTR		Data Terminal Ready

*Note: Direction is Printer relative Computer.*

Contributor: [Joakim Ögren](#)

Source:

[Technote HW19: Pinouts](#) at [Apple Technical Notes](#)

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






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# Apple LaserWriter AppleTalk

## 9 PIN D-SUB CONNECTOR

Pin	Name	Dir	Description
1	GND		Ground
2	n/c		Not connected
3	GND		Ground
4	TXD+		Transmit Data +
5	TXD-		Transmit Data -
6	n/c		Not connected
7	RXCLK		TRxC of Zilog 8530
8	RXD+		Receive Data +
9	RXD-		Receive Data -

*Note: Direction is Printer relative Computer.*

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# Apple LaserWriter Serial

## 25 PIN D-SUB CONNECTOR

Pin	Name	Dir	Description
1	GND	—	Ground
2	TXD-	→	Transmit Data
3	RXD-	←	Receive Data
4	RTS	→	Request To Send
5	CTS	←	Clear To Send
6	DSR	←	Data Set Ready
7	GND	—	Ground
8	DCD	→	Data Carrier Detect
20	DTR-	→	Data Terminal Ready
22	RING	←	?

*Note: Direction is Printer relative Computer.*

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# Apple Macintosh XL Serial A

## 25 PIN D-SUB CONNECTOR

Pin	Name	Description
1	GND	Ground
2	TxD	Transmit Data line
3	RxD	Receive Data line
4	RTS	Request To Send
5	CTS	Clear To Send
6	DSR	Data Set Ready
7	GND	Ground
8	DCD	Data Carrier Detect
9	n/c	Not connected
10	n/c	Not connected
11	n/c	Not connected
12	n/c	Not connected
13	n/c	Not connected
14	n/c	Not connected
15	TxC	Connected to TRxCA
16	n/c	Not connected
17	RxC	Connected to RTxCA
18	n/c	Not connected
19	n/c	Not connected
20	n/c	Not connected
21	n/c	Not connected
22	n/c	Not connected
23	n/c	Not connected
24	TEXT	Connected to TRxCA

25

n/c

Not connected

Contributor: [Joakim Ögren](#)

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# Apple Macintosh XL Serial B

## 25 PIN D-SUB CONNECTOR

Pin	Name	Description
1	GND	Ground
2	TxD-	Transmit Data line
3	RxD-	Receive Data line
4	n/c	Not connected
5	n/c	Not connected
6	HSK/DSR	TRxCB or CTSB
7	GND	Ground
8	n/c	Not connected
9	n/c	Not connected
10	n/c	Not connected
11	n/c	Not connected
12	n/c	Not connected
13	n/c	Not connected
14	n/c	Not connected
15	n/c	Not connected
16	n/c	Not connected
17	n/c	Not connected
18	n/c	Not connected
19	RxD+	Receive Data line
20	TxD+/DTR	Connected to DTRB
21	n/c	Not connected
22	n/c	Not connected
23	n/c	Not connected
24	n/c	Not connected

25

n/c

Not connected

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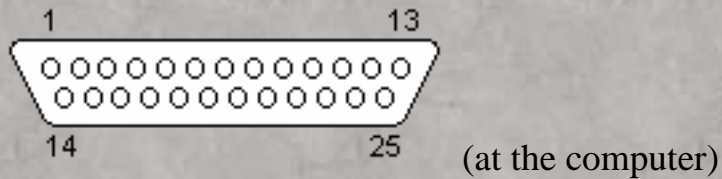
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# AppleLine RS232



25 PIN D-SUB MALE at the computer.

Pin	Name	Dir	Description
1	SNG	—	Shield ground
2	TXD	→	Tx Transmit Data, Out
3	RCD	←	Rx Receive Data, In
4	RTS	→	Request to Send, Out
5	CTS	←	Clear to Send, In
6	DSR	←	Data Set Ready, In
7	GND	—	Ground
8	DCD	←	Data Carrier Detect, In
9	n/c		No connection
10	n/c		No connection
11	n/c		No connection
12	CH	←	Data signal rate selector, In
13	n/c		No connection
14	n/c		No connection
15	n/c		No connection
16	n/c		No connection
17	n/c		No connection
18	n/c		No connection
19	n/c		No connection
20	DTR		Terminal Ready Signal, Out

21	n/c		No connection
22	CE		Ring indicator, In
23	n/c		No connection
24	n/c		No connection
25	n/c		No connection

Contributor: [Joakim Ögren](#)

Source:

[Apple Tech Info Library 1184: AppleLine Pinouts](#) at [Apple TIL homepage](#)

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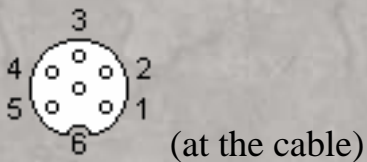
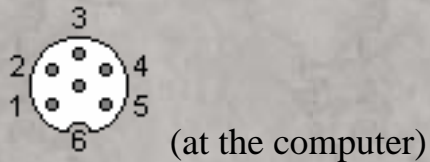
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# C64 Serial I/O

Available on the Commodore C64, C16, C116 and +4 computers.



6 PIN DIN (DIN45322) FEMALE at the Computer.

6 PIN DIN (DIN45322) MALE at the Cable.

Pin	Name	Description
1	/SRQIN	Serial SRQIN
2	GND	Ground
3	ATN	Serial ATN In/Out
4	CLK	Serial CLK In/Out
5	DATA	Serial DATA In/Out
6	/RESET	Reset

Contributor: [Joakim Ögren](#), [Arwin Vosselman](#)

Source:  
SAMS Computerfacts CC8 Commodore 16.

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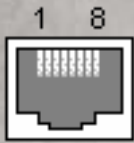
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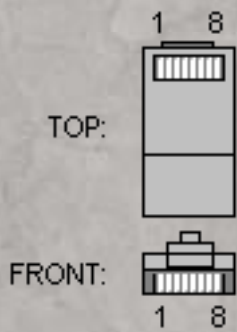


# Cisco Console Port

Used to configure a Cisco router.



(at the Cisco hub)



(at the cables)

RJ45 FEMALE CONNECTOR at the Cisco routers.

RJ45 MALE CONNECTOR at the cables.

Pin	Name	Description	Dir
1	RTS	Request To Send	→
2	DTR	Data Terminal Ready	→
3	TXD	Tranceive Data	→
4	n/c	Not connected	
5	n/c	Not connected	
6	RXD	Receive Data	←
7	DSR	Data Set Ready	←
8	CTS	Clear To Send	←

Contributor: [Joakim Ögren](#), [Damien Miller](#)

Source:

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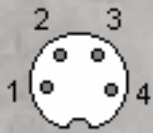
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# CoCo Serial Printer

Available on the Tandy Color Computer, also known as CoCo.



(at the computer)

4 PIN DIN 270° FEMALE at the computer.

Pin	Name	Description
1	NC	
2	/BUSY	Enabled when the printer is busy
3	GND	
4	DATA	RS-232 level data

Contributor: [Rob Gill](#)

Source:  
*Tandy TRP 100 printer manual*

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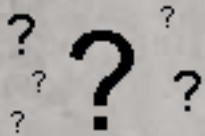
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# Conrad Electronics MM3610D

This connector is available on the Conrad Electronics Multimeter 3610D and is used to connect it to a computer.



(at the multimeter).

5 PIN UNKNOWN CONNECTOR at the multimeter

Conrad	Name	Description	Dir
1	RTS	Request To Send	
2	RXD	Receive Data	
3	TXD	Transmit Data	
4	DTR	Data Terminal Ready	
5	GND	Ground	

*Note: Since the multimeter is a [DCE](#) the pin naming can seem strange.*

*Contributor: [Joakim Ögren](#), [Anselm Belz](#)*

*Source:*  
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





# DEC DLV11-J Serial

Available on the DEC DLV11-J Serial card

**NOT  
DRAWN  
YET...** 

(at the serial card)

10 PIN IDC MALE at the Serial card.

Pin	Name	Dir	Description
1	CLK	?	Clock
2	GND		Ground
3	TXD+		Transmit data +
4	TXD-		Transmit data - (0V for RS-232, Reader enable for 20mA)
5	GND		Ground
6	n/c	-	Not connected (no pin)
7	RXD-		Receive data -
8	RXD+		Receive data +
9	GND		Ground
10	+12V		+12 VDC

*Note: Direction is Serial card relative other Devices.*

Contributor: [Ben Harris](#)

Source:  
DEC DLV11-J Printset, M8043-0-1, sheet 7

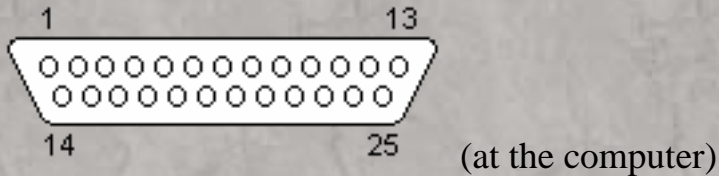
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# DEC Dual RS-232

Found on the DEC Multia and DEC UDB (Universal Desktop Box). It contains two Serial ports on one connector. The 1st Port is located on the normal pins, and the 2nd port is located on some "spare" pins.



25 PIN D-SUB MALE at the computer.

Pin	Port	Name	Dir	Description
1		n/c		Not connected
2	1	TXD	→	Transmit Data
3	1	RXD	←	Receive Data
4	1	RTS	→	Ready To Send
5	1	CTS	←	Clear To Send
6	1	DSR	←	Data Set Ready
7	1+2	GND	-	Ground
8	1	DCD	←	Data Carrier Detect
9		n/c		Not connected
10		n/c		Not connected
11	2	DTR	→	Data Terminal Ready
12	2	DCD	←	Data Carrier Detect
13	2	CTS	←	Clear To Send
14	2	TXD	→	Transmit Data
15		n/c		Not connected
16	2	RXD	←	Receive Data
17		n/c		Not connected

18		n/c		Not connected
19	2	RTS		Ready To Send
20	1	DTR		Data Terminal Ready
21		n/c		Not connected
22	1	RI		Ring Indicator
23	2	DSR		Data Set Ready
24		n/c		Not connected
25	2	RI		Ring Indicator

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Contributor: [Joakim Ögren](#), [Greg A. Woods](#)*

*Source:*

*[Tommy's pinout Collection](#) by [Tommy Johnson](#)*

*[Digital UDB Information](#) by [Eric Smith](#)*

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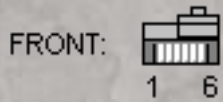
# DEC MMJ

MMJ=Modified Modular Jack

Invented by Digital Equipment Corporation (DEC) (now: Compaq)



(at the devices)



(at the cables)

MMJ FEMALE CONNECTOR at the devices.

MMJ MALE CONNECTOR at the cables.

Pin	Name	Description
1	DTR	Data Terminal Ready
2	TXD+	Transmit Data +
3	TXD-	Transmit Data -
4	RXD+	Receive Data +
5	RXD-	Receive Data -
6	DSR	Data Set Ready

Contributor: [Joakim Ögren](#)

Source:  
?

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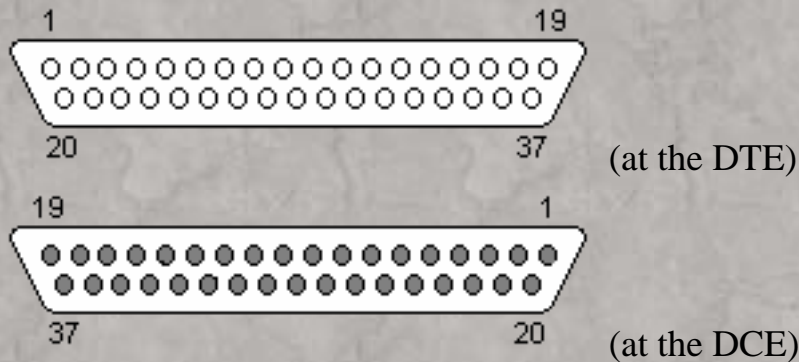




# EIA-449 (RS-449)

Common names: EIA-449, RS-449, ISO 4902

## Primary channel



























CORRECT?

37 PIN D-SUB MALE at the DTE (Computer).

37 PIN D-SUB FEMALE at the DCE (Modem).

Pin	Name	V.24	Dir	Description	Type
1		101	—	Shield	Ground
2	SI	112	→	Signal Rate Indicator	Control
3	n/a		n/a	unused	
4	SD-	103	→	Send Data (A)	Data
5	ST-	114	←	Send Timing (A)	Timing
6	RD-	104	←	Receive Data (A)	Data
7	RS-	105	→	Request To Send (A)	Control
8	RT-	115	←	Receive Timing (A)	Timing
9	CS-	106	←	Clear To Send (A)	Control
10	LL	141	→	Local Loopback	Control
11	DM-	107	←	Data Mode (A)	Control
12	TR-	108.2	→	Terminal Ready (A)	Control

13	RR-	109		Receiver Ready (A)	Control
14	RL	140		Remote Loopback	Control
15	IC	125		Incoming Call	Control
16	SF/SR+	126		Signal Freq./Sig. Rate Select.	Control
17	TT-	113		Terminal Timing (A)	Timing
18	TM-	142		Test Mode (A)	Control
19	SG	102		Signal Ground	Ground
20	RC	102b		Receive Common	Ground
21	n/a		n/a	unused	
22	SD+	103		Send Data (B)	Data
23	ST+	114		Send Timing (B)	Timing
24	RD+	104		Receive Data (B)	Data
25	RS+	105		Request To Send (B)	Control
26	RT+	115		Receive Timing (B)	Timing
27	CS+	106		Clear To Send (B)	Control
28	IS	n/a		Terminal In Service	Control
29	DM+	107		Data Mode (B)	Control
30	TR+	108.2		Terminal Ready (B)	Control
31	RR+	109		Receiver Ready (B)	Control
32	SS	116		Select Standby	Control
33	SQ	110		Signal Quality	Control
34	NS	n/a		New Signal	Control
35	TT+	113		Terminal Timing (B)	Timing
36	SB	117		Standby Indicator	Control
37	SC	102a		Send Common	Ground

*Note: Direction is DTE (Computer) relative DCE (Modem).*

Name	Description	Function
AA	Shield Ground	Also known as protective ground. This is the chassis ground connection between DTE and DCE.

AB	Signal Ground	The reference ground between a DTE and a DCE. Has the value 0 Vdc.
BA	Transmitted Data	Data send by the DTE.
BB	Received Data	Data received by the DTE.
CA	Request To Send	Originated by the DTE to initiate transmission by the DCE.
CB	Clear To Send	Send by the DCE as a reply on the RTS after a delay in ms, which gives the DCEs enough time to energize their circuits and synchronize on basic modulation patterns.
CC	DCE Ready	Known as DSR. Originated by the DCE indicating that it is basically operating (power on, and in functional mode).
CD	DTE Ready	Known as DTR. Originated by the DTE to instruct the DCE to setup a connection. Actually it means that the DTE is up and running and ready to communicate.
CE	Ring Indicator	A signal from the DCE to the DTE that there is an incoming call (telephone is ringing). Only used on switched circuit connections.
CF	Received Line Signal Detector	Known as DCD. A signal send from DCE to its DTE to indicate that it has received a basic carrier signal from a (remote) DCE.
CH/CI	Data Signal Rate Select (DTE/DCE Source>	A control signal that can be used to change the transmission speed.
DA	Transmit Signal Element Timing (DTE Source)	Timing signals used by the DTE for transmission, where the clock is originated by the DTE and the DCE is the slave.
DB	Transmitter Signal Element Timing (DCE Source)	Timing signals used by the DTE for transmission.
DD	Receiver Signal Element Timing (DCE Source)	Timing signals used by the DTE when receiving data.
IS	terminal In Service	Signal that indicates that the DTE is available for operation
NS	New Signal	A control signal from the DTE to the DCE. It instructs the DCE to rapidly get ready to receive a new analog signal. It helps master-station modems rapidly synchronize on a new modem at a tributary station in multipoint circuits
RC	Receive Common	A signal return for receiver circuit reference
LL	Local Loopback / Quality Detector	A control signal from the DTE to the DCE that causes the analog transmission output to be connected to the analog receiver input.



RL	Remote Loopback	Signal from the DTE to the DCE. The local DCE then signals the remote DCE to loopback the analog signal and thus causing a line loopback.
SB	Standby Indicator	Signal from the DCE to indicate if it uses the normal communication or standby channel
SC	Send Common	A return signal for transmitter circuit reference
SF	Select Frequency	A signal from the DTE to tell the DCE which of the two analog carrier frequencies should be used.
SS	Select Standby	A signal from DTE to DCE, to switch between normal communication or standby channel.
TM	Test Mode	A signal from the DCE to the DTE that it is in test-mode and can't send any data.
	Reserved for Testing	

Contributor: [Joakim Ögren](#)

Source:

[RS449 Page](#) at [Connectivity Knowledge Platform \(Made IT\)](#)

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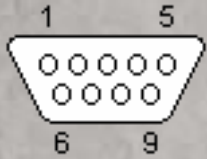




# EIA-449 (RS-449) Secondary

Common names: EIA-449, RS-449, ISO 4902

**Secondary (auxiliary) channel**



(at the Computer)

Pin	Name	RS232	V.24	Dir	Description
1		n/a	101	—	Shield
2	SSR	SRR	122	←	Secondary Receiver Ready
3	SSD	SSD	118	→	Secondary Send Data
4	SRD	SRD	119	←	Secondary Receive Data
5	SG	SG	102	—	Signal Ground
6	RC	RC	102b	—	Receive Common
7	SRS	SRS	120	→	Secondary Request To Send
8	SCS	SCS	121	←	Secondary Clear To Send
9	SC	SC	102a	—	Send Common

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Note: RS232 column is RS232 circuit name.*

*Note: V.24 column is ITU-TSS V.24 circuit name.*

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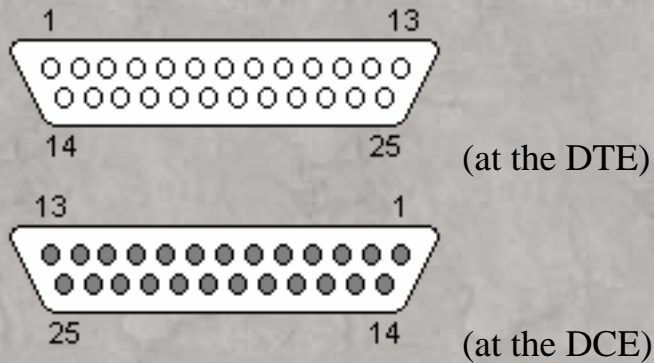
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# EIA530 (RS530)














CORRECT?

25 PIN D-SUB MALE at the DTE (Computer).

25 PIN D-SUB FEMALE at the DCE (Modem).

Pin	Name	Dir	Description	Circuit	Paired with
1		—	Shield		18
2	TxD	→	Transmitted Data	BA	14
3	RxD	→	Received Data	BB	16
4	RTS	→	Request To Send	CA	19
5	CTS	→	Clear To Send	CB	13
6	DSR	→	Data Set Ready	CC	22
7	SGND	—	Signal Ground	Ground	21
8	DCD	→	Data Carrier Detect	CF	10
9		→	Rtrn Receive Sig. Elmnt Timing	DD	17
10		→	Rtrn DCD	CF	8
11		→	Rtrn Transmit Sig. Elmnt Timing	DA	24
12		→	Rtrn Transmit Sig. Elmnt Timing	DB	15
13		→	Rtrn CTS	CB	5
14		→	Rtrn TxD	BA	2

15			Transmit Signal Element Timing	DB	12
16			Rtrn RxD	BB	3
17			Receive Signal Element Timing	DD	9
18	LL		Local Loopback	LL	1
19			Rtrn RTS	CA	4
20	DTR		Data Terminal Ready	CD	23
21	RL		Remote Loopback	RL	7
22			Rtrn DSR	CC	6
23			Rtrn DTR	CD	20
24			Transmit Signal Element timing	DA	11
25			Test Mode	TM	

*Note: Direction is DTE (Computer) relative DCE (Modem).*

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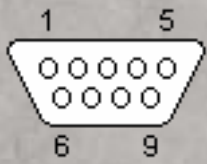
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# HP 4S Scanner



(at the Scanner)

9 PIN D-SUB ??? at the Scanner.

Pin	Name	Dir	Description
1	CD	←	Carrier Detect
2	RXD	←	Receive Data
3	TXD	→	Transmit Data
4	GND	—	System Ground
5	CTS	←	Clear to Send
6	DSR	←	Data Set Ready
7	RI	←	Ring Indicator
8	RTS	→	Request to Send
9	DTR	→	Data Terminal Ready

*Note: Direction is DTE (Computer) relative DCE (Scanner).*

Contributor: [Joakim Ögren](#)

Source:  
[HP 4S Scanner pinout](#) at [The Pin-Out directory](#)

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# HP48/HP95

```

+-----+
| . . . . | (at the Calculator)
\-----/
 1  2  3  4

```

Pin	Name	Dir	Description
1	-	-	-
2	TXD	OUT	Transmit Data
3	RXD	IN	Receive Data
4	GND	-	Ground

Contributor: [Joakim Ögren](#)

Source:  
?

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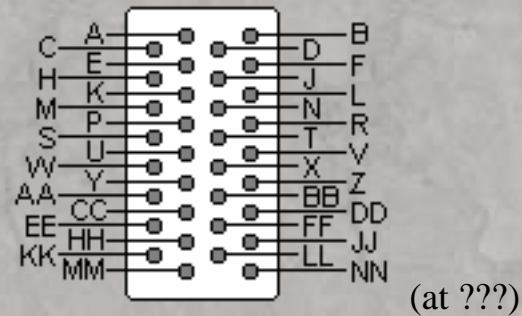
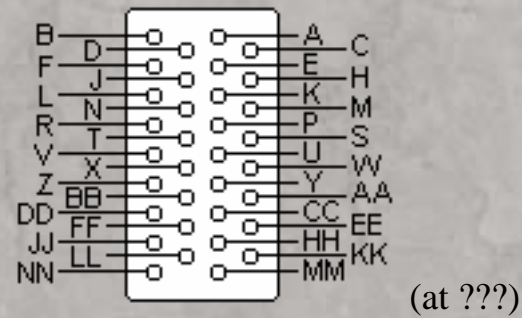
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# ITU-TSS V.35











Common names: ITU-TSS (CCITT) V.35



34 PIN M/34 MALE at ???.

34 PIN M/34 FEMALE at ???.

Pin	Name	Dir	Description
A			Chassis Ground
B			Signal Ground
C	RTS		Request To Send
D	CTS		Clear To Send
E	DSR		Data Set Ready
F	DCD		Data Carrier Detect
H	DTR		Data Terminal Ready
J	LL		Local Loopback
K			Local Test
L			unused

M			unused
N			unused
P	TxD-		Send Data A
R	RxD-		Receive Data A
S	TxD+		Send Data B
T	RxD+		Receive Data B
U			Terminal Timing A
V			Receive Timing A
W			Terminal Timing B
X			Receive Timing B
Y			Send Timing A
Z			unused
AA			Send Timing B
BB			unused
CC			unused
DD			unused
EE			unused
FF			unused
HH			unused
JJ			unused
KK			unused
LL			unused
MM			unused
NN			unused

*Note: Direction is DTE (Computer) relative DCE (Modem).*

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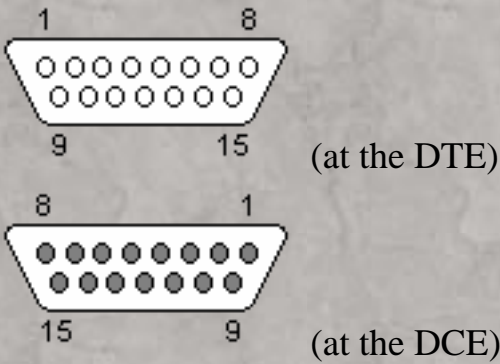
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# ITU-TSS X.21


Common names: ITU-TSS (CCITT) X.21, ISO 4903



CORRECT?

- 15 PIN D-SUB MALE at the DTE (Computer).
- 15 PIN D-SUB FEMALE at the DCE (Modem).

Pin	Name	Dir	Description	Type
1	n/a		Shield	Ground
2	T (A)		Transmit (A)	Data
3	C (A)		Control (A)	Control
4	R (A)		Receive (A)	Data
5	I (A)		Indication (A)	Control
6	S (A)		Signal Timing (A)	Timing
7	B (A)		Byte Timing (A)	Timing
8	G		Ground	Ground
9	T (B)		Transmit (B)	Data
10	C (B)		Control (B)	Control
11	R (B)		Receive (B)	Data
12	I (B)		Indication (B)	Control
13	S (B)		Signal Timing (B)	Timing

14	B (B)		Byte Timing (B)	Timing
15			unused	

*Note: Direction is DTE (Computer) relative DCE (Modem).*

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# Lowrance AirMap 100, GlobalMap 100, GlobalNav 12, GlobalNav 200, GlobalNav 212



(at the GPS)

## 6 PIN LOWRANCE SPECIAL CONNECTOR at the GPS

Pin	Name	Description
1	VCC	Power
2	RX	RS-232 (receive serial)
3	GND	Ground
4	TX	NMEA/Pseudo RS-232 (transmit serial)
5	-	DO NOT USE (recharging purposes)
6	-	DO NOT USE (recharging purposes)

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# Lowrance AirMap, AirMap 300, GlobalMap 12, GlobalMap Sport



6 1 (at the GPS)

6 PIN LOWRANCE SPECIAL CONNECTOR at the GPS

Pin	Name	Description
1	GND	Ground
2	VCC	Power
3	TX	NMEA/Pseudo RS-232 (transmit serial)
4	RX	RS-232 (receive serial)
5	-	DO NOT USE
6	-	DO NOT USE

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# Lowrance GlobalNav 310



(at the GPS)

4 PIN LOWRANCE SPECIAL CONNECTOR at the GPS

Pin	Name	Description
1	VCC	Power
2	RX	RS-232 (receive serial)
3	GND	Ground
4	TX	NMEA/Pseudo RS-232 (transmit serial)

Contributor: [Joakim Ögren](#)

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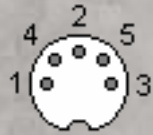
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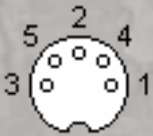


# MIDI In

MIDI=Musical Instrument Digital Interface.



(at the peripheral)



(at the cable)

5 PIN DIN 180° (DIN41524) FEMALE at the peripheral.

5 PIN DIN 180° (DIN41524) MALE at the cable.

Pin	Name	Description
1	n/c	Not connected
2	n/c	Not connected
3	n/c	Not connected
4	CSRC	Current Source
5	CSINK	Current Sink

Contributor: [Joakim Ögren](#)

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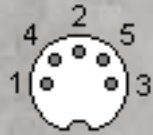
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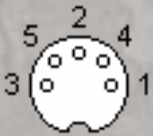


# MIDI Out

MIDI=Musical Instrument Digital Interface.



(at the peripheral)



(at the cable)

5 PIN DIN 180° (DIN41524) FEMALE at the peripheral.

5 PIN DIN 180° (DIN41524) MALE at the cable.

Pin	Name	Description
1	n/c	Not connected
2	GND	Ground
3	n/c	Not connected
4	CSINK	Current Sink
5	CSRC	Current Source

Contributor: [Joakim Ögren](#)

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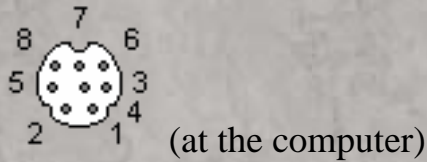
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# Macintosh RS-422

It's possible to connect RS-232 peripheral to the RS-422 port available on Macintosh computers. Use RXD- as RXD, TXD- as TXD, Ground RXD+, Leave TXD+ unconnected, GPi as CD.



8 PIN MINI-DIN FEMALE at the computer.

Pin	Name	Dir	Description
1	HSKo	→	Output Handshake
2	HSKi/CLK	←	Input Handshake or External Clock
3	TXD-	→	Transmit Data (-)
4	GND	—	Ground
5	RXD-	←	Receive Data (-)
6	TXD+	→	Transmit Data (+)
7	GPi	←	General Purpose Input
8	RXD+	←	Receive Data (+)

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Note: GPi is connected to SCC Data Carrier Detect (or to Receive/Transmit Clock if the VIA1 SYNC signal is high). Not connected on the Macintosh Plus, Classic, Classic II, LC, LC II or IIsi.*

Contributor: [Joakim Ögren](#), [Pierre Olivier](#), [Ben Harris](#), [Nathan Schmidt](#)

Source:  
[comp.sys.mac.comm FAQ Part 1](#), Apple Tech Info Library, Article ID: TECHINFO-0001699

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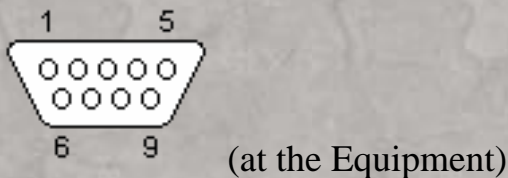
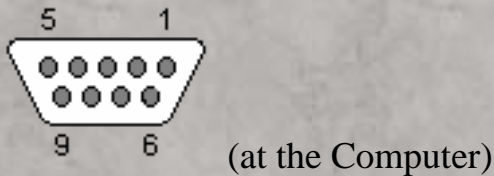


*Document last modified: 2001-06-08*



# Macintosh Serial

Available on Macintosh Mac 512KE and earlier.



9 PIN D-SUB FEMALE at the computer.

9 PIN D-SUB MALE at the mouse cable.

Pin	Name	Dir	Description
1	GND	—	Ground
2	+5V	→	+5 VDC. Don't use this one, it may be converted into output handshake in later equipment.
3	GND	—	Ground
4	Tx+	→	Transmit Data, positive going component
5	Tx-	→	Transmit Data, negative going component
6	+12V	→	+12 VDC
7	DSR/HSK	←	Handshake input. Signal name depends on mode: Used for Flow Control or Clock In.
8	Rx+	←	Receive Data, positive going component
9	Rx-	←	Receive Data, negative going component

*Note: Direction is Computer relative Equipment.*

Contributor: [Ben Harris](#)

*Source:*

*Apple Tech Info Library, Article ID: TECHINFO-0001424*

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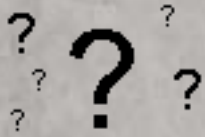
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*Document last modified: 2001-06-07*



# Minuteman UPS

Is the directions right???



(at the UPS)

9 PIN D-SUB ??? at the UPS.

Pin	Description
1	Unused
2	Battery power
3	Unused
4	Common (same as 7)
5	Low battery
6	RS-232 level shutdown
7	Common (same as 4)
8	Ground level shutdown (A500 and above, reserved on <A500)
9	Reserved

Pins 2 and 5 are connected to Common when they are true.

On pin 6, an rs-232 high level (>9V) will shutdown, when running off the battery.

On pin 8, shorting to ground will shutdown.

Contributor: [Joakim Ögren](#)

Source:

[Tommy's pinout Collection](#) by [Tommy Johnson](#)

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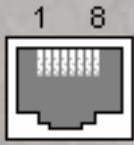
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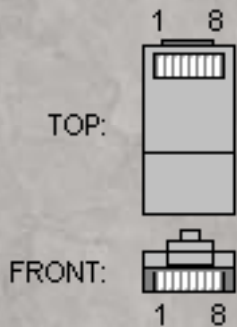
*Document last modified: 2001-06-07*



# RS-232D



(at the devices)



(at the cables)

RJ45 FEMALE CONNECTOR at the devices.

RJ45 MALE CONNECTOR at the cables.

Pin	Name	Dir	Description
1	DSR/RI	←	Data Set Ready / Ring Indicator
2	CD	←	Carrier Detect
3	DTR	→	Data Terminal Ready
4	GND	—	System Ground
5	RXD	←	Receive Data
6	TXD	→	Transmit Data
7	CTS	←	Clear to Send
8	RTS	→	Request to Send

*Note: Direction is DTE (Computer) relative DCE (Modem).*

Contributor: [Joakim Ögren](#)

Source:

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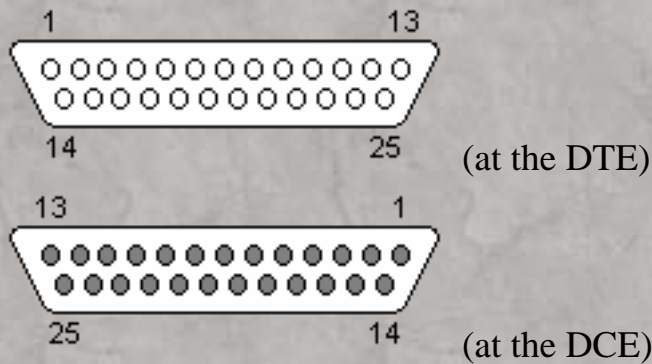
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# RS232

Common names: EIA-232D (RS232-D), ITU-TSS (CCITT) V.24/V.28, ISO 2110














25 PIN D-SUB MALE at the DTE (Computer).

25 PIN D-SUB FEMALE at the DCE (Modem).

Pin	Name	RS232	V.24	Dir	Description
1	GND	n/a	101	—	Shield Ground
2	TXD	BA	103	→	Transmit Data
3	RXD	BB	104	←	Receive Data
4	RTS	CA	105	→	Request to Send
5	CTS	CB	106	←	Clear to Send
6	DSR	CC	107	←	Data Set Ready
7	GND	AB	102	—	System Ground
8	CD	CF	109	←	Carrier Detect
9	-			-	RESERVED
10	-			-	RESERVED
11	STF		126	→	Select Transmit Channel
12	S.CD	SCF	122	←	Secondary Carrier Detect
13	S.CTS	SCB	121	←	Secondary Clear to Send
14	S.TXD	SBA	118	→	Secondary Transmit Data



15	TCK	DB	114		Transmission Signal Element Timing
16	S.RXD	SBB	119		Secondary Receive Data
17	RCK	DD	115		Receiver Signal Element Timing
18	LL	LL	141		Local Loop Control
19	S.RTS	SCA	120		Secondary Request to Send
20	DTR	CD	108.2		Data Terminal Ready
21	RL	RL	140		Remote Loop Control
22	RI	CE	125		Ring Indicator
23	DSR	CH	111		Data Signal Rate Selector
24	XCK	DA	113		Transmit Signal Element Timing
25	TI	TM	142		Test Indicator

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Note: RS232 column is RS232 circuit name.*

*Note: ITU-T column is ITU-TSS V.24 circuit name.*

*Note: Do not connect SHIELD(1) to GND(7).*

*Contributor: [Joakim Ögren](#), [Petr Krc](#)*

*Source:*

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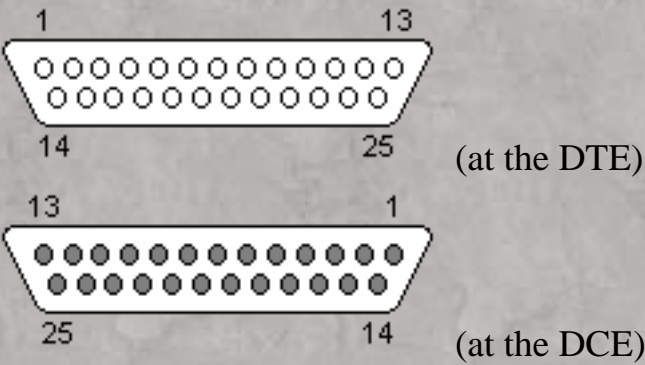
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# RS366



CORRECT?

- 25 PIN D-SUB MALE at the DTE (Computer).
- 25 PIN D-SUB FEMALE at the DCE (Modem).

Pin	Function	Description	Circuit EIA
1		unused	
2	Digit Present	A signal given to the ACE indicating that the digit lines contain a digit	DPR
3	Abandon Call and Retry	An indicator signal from the ACE that it could not make a connection. Could be 'busy'.	ACR
4	Call Request	A signal from the DTE that tells the ACE to go 'off hook'	CRQ
5	Present Next Digit	A signal from the ACE to the DTE to indicate that the ACE is ready to receive the next digit.	PND
6		unused	
7		unused	
8		unused	
9		unused	
10		unused	

11		unused	
12		unused	
13	Distant Station Connected	Indicator from ACE to DTE that the call is succesfully made.	DSC
14-17	Digit Signal Circuits	Four lines containing a parallel BCD dial digit (10 digits, plus control digits)	NB1-NB8
18		unused	
19		unused	
20		unused	
21		unused	
22	Data Line Occupied	An indicator that is used by the ACE to let the DTE know that the line it wants to use is used by another device.	DLO
23		unused	
24		unused	
25		unused	

Contributor: [Joakim Ögren](#)

Source:

[RS366 Page](#) at [Connectivity Knowledge Platform \(Made IT\)](#)

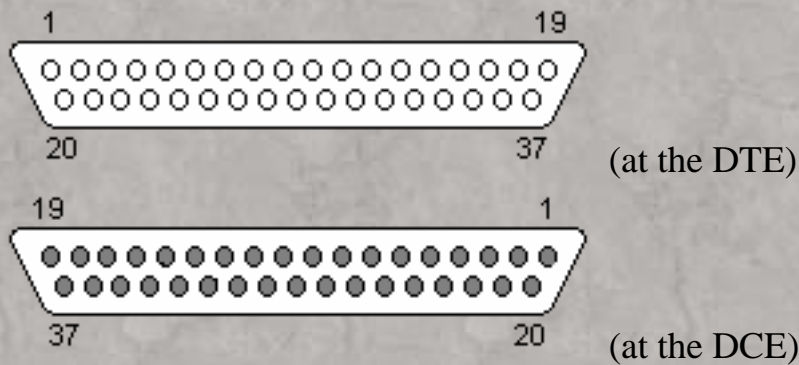
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# RS422 37pin
























37 PIN D-SUB MALE at the DTE (Computer).

37 PIN D-SUB FEMALE at the DCE (Modem).

Pin	Name	Dir	Description
1	GND	—	Shield Ground
2	SRI	←	Signal Rate Indicator
3	n/c	-	Spare
4	SD	→	Send Data
5	ST	→	Send Timing
6	RD	←	Receive Data
7	RTS	→	Request To Send
8	RR	←	Receiver Ready
9	CTS	←	Clear To Send
10	LL	→	Local Loopback
11	DM	←	Data Modem
12	TR	→	Terminal Ready
13	RR	←	Receiver Ready
14	RL	→	Remote Loopback
15	IC	←	Incoming Call
16	SF/SR	→	Select Frequency/Select Rate



17	TT		Terminal Timing
18	TM		Test Mode
19	GND		Ground
20	RC		Receive Twister-Pair Common
21	GND		Spare Twister-Pair Return
22	/SD		Send Data TPR
23	GND		Send Timing TPR
24	GND		Receive Timing TPR
25	/RS		Request To Send TPR
26	/RT		Receive Timing TPR
27	/CS		Clear To Send TPR
28	IS		Terminal In Service
29	/DM		Data Mode TPR
30	/TR		Terminal Ready TPR
31	/RR		Receiver TPR
32	SS		Select Standby
33	SQ		Signal Quality
34	NS		New Signal
35	/TT		Terminal Timing TPR
36	SB		Standby Indicator
37	SC		Send Twister Pair Common

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Contributor: [Joakim Ögren](#), [Petr Krc](#)*

*Source:  
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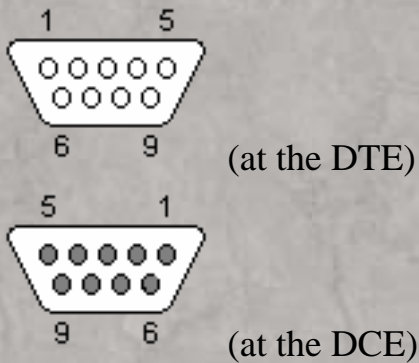
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# RS422 9pin



CORRECT?

9 PIN D-SUB MALE at the DTE (Computer).

9 PIN D-SUB FEMALE at the DCE (Modem).

Pin	Name	Description
1		Shield
2	RTS+	Request To Send +
3	RTS-	Request To Send -
4	TXD+	Transmit Data +
5	TXD-	Transmit Data -
6	CTS+	Clear To Send +
7	CTS-	Clear To Send -
8	RXD+	Received Data +
9	RXD-	Received Data -

*Note: Direction is DTE (Computer) relative DCE (Modem).*

Contributor: [Joakim Ögren](#)

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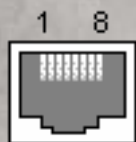
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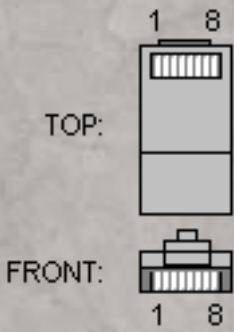


# RocketPort Serialport

Available at RocketPort serialport expansion cards.



(at the RocketPort card)



(at the cables)

RJ45 FEMALE CONNECTOR at the RocketPort card.  
RJ45 MALE CONNECTOR at the cables.

Pin	Name	Description	Dir
1	RTS	Request To Send	→
2	DTR	Data Terminal Ready	→
3	GND	Ground	→
3	TXD	Tranceive Data	→
6	RXD	Receive Data	←
6	DCD	Data Carrier Detect	←
7	DSR	Data Set Ready	←
8	CTS	Clear To Send	←

Contributor: [Joakim Ögren](#), [Karl Asha](#)

Source:  
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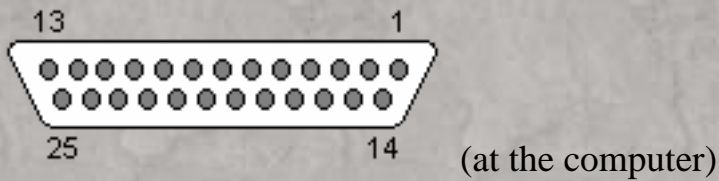
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# SUN LX/Classic/SS4/5/10/20 Serial Port

This port is located in modern SUN Sparcs such as SUN LX/Classic/SS4/5/10/20 and has both serial ports (A/B) in the same connector. Simply plugging in a regular serial cable in results in accessing port A.



25 PIN D-SUB FEMALE at the computer.

Pin	Name	Port	Dir	Description
2	TXD	A	→	Transmit Data
3	RXD	A	←	Receive Data
4	RTS	A	→	Request to Send
5	CTS	A	←	Clear to Send
6	DSR	A	←	Data Set Ready
7	GND	-	-	System Ground
8	CD	A	←	Carrier Detect
11	DTR	B	→	Data Terminal Ready
12	CD	B	←	Carrier Detect
13	CTS	B	←	Clear to Send
14	TXD	B	→	Transmit Data
15	TC	A	←	Transmit Clock from DCE, usually not used
16	RXD	B	←	Receive Data
17	RC	A	←	Receive Clock from DCE, usually not used
18	TC	B	←	Transmit Clock from DCE, usually not used
19	RTS	B	→	Request to Send
20	DTR	A	→	Data Terminal Ready

21	TCO	A		Transmit Clock from DTE, usually not used.
25	TCO	B		Transmit Clock from DTE, usually not used.

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Note: Do not connect SHIELD(1) to GND(7).*

*Contributor:* [Niklas Edmundsson](#)

*Source:*

*SUN Field Engineer Handbook, VolumeII, 12/15/93*

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# Serial (15)

Seems to be available at a 14.4kbps modem called Speedster.

```

      2    4    6      10   12   14
- [ ] [ ] [ ] [ ] [ ] [ ] [ ] [ ] [ ] [ ] [ ] [ ] -
   1    3    5    7 8 9   11   13   15

```

? ?  
? ?  
? ?

(at the modem)

15 PIN FEMALE ??? at the modem.

Pin	Name	RS232	Dir	Description
1	GROUND	GND		Ground
2	SUSP#		?	
3	COMBDSR#	DSR		Data Set Ready
4	COMBRTS#	RTS		Request to Send
5	COMBCTS#	CTS		Clear to Send
6	COMBRI#	RI		Ring Indicator
7	n/c		?	
8	GROUND	GND		Ground
9	+5VIN			+5V DC In
10	COMBDTR#	DTR		Data Terminal Ready
11	COMBDCD#	CD		Carrier Detect
12	COMBTXD	TXD		Transmit Data
13	COMBRXD	RXD		Receive Data
14	SPKDATA		?	
15	GROUND	GND		Ground



*Contributor:* [Joakim Ögren](#), [Joerg Brinkel](#)

*Source:*  
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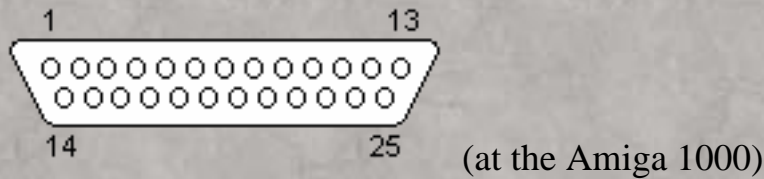
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# Serial (Amiga 1000)



25 PIN D-SUB MALE at the Amiga 1000.

Pin	Name	Dir	Description
1	SHIELD	—	Shield Ground
2	TXD	→	Transmit Data
3	RXD	←	Receive Data
4	RTS	→	Request to Send
5	CTS	←	Clear to Send
6	DSR	←	Data Set Ready
7	GND	—	System Ground
8	CD	←	Carrier Detect
9	n/c	-	
10	n/c	-	
11	n/c	-	
12	n/c	-	
13	n/c	-	
14	-5V	→	-5 Volts DC (50mA max)
15	AUDO	→	Amiga Audio Out (Left)
16	AUDI	←	Amiga Audio In (Right)
17	EB	-	EB=Buffered Port Clock 716 kHz
18	/INT2	?	Interrupt 2
19	n/c	-	
20	DTR	→	Data Terminal Ready

21	+5V		+5 Volts DC
22	n/c	-	
23	+12V		+12 Volts DC (20 mA max)
24	/C2		C2=Clock 3.58MHz
25	/RESET		Reset

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Note: Do not connect SHIELD(1) to GND(7).*

*Contributor: [Joakim Ögren](#)*

*Source:*

*Amiga 4000 User's Guide from Commodore*

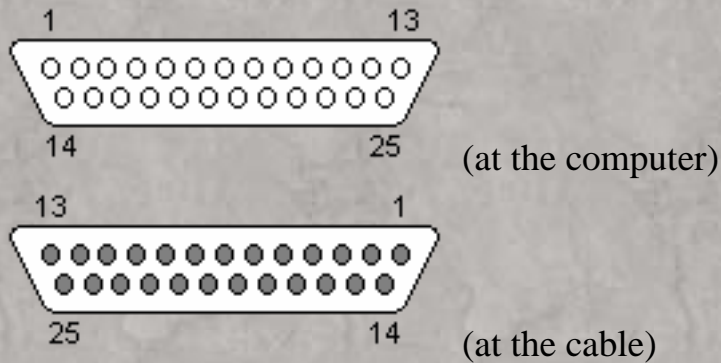
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# Serial (Amiga)






25 PIN D-SUB MALE at the computer.

25 PIN D-SUB FEMALE at the cable.

Pin	Name	Dir	Description
1	SHIELD	—	Shield Ground
2	TXD	→	Transmit Data
3	RXD	←	Receive Data
4	RTS	→	Request to Send
5	CTS	←	Clear to Send
6	DSR	←	Data Set Ready
7	GND	—	System Ground
8	CD	←	Carrier Detect
9	+12V	→	+12 Volts DC (20 mA max)
10	-12V	→	-12 Volts DC (20 mA max)
11	AUDO	→	Amiga Audio Out (Left)
12	n/c	-	Speed Indicate
13	n/c	-	
14	n/c	-	
15	n/c	-	
16	n/c	-	



17	n/c	-	
18	AUDI		Amiga Audio In (Right)
19	n/c	-	
20	DTR		Data Terminal Ready
21	n/c	-	
22	RI		Ring Indicator
23	n/c	-	
24	n/c	-	
25	n/c	-	

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Note: Do not connect SHIELD(1) to GND(7).*

*Contributor: [Joakim Ögren](#)*

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# Serial (MSX)



(at the Computer)

9 PIN D-SUB FEMALE at the Computer.

Pin	Name	Dir	Description
1	PG	-	Protective Ground
2	TXD	→	Transmit Data
3	RXD	←	Receive Data
4	RTS	→	Request to Send
5	CTS	←	Clear to Send
6	DSR	←	Data Set Ready
7	GND	-	Signal Ground
8	DCD	←	Carrier Detect
9	DTR	→	Data Terminal Ready

*Note: Direction is DTE (Computer) relative DCE (Modem).*

Contributor: [Joakim Ögren](#)

Source:  
Mayer's SV738 X'press I/O map

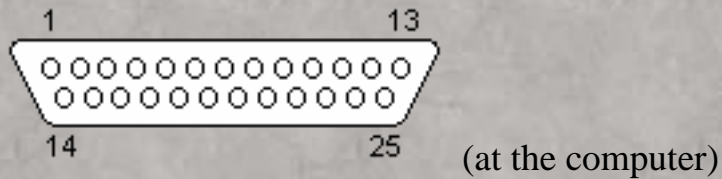
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# Serial (PC 25)



25 PIN D-SUB MALE at the computer.

Pin	Name	Dir	Description
1	SHIELD	-	Shield Ground
2	TXD	→	Transmit Data
3	RXD	←	Receive Data
4	RTS	→	Request to Send
5	CTS	←	Clear to Send
6	DSR	←	Data Set Ready
7	GND	-	System Ground
8	CD	←	Carrier Detect
9	n/c	-	
10	n/c	-	
11	n/c	-	
12	n/c	-	
13	n/c	-	
14	n/c	-	
15	n/c	-	
16	n/c	-	
17	n/c	-	
18	n/c	-	
19	n/c	-	
20	DTR	→	Data Terminal Ready

21	n/c	-	
22	RI		Ring Indicator
23	n/c	-	
24	n/c	-	
25	n/c	-	

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Note: Do not connect SHIELD(1) to GND(7).*

*Contributor:* [Joakim Ögren](#)

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# Serial (PC 9)

Also known as EIA/TIA 574



(at the Computer)

9 PIN D-SUB MALE at the Computer.

Pin	Name	RS232	V.24	Dir	Description
1	CD	CF	109	←	Carrier Detect
2	RXD	BB	104	←	Receive Data
3	TXD	BA	103	→	Transmit Data
4	DTR	CD	108.2	→	Data Terminal Ready
5	GND	AB	102	—	System Ground
6	DSR	CC	107	←	Data Set Ready
7	RTS	CA	105	→	Request to Send
8	CTS	CB	106	←	Clear to Send
9	RI	CE	125	←	Ring Indicator

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Note: RS232 column is RS232 circuit name.*

*Note: V.24 column is ITU-TSS V.24 circuit name.*

Contributor: [Joakim Ögren](#)

Source:

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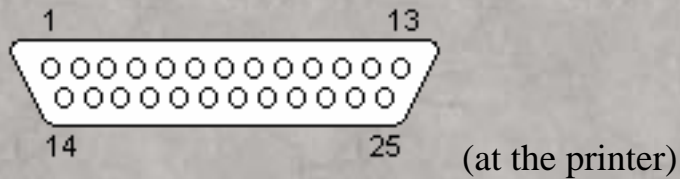
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# Serial (Printer)



25 PIN D-SUB MALE at the printer.

Pin	Name	Dir	Description
1	SHIELD	—	Shield Ground
2	TXD	→	Transmit Data
3	RXD	←	Receive Data
4	n/c	-	Not connected
5	n/c	-	Not connected
6	DSR	←	Data Set Ready
7	GND	—	System Ground
8	DCD	←	Data Carrier Detect
9	n/c	-	Not connected
10	n/c	-	Not connected
11	?	→	Reverse Channel
12	n/c	-	Not connected
13	n/c	-	Not connected
14	n/c	-	Not connected
15	n/c	-	Not connected
16	n/c	-	Not connected
17	TTY-TXD	→	TTY Receive Data
18	n/c	-	Not connected
19	n/c	-	Not connected
20	DTR	→	Data Terminal Ready

21	n/c	-	Not connected
22	n/c	-	Not connected
23	?		TTY Receive Data Return
24	?		TTY Transmit Data Return
25	TTY-RXD		TTY Receive Data

Contributor: [Joakim Ögren](#), [Petr Krc](#)

Source:

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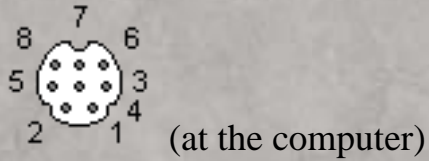
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# Serial (SGI MiniDIN)



8 PIN MINI-DIN (CENTER PIN) FEMALE at the computer.

Pin	Name	Dir	Description
1	DTR	→	Data Terminal Ready
2	CTS	←	Clear to Send
3	TXD	→	Transmit Data
4	GND	—	System Ground
5	RXD	←	Receive Data
6	RTS	→	Request to Send
7	CD	←	Carrier Detect
8	GND	—	System Ground

*Note: Direction is DTE (Computer) relative DCE (Modem).*

*Contributor:* [Egon Kastelijn](#)

*Source:*  
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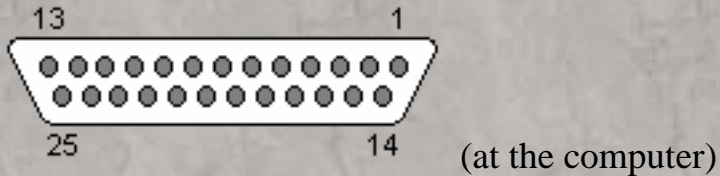
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*Document last modified:* 2001-06-07





# Serial (SUN)

Available on SUN computers since the SUN3 series (1988) to the current UltraSparc systems (RS423/RS232)



25 PIN D-SUB FEMALE at the computer.

Pin	Name	Dir	Description
1	n/c	-	
2	TXD	→	Transmit Data
3	RXD	←	Receive Data
4	RTS	→	Request to Send
5	CTS	←	Clear to Send
6	DSR	←	Data Set Ready
7	GND	-	System Ground
8	DCD	←	Data Carrier Detect
9	n/c	-	
10	n/c	-	
11	n/c	-	
12	n/c	-	
13	n/c	-	
14	n/c	-	
15	TRxC	←	Transmit Clock
16	n/c	-	
17	RTxC	←	Receive Clock

18	n/c	-	
19	n/c	-	
20	DTR		Data Terminal Ready
21	n/c	-	
22	n/c	-	
23	n/c	-	
24	TxC		Transmit Clock
25	n/c	-	

*Note: Direction is DTE (Computer) relative DCE (Modem).*

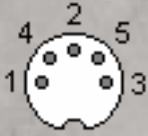
*Contributor: [Joakim Ögren](#)*

*Source:  
SUN SPARCengine Ultra 20 OEM Manual*

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# Amstrad CPC6128 Tape



(at the computer)

5 PIN DIN 180° (DIN41524) FEMALE at the computer.

Pin	Name
1	REMOTE SWITCH
2	GND
3	REMOTE SWITCH
4	DATA IN
5	DATA OUT

Contributor: [Joakim Ögren](#), [Agnello Guarracino](#)

Source:  
*Amstrad CPC6128 User Instructions Manual*

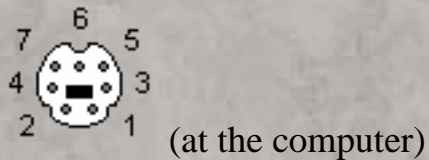
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# C16/C116/+4 Cassette

Available on the Commodore C16, C116 and +4 computers.



7 PIN MINI-DIN FEMALE at the computer.

Pin	Name	Dir	Description
1	GND	—	Ground
2	+5V	→	+5 Volts DC
3	MOTOR	→	Cassette Motor
4	READ	←	Cassette Read
5	WRITE	→	Cassette Write
6	SENSE	→	Cassette Sense
7	GND	—	Ground

*Note: Direction is Computer relative Cassette.*

Contributor: [Joakim Ögren](#), [Arwin Vosselman](#)

Source:  
SAMS Computerfacts CC8 Commodore 16

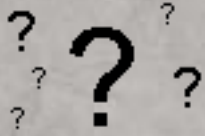
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# C64 Cassette



(at the computer)

6 PIN MALE EDGE at the computer.

Pin	Name	Dir	Description
A-1	GND		Ground
B-2	+5V		+5 Volts DC
C-3	MOTOR		Cassette Motor
D-4	READ		Cassette Read
E-5	WRITE		Cassette Write
F-6	SENSE		Cassette Sense

*Note: Direction is Computer relative Cassette.*

*Contributor: [Joakim Ögren](#), [Arwin Vosselman](#)*

*Source:  
Commodore 64 Programmer's Reference Guide*

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# Cassette TI-99/4a



(at the computer)



(at the cassette cable)

9 PIN D-SUB MALE at the Computer.

9 PIN D-SUB FEMALE at the Cassette cable.

Pin	Name	Dir	Comment
1	Cass 1 motor control	OUT	CRU bit 22
2	Dito	OUT	neg
3	Output to tape 2	OUT	CRU bit 25
4	Audio gate	OUT	CRU bit 24
5	Output to tape 2	OUT	neg
6	Cass 2 motor control	OUT	CRU bit 23
7	Dito	OUT	neg
8	Input from tape 1 or 2	IN	CRU bit 27
9	Dito	IN	neg

*Note: Direction is Computer relative Cassette.*

*Note: Cassette 1 can't be written to.*

Contributor: [Joakim Ögren](#)

Source:

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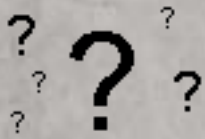
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# CoCo Cassette

Available on the Tandy/Radio Shack Color Computer (CoCo).



(at the CoCo)

UNKNOWN CONNECTOR at the CoCo.

Pin	Description
1	Motor Relay
2	Ground
3	Motor Relay
4	Signal Input
5	Signal Output

Contributor: [Joakim Ögren](#)

Source:

[Tandy Color Computer FAQ](#) at [Video Game Advantage's homepage](#)

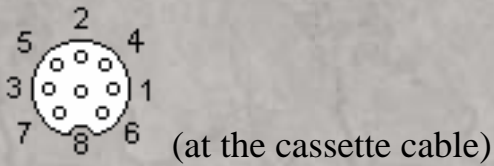
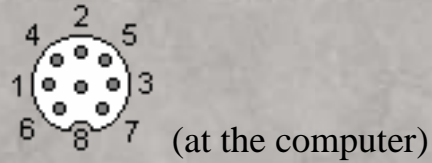
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# MSX Cassette



8 PIN DIN (DIN45326) FEMALE at the computer.

8 PIN DIN (DIN45326) MALE at the cassette cable.

Pin	Name	Dir	Description
1	GND	—	Ground
2	GND	—	Ground
3	GND	—	Ground
4	CMTOUT	→	Sound Output
5	CMTIN	←	Sound Input
6	REM+	→	Remote control (from relay)
7	REM-	→	Remote control (from relay)
8	GND	—	Ground

*Note: Direction is Computer relative Cassette.*

Contributor: [Joakim Ögren](#)

Source:  
Mayer's SV738 X'press I/O map

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# Spectravideo SVI318/328 Cassette

```
+-----+
| 1  2  3  4  5  6  7 |
+-----+
```

? ?  
? ? ?

(at the computer)

7 PIN FEMALE EDGE CONNECTOR at the computer.

Pin	Name	Description
1	12v	Power 100mA
2	CASR	Cassette data read
3	CASW	Cassette data write
4	AUDIO	Cassette audio
5	GND	System ground
6	ME	
7	READY	System Ready

Contributor: [Rob Gill](#)

Source:  
*SVI mk II user manual*

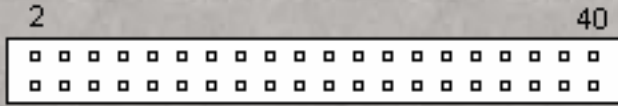
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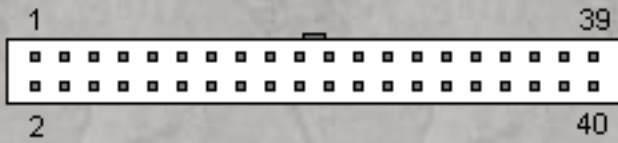
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# Mitsumi CD-ROM



(at the controller & CD-ROM)



(at the cable.)

40 PIN IDC MALE at the controller & CD-ROM.

40 PIN IDC FEMALE at the cable.

Pin	Name	Description
1	A0	Address Bit 0
2	GND	Ground
3	A1	Address Bit 1
4	GND	Ground
5	n/c	Not connected
6	GND	Ground
7	n/c	Not connected
8	GND	Ground
9	n/c	Not connected
10	GND	Ground
11	n/c	Not connected
12	GND	Ground
13	INT	Interrupt
14	GND	Ground
15	REQ	Data request For DMA
16	GND	Ground



17	ACK	Data Acknowledge For DMA
18	GND	Ground
19	RE	Read Enable
20	GND	Ground
21	WE	Write Enable
22	GND	Ground
23	EN	Bus Enable
24	GND	Ground
25	DB0	Data Bit 0
26	GND	Ground
27	DB1	Data Bit 1
28	GND	Ground
29	DB2	Data Bit 2
30	GND	Ground
31	DB3	Data Bit 3
32	GND	Ground
33	DB4	Data Bit 4
34	GND	Ground
35	DB5	Data Bit 5
36	GND	Ground
37	DB6	Data Bit 6
38	GND	Ground
39	DB7	Data Bit 7
40	GND	Ground

Contributor: [Keith Solomon](#)

Source:  
*SoundFX 16-bit Multimedia Kit Hardware Manual from Reveal*

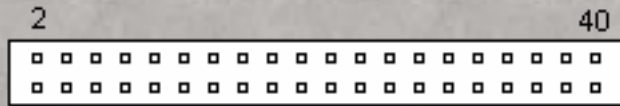
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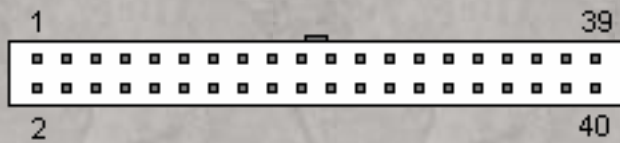
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# Panasonic CD-ROM



(at the controller & CD-ROM)



(at the cable.)

40 PIN IDC MALE at the controller & CD-ROM.

40 PIN IDC FEMALE at the cable.

Pin	Name	Description
1	GND	Ground
2	RESET	CD-Reset
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	MODE0	Operation Mode Bit 0
7	GND	Ground
8	MODE1	Operation Mode Bit 1
9	GND	Ground
10	WRITE	CD-Write
11	GND	Ground
12	READ	CD-Read
13	GND	Ground
14	ST0	CD-Status Bit 0
15	GND	Ground
16	n/c	No Connection

17	GND	Ground
18	n/c	No Connection
19	GND	Ground
20	ST1	CD-Status Bit 1
21	GND	Ground
22	EN	CD-Data Enable
23	GND	Ground
24	ST2	CD-Status Bit 2
25	GND	Ground
26	S/DE	CD-Status/Data Enable
27	GND	Ground
28	ST3	CD-Status Bit 3
29	GND	ground
30	GND	ground
31	D7	CD-Data 7
32	D6	CD-Data 6
33	GND	ground
34	D5	CD-Data 5
35	D4	CD-Data 4
36	D3	CD-Data 3
37	GND	ground
38	D2	CD-Data 2
39	D1	CD-Data 1
40	D0	CD-Data 0

Contributor: [Keith Solomon](#)

Source:

*SoundFX 16-bit Multimedia Kit Hardware Manual from Reveal*

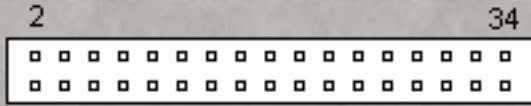
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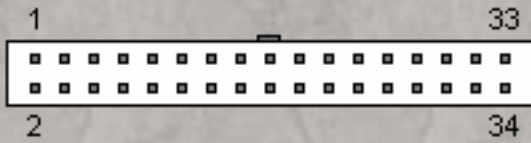
*Document last modified: 2001-06-07*



# Sony CD-ROM



(at the controller & CD-ROM)



(at the cable.)

34 PIN IDC MALE at the controller & CD-ROM.

34 PIN IDC FEMALE at the cable.

Pin	Name	Description
1	RESET	Reset
2	GND	Ground
3	DB7	Data Bit 7
4	GND	Ground
5	DB6	Data Bit 6
6	GND	Ground
7	DB5	Data Bit 5
8	GND	Ground
9	DB4	Data Bit 4
10	GND	Ground
11	DB3	Data Bit 3
12	GND	Ground
13	DB2	Data Bit 2
14	GND	Ground
15	DB1	Data Bit 1
16	GND	Ground



17	DB0	Data Bit 0
18	GND	Ground
19	WE	Write Enable
20	GND	Ground
21	RE	Read Enable
22	GND	Ground
23	ACK	Data Acknowledge For DMA
24	GND	Ground
25	REQ	Data Request For DMA
26	GND	Ground
27	INT	Interrupt
28	GND	Ground
29	A1	Address Bit 1
30	GND	Ground
31	A0	Address Bit 0
32	GND	Ground
33	EN	Bus Enable
34	GND	Ground

Contributor: [Keith Solomon](#)

Source:

*SoundFX 16-bit Multimedia Kit Hardware Manual from Reveal*

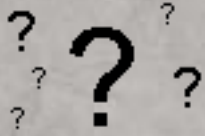
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# 8" Floppy Diskdrive



(at the computer)

50 PIN EDGE or IDC at the computer??.

Pin	Name	Dir	Description
2	/REDWC	←	Reduced Write Current
4	n/c	-	Reserved
6	n/c	-	Reserved
8	n/c	-	Reserved
10	/FD2S	←	Disk is two sided
12	/DCG	←	Disk has been changed/door open
14	/SIDE	→	Side select
16	/DLOCK	→	Door lock
18	/HLD	→	Head load
20	/INDEX	←	Index Pulse
22	/READY	←	Ready
24	n/c	-	Not connected
26	/SEL1	←	Select Drive 1
28	/SEL2	←	Select Drive 2
30	/SEL3	←	Select Drive 3
32	/SEL4	←	Select Drive 4
34	/DIR	→	Direction
36	/STEP	→	Step
38	/WDAT	→	Write data
40	/WGAT	→	Write gate

42	/TR00		Track 00 (Zero)
44	/WPROT		Write protect
46	/RDATA		Read data
48	n/c	-	Not connected
50	n/c	-	Not connected

*Note: Direction is Computer relative Diskdrive.*

*Note: All odd pins are GND, Ground.*

*Contributor: [Joakim Ögren](#), [Dennis Painter](#)*

*Source:*

*?*

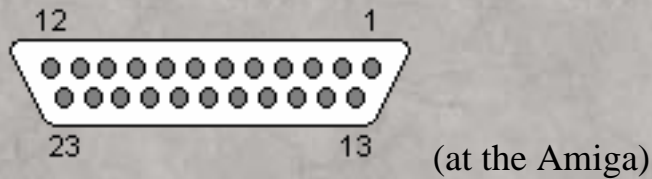
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# Amiga External Diskdrive



23 PIN D-SUB FEMALE at the Amiga.

Pin	Name	Dir	Description
1	/RDY	↔	Disk Ready
2	/DKRD	→	Disk Read Data
3	GND	—	Ground
4	GND	—	Ground
5	GND	—	Ground
6	GND	—	Ground
7	GND	—	Ground
8	/MTRXD	OC	Disk Motor Control
9	/SEL2	OC	Select Drive 2
10	/DRES	OC	Disk Reset
11	/CHNG	↔	Disk Removed From Drive-Latched Low
12	+5V	→	+5 Volts DC (250 mA max)
13	/SIDE	→	Select Disk Side (0=Upper, 1=Lower)
14	/WPRO	↔	Disk is Write Protected
15	/TKO	↔	Drive Head position over Track 0
16	/DKWE	OC	Disk Write Enable
17	/DKWD	OC	Disk Write Data
18	/STEP	OC	Step the Head-Pulse, First low, then high
19	DIR	OC	Select Head Direction (0=Inner, 1=Outer)
20	/SEL3	OC	Select Drive 3



21	/SEL1	OC	Select Drive 1
22	/INDEX	OC	Disk Index Pulse
23	+12V		+12 Volts DC (160 mA max, 540 mA surge)

*Note: Direction is Computer relative Diskdrive.*

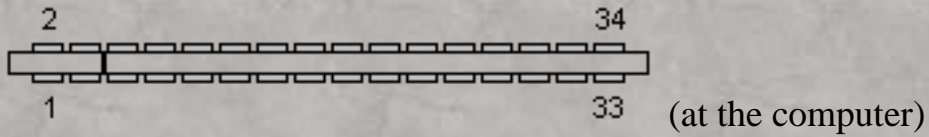
*Contributor:* [Joakim Ögren](#)

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*Amiga 4000 User's Guide from Commodore*

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# Amstrad CPC6128 Diskdrive 2



34 PIN MALE EDGE at the computer.

Pin	Name
1	READY
2	GND
3	SIDE 1 SELECT
4	GND
5	READ DATA
6	GND
7	WRITE PROTECT
8	GND
9	TRACK 0
10	GND
11	WRITE GATE
12	GND
13	WRITE DATA
14	GND
15	STEP
16	GND
17	DIRECTION SELECT
18	GND
19	MOTOR ON
20	GND

21	n/c
22	GND
23	DRIVE SELECT 1
24	GND
25	n/c
26	GND
27	INDEX
28	GND
29	n/c
30	GND
31	n/c
32	GND
33	n/c
34	GND

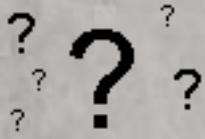
Contributor: [Joakim Ögren](#), [Agnello Guarracino](#)

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# Amstrad CPC6128 Plus External Diskdrive



(at the Computer)

36 PIN D-SUB MALE at the Computer.

Pin	Name	Dir	Description
1	n/c	-	Not connected
3	n/c	-	Not connected
5	n/c	-	Not connected
7	NINDEX	?	
9	n/c	-	Not connected
11	NDSEL1	?	
13	n/c	-	Not connected
15	NMOTOR	?	
17	NDSEL	?	
19	NSTEP	→	Step head
21	NWDATA	→	Write Data
23	NWGATE	→	Write Gate
25	NTK00	←	Track 00
27	NWRPT	←	Write Protect
29	NRDDTA	←	Read Data
31	NSIDE1	?	
33	NREADY	?	
35	n/c		Not connected



*Note: Direction is Computer relative Diskdrive.*

*Note: All even pins are GND, Ground.*

*Contributor: [Joakim Ögren](#), [Colin Gaunt](#)*

*Source:*

*Amstrad 6128 Plus Home Computer Manual*

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# Apple Macintosh External Drive

## 19 PIN D-SUB CONNECTOR

Pin	Name	Description
1	Ground	
2	Ground	
3	Ground	
4	Ground	
5	-12V	-12 VDC
6	+5V	+5 VDC
7	+12V	+12 VDC
8	+12V	+12 VDC
9	?	?
10	PWM	Regulates speed of the drive
11	PH0	Control line to send commands to the drive
12	PH1	Control line to send commands to the drive
13	PH2	Control line to send commands to the drive
14	PH3	Control line to send commands to the drive
15	WrReq-	Turns on the ability to write data to the drive
16	HdSel	Control line to send commands to the drive
17	Enb12-	Enables the Rd line (else Rd is tri-stated)
18	Rd	Data actually read from the drive
19	Wr	Data actually written to the drive

Contributor: [Joakim Ögren](#)

Source:

[Technote HW19: Pinouts](#) at [Apple Technical Notes](#)

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*Document last modified: 2000-07-09*



# Apple Macintosh Internal Floppy disk drive

## 20 PIN UNKNOWN CONNECTOR

Pin	Name	Description
1	GND	Ground
2	PH0	Phase 0: state control line
3	GND	Ground
4	PH1	Phase 1: state control line
5	GND	Ground
6	PH2	Phase 2: state control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	+5V	+5 volts
10	/WRREQ	Write data request
11	+5V	+5 volts
12	SEL	Head select
13	+12V	+12 volts
14	/ENBL	Drive enable
15	+12V	+12 volts
16	RD	Read data
17	+12V	+12 volts
18	WR	Write data
19	+12V	+12 volts
20	n.c.	Not connected

Contributor: [Joakim Ögren](#)



*Source:*

*Apple Power Macintosh 5400 Developer Note*

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# Atari Floppy Port

**NOT  
DRAWN  
YET...**



(at the Computer)

**NOT  
DRAWN  
YET...**



(at the Diskdrive)

14 PIN DIN FEMALE at the Computer.

14 PIN DIN MALE at the Diskdrive.

Pin	Name	Description
1	RD	Read Data
2	SIDE0	Side 0 Select
3	GND	Ground
4	INDEX	Index
5	SEL0	Drive 0 Select
6	SEL1	Drive 1 Select
7	GND	Ground
8	MOTOR	Motor On
9	DIR	Direction In
10	STEP	Step
11	WD	Write Data
12	WG	Write Gate
13	TRK00	Track 00
14	WP	Write Protect

Contributor: [Joakim Ögren](#), [Lawrence Wright](#), [Steve & Sally Blair](#)

*Source:*

*?*

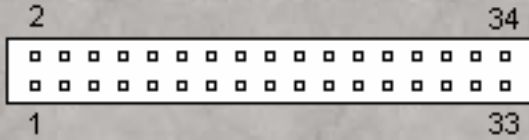
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# Internal Diskdrive



(at the computer & diskdrives)

34 PIN IDC MALE at the computer & diskdrives.

Pin	Name	Dir	Description
2	/REDWC	→	Density Select
4	n/c		Reserved
6	n/c		Reserved
8	/INDEX	←	Index
10	/MOTEA	→	Motor Enable A
12	/DRVSB	→	Drive Sel B
14	/DRVSA	→	Drive Sel A
16	/MOTEB	→	Motor Enable B
18	/DIR	→	Direction
20	/STEP	→	Step
22	/WDATE	→	Write Data
24	/WGATE	→	Floppy Write Enable
26	/TRK00	←	Track 0
28	/WPT	←	Write Protect
30	/RDATA	←	Read Data
32	/SIDE1	→	Head Select
34	/DSKCHG	→	Disk Change

*Note: Direction is Computer relative Diskdrive.*

*Note: All odd pins are GND, Ground.*



*Note: Can be an Edge-connector on old PC's.*

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*Source:  
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# Macintosh External Drive

**NOT  
DRAWN  
YET...**



(at the Computer)

**NOT  
DRAWN  
YET...**





(at the Diskdrive)

19 PIN D-SUB FEMALE at the Computer.

19 PIN D-SUB MALE at the Diskdrive.

Pin	Name	Dir	Description
1	CGND		Chassis ground
2	CGND		Chassis ground
3	CGND		Chassis ground
4	CGND		Chassis ground
5	-12V		-12 VDC
6	+5V		+5 VDC
7	+12V		+12 VDC
8	+12V		+12 VDC
9	n/c	-	Not connected
10	PWM	?	Regulates speed of the drive
11	CA0	?	Control line to send commands to the drive
12	CA1	?	Control line to send commands to the drive
13	CA2	?	Control line to send commands to the drive
14	LSTRB	?	Control line to send commands to the drive
15	/WrReq	?	Turns on the ability to write data to the drive
16	HdSel	?	Control line to send commands to the drive

17	/Enbl2	?	Enables the Rd line (else Rd is tri-stated)
18	Rd		Data actually read from the drive
19	Wr		Data actually written to the drive

*Note: Direction is Computer relative Diskdrive.*

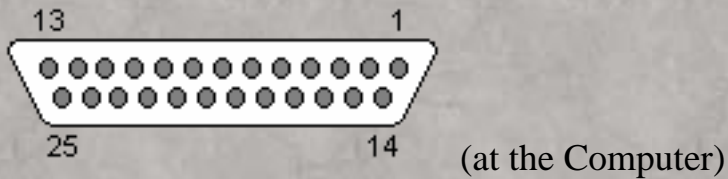
*Contributor:* [Ben Harris](#)

*Source:*  
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# MSX External Diskdrive



25 PIN D-SUB FEMALE at the Computer.

Pin	Name	Dir	Description
1	+12V	→	+12 VDC
2	+5V	→	+5 VDC
3	+5V	→	+5 VDC
4	/INDEX	←	Sector hole passed sensor.
5	/DSEL1	→	Drive Select 1
6	DIR	→	Direction (0=In, 1=Dir)
7	/STEP	→	Moves head 1 step in DIR direction.
8	WRITEDATA	→	Write Data
9	/WRITEGATE	→	Write Gate
10	/TRACK00	←	Head is over Track 00 (outermost track)
11	/WRITEPROTECT	←	Write protected disk (0=Write protected)
12	READDATA	←	Data read from diskette.
13	/SIDESELECT	→	Side Select (0=Side 1, 1=Side 0)
14	+12V	→	+12 VDC
15	+12V	→	+12 VDC
16	+5V	→	+5 VDC
17	/DSEL1	→	Select Drive 0
18	/MOTOR	→	Motor On
19	READY	←	Ready
20	GND	—	Ground



21	GND		Ground
22	GND		Ground
23	GND		Ground
24	GND		Ground
25	GND		Ground

*Note: Direction is Computer relative Diskdrive.*

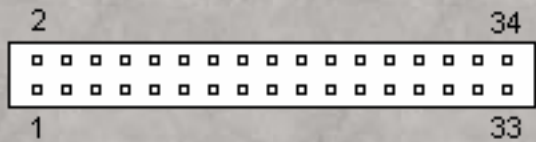
*Contributor:* [Joakim Ögren](#)

*Source:*  
*Mayer's SV738 X'press I/O map*

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# SUN Internal Floppydrive



(at the computer & diskdrives)

34 PIN IDC MALE at the computer & diskdrives.

Pin	Name
1	GND
2	FD_DENSEL
3	GND
4	33_W_to_VCC
5	GND
6	FD_DRATE0_MSEN0
7	N/C
8	FD_INDEX_L
9	GND
10	MTR0_L
11	GND
12	FD_DRV1_SEL_L
13	N/C
14	FD_DRV0_SEL_L
15	GND
16	FD_MTR1_L
17	MSEN1
18	FD_DIR_L
19	GND
20	FD_STEP_L

21	GND
22	FD_WR_DAT_L
23	GND
24	FD_WR_GATE_L
25	GND
26	FD_TRK0_L
27	MSEN0
28	FD_WR_PROT_L
29	GND
30	FD_RD_DAT_L
31	GND
32	FD_HD_SEL_L
33	GND
34	FD_DSK_CHNG_L

*Contributor:* [Joakim Ögren](#)

*Source:*  
*SUN SPARCengine Ultra AXmp Manual*

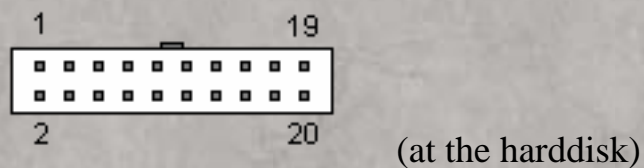
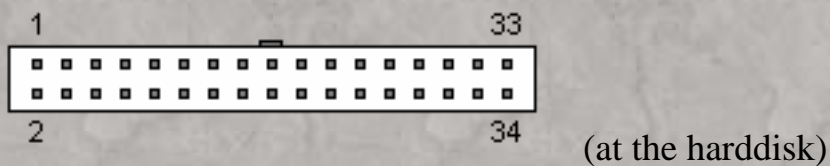
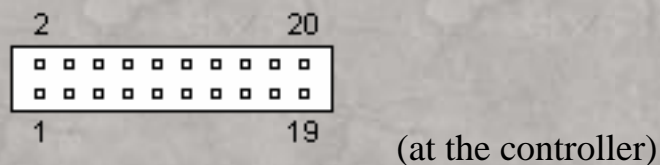
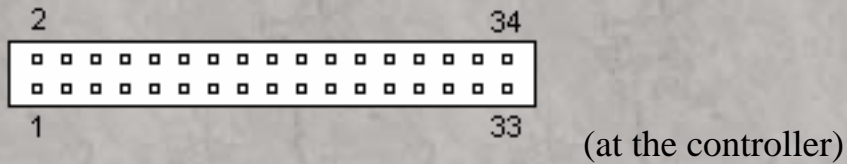
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# ESDI

ESDI=Enhanced Small Device Interface.

Developed by Maxtor in the early 1980's as an upgrade and improvement to the ST506 design.



34 PIN IDC MALE at the Controller.

20 PIN IDC MALE at the Controller.

34 PIN IDC FEMALE at the Harddisk.

20 PIN IDC FEMALE at the Harddisk.

## Control connector

Pin	Name	Description
2		Head Sel 3
4		Head Sel 2
6		Write Gate



8	Config/Stat Data
10	Transfer Acknowledge
12	Attention
14	Head Sel 0
16	Sect/Add MK Found
18	Head Sel 1
20	Index
22	Ready
24	Transfer Request
26	Drive Sel 1
28	Drive Sel 2
30	Drive Sel 3
32	Read Gate
34	Command Data

*Note: All odd are GND, Ground.*

## Data connector

Pin	Name	Description
1		Drive Selected
2		Sect/Add MK Found
3		Seek Complete
4		Address Mark Enable
5		(reserved, for step mode)
6	GND	Ground
7		Write Clock+
8		Write Clock-
9		Cartridge Changed
10		Read Ref Clock+
11		Read Ref Clock-
12	GND	Ground

13		NRZ Write Data+
14		NRZ Write Data-
15	GND	Ground
16	GND	Ground
17		NRZ Read Data+
18		NRZ Read Data-
19	GND	Ground
20	GND	Ground

*Contributor:* [Joakim Ögren](#)

*Source:*

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# PC Card ATA

This specification makes it possible to share ATA & PC Card with the same connectors.

**NOT  
DRAWN  
YET...**



(at the controller)

**NOT  
DRAWN  
YET...**






























(at the peripherals)
















68 PIN ??? MALE at the controller.

68 PIN ??? FEMALE at the peripherals.

Pin	Name	Host	Dir	Dev	PC-Card equiv
1	Ground	x	→	x	Ground
2	DD3	x	↔	x	D3
3	DD4	x	↔	x	D4
4	DD5	x	↔	x	D5
5	DD6	x	↔	x	D6
6	DD7	x	↔	x	D7
7	/CS0	x	→	x	/CE1
8			→	i	A10
9	/SELATA	x	→	x	/OE
10					
11	/CS1	x	→	x <sup>1)</sup>	A9
12			→	i	A8
13					
14					

15				i	/WE
16	INTRQ	x		x	/READY:IREQ
17	VCC	x		x	VCC
18					
19					
20					
21					
22				i	A7
23				i	A6
24				i	A5
25				i	A4
26				i	A3
27	DA2	x		x	A2
28	DA1	x		x	A1
29	DA0	x		x	A0
30	DD0	x		x	D0
31	DD1	x		x	D1
32	DD2	x		x	D2
33	/IOCS16	x		x	/WP:IOIS16
34	Ground	x		x	Ground
35	Ground	x		x	Ground
36	/CD1	x		x	/CD1
37	DD11	x		x	D11
38	DD12	x		x	D12
39	DD13	x		x	D13
40	DD14	x		x	D14
41	DD15	x		x	D15
42	/CS1	x		x <sup>1)</sup>	/CE2
43				i	/VS1
44	/DIOR	x		x	/IORD
45	/DIOW	x		x	/IOWR



46					
47					
48					
49					
50					
51	VCC	x		x	VCC
52					
53					
54					
55	M/S-	x		x <sup>2)</sup>	
56	CSEL	x		x <sup>2)</sup>	
57				i	/VS2
58	/RESET	x		x	RESET
59	IORDY	o		x <sup>3)</sup>	/WAIT
60	DMARQ	o		x <sup>3)</sup>	/INPACK
61	/DMACK	o		o	/REG
62	/DASP	x		x	/BVD2:SPKR
63	/PDIAG	x		x	/BVD1:STSCHG
64	DD8	x		x	D8
65	DD9	x		x	D9
66	DD10	x		x	D10
67	/CD2	x		x	/CD2
68	Ground	x		x	Ground

*x = Required.*

*i = Ignored by host in ATA mode.*

*o = Optional.*

*nothing = Not connected.*

<sup>1)</sup> Device shall support only one /CS1 signal pin.

<sup>2)</sup> Device shall support either /M/S or CSEL but not both.

<sup>3)</sup> Device shall hold this signal negated if it does not support this function.

Contributor: [Joakim Ögren](#)

*Source:  
ATA-2 specifications*

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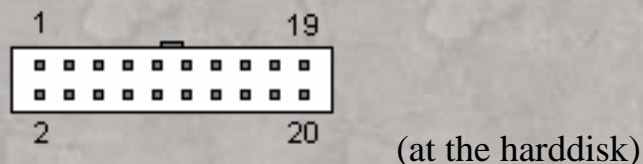
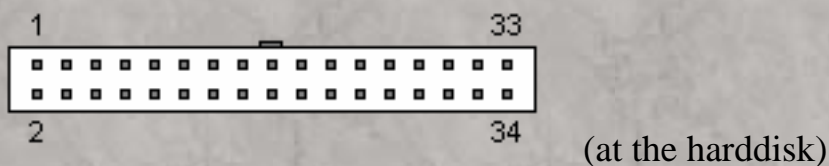
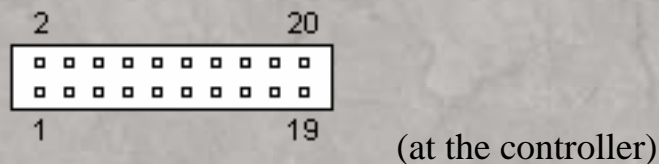
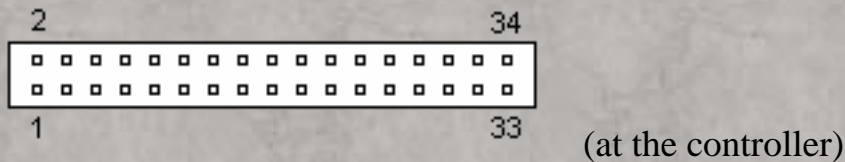


# ST506/412

Developed by Seagate.

Also known as MFM or RLL since these are the encoding methods used to store data. Seagate originally developed it to support their ST506 (5 MB) and ST412 (10 MB) drives.

The first drives used an encoding method called MFM (Modified Frequency Modulation). Later a new encoding method was developed, RLL (Run Length Limited). RLL had the advantage that it was possible to store 50% more with it. But it required better drives. This is almost never an problem. Often called 2,7 RLL because the recording scheme involves patterns with no more than 7 successive zeros and no less than two.



34 PIN IDC MALE at the Controller.

20 PIN IDC MALE at the Controller.

34 PIN IDC FEMALE at the Harddisk.

20 PIN IDC FEMALE at the Harddisk.

## Control connector

Pin	Name	Description
2		Head Sel 8
4		Head Sel 4
6		Write Gate
8		Seek Complete
10		Track 0
12		Write Fault
14		Head Sel 1
16	RES	(reserved)
18		Head Sel 2
20		Index
22		Ready
24		Step
26		Drive Sel 1
28		Drive Sel 2
30		Drive Sel 3
32		Drive Sel 4
34		Direction In

*Note: All odd pins are GND, Ground.*

## Data connector

Pin	Name	Description
1		Drive Selected
2	GND	Ground
3	RES	(reserved)
4	GND	Ground
5	RES	(reserved)
6	GND	Ground
7	RES	(reserved)
8	GND	Ground



9	RES	(reserved)
10	RES	(reserved)
11	GND	Ground
12	GND	Ground
13		Write Data+
14		Write Data-
15	GND	Ground
16	GND	Ground
17		Read Data+
18		Read Data-
19	GND	Ground
20	GND	Ground

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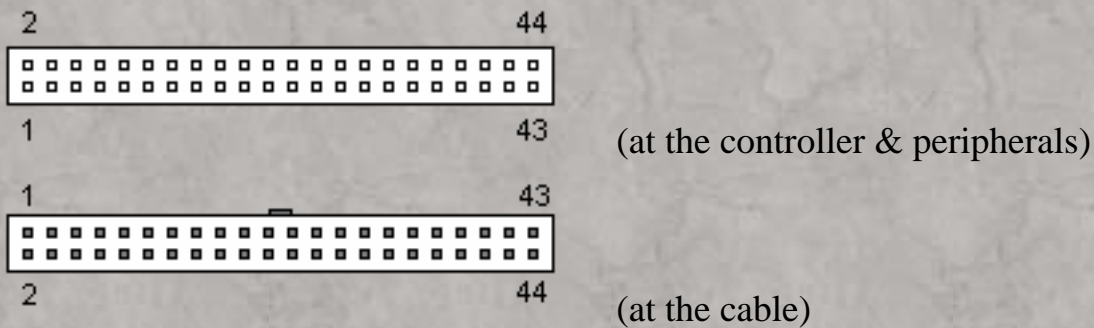
*Document last modified:* 2001-06-07



# ATA (44) Internal

ATA=AT bus Attachment.

This connector is mostly used for 2.5" internal harddisks.  
See [ATA](#) for pin 1-40.



44 PIN IDC (0.75") MALE at the controller & peripherals.  
44 PIN IDC (0.75") FEMALE at the cable.

Pin	Name	Dir	Description
41	+5VL	→	+5 VDC (Logic)
42	+5VM	→	+5 VDC (Motor)
43	GND	→	Ground
44	/TYPE	→	Type (0=ATA)

*Note: Direction is Controller relative Devices (harddisks).*

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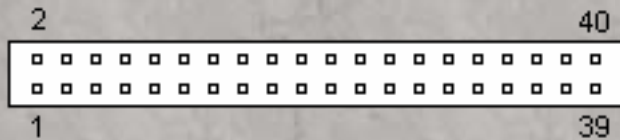
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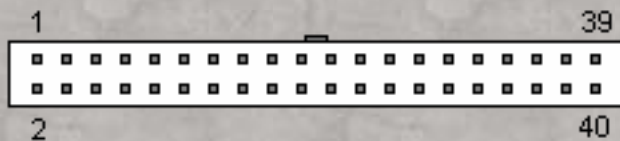
# ATA Internal

ATA=AT bus Attachment..

Developed by Western Digital, Conner & Seagate ?.



(at the controller & peripherals)























(at the cable)

40 PIN IDC MALE at the controller & peripherals.

40 PIN IDC FEMALE at the cable.

Pin	Name	Dir	Description
1	/RESET	→	Reset
2	GND	—	Ground
3	DD7	↔	Data 7
4	DD8	↔	Data 8
5	DD6	↔	Data 6
6	DD9	↔	Data 9
7	DD5	↔	Data 5
8	DD10	↔	Data 10
9	DD4	↔	Data 4
10	DD11	↔	Data 11
11	DD3	↔	Data 3
12	DD12	↔	Data 12
13	DD2	↔	Data 2
14	DD13	↔	Data 13

15	DD1		Data 1
16	DD14		Data 14
17	DD0		Data 0
18	DD15		Data 15
19	GND		Ground
20	KEY	-	Key (Pin missing)
21	DMARQ	?	DMA Request
22	GND		Ground
23	/DIOW		Write Strobe
24	GND		Ground
25	/DIOR		Read Strobe
26	GND		Ground
27	IORDY		I/O Ready
28	SPSYNC:CSEL	?	Spindle Sync or Cable Select
29	/DMACK	?	DMA Acknowledge
30	GND		Ground
31	INTRQ		Interrupt Request
32	/IOCS16	?	IO ChipSelect 16
33	DA1		Address 1
34	PDIAG	?	Passed Diagnostics
35	DA0		Address 0
36	DA2		Address 2
37	/IDE_CS0		(1F0-1F7)
38	/IDE_CS1		(3F6-3F7)
39	/ACTIVE		Led driver
40	GND		Ground

*Note: Direction is Controller relative Devices (Harddisks).*

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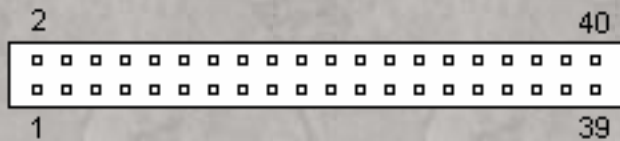


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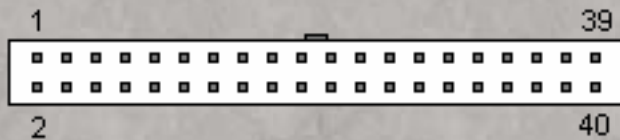
IDE=Integrated Drive Electronics.

Developed by Compaq and Western Digital.

Newer version of IDE goes under the name ATA=AT bus Attachment.



(at the controller & peripherals)

























(at the cable)

40 PIN IDC MALE at the controller & peripherals.

40 PIN IDC FEMALE at the cable.

Pin	Name	Dir	Description
1	/RESET	→	Reset
2	GND	—	Ground
3	DD7	↔	Data 7
4	DD8	↔	Data 8
5	DD6	↔	Data 6
6	DD9	↔	Data 9
7	DD5	↔	Data 5
8	DD10	↔	Data 10
9	DD4	↔	Data 4
10	DD11	↔	Data 11
11	DD3	↔	Data 3
12	DD12	↔	Data 12
13	DD2	↔	Data 2

14	DD13		Data 13
15	DD1		Data 1
16	DD14		Data 14
17	DD0		Data 0
18	DD15		Data 15
19	GND		Ground
20	KEY	-	Key
21	n/c	-	Not connected
22	GND		Ground
23	/IOW		Write Strobe
24	GND		Ground
25	/IOR		Read Strobe
26	GND		Ground
27	IO_CH_RDY		
28	ALE		Address Latch Enable
29	n/c	-	Not connected
30	GND		Ground
31	IRQ		Interrupt Request
32	/IOCS16	?	IO ChipSelect 16
33	DA1		Address 1
34	n/c	-	Not connected
35	DA0		Address 0
36	DA2		Address 2
37	/IDE_CS0		(1F0-1F7)
38	/IDE_CS1		(3F6-3F7)
39	/ACTIVE		Led driver
40	GND		Ground

*Note: Direction is Controller relative Devices (Harddisks).*

Contributors: [Joakim Ögren](#), [Dan Williams](#)

Source:

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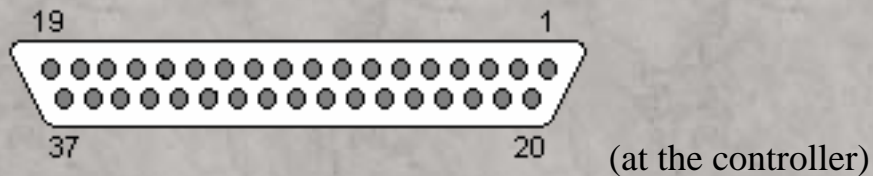
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# Paravision SX-1 External IDE

Paravision was formerly known as Microbotics.



37 PIN D-SUB FEMALE at the controller.

Pin	Name	Description
1	/IDE-RESET	Drive Reset
2	D0	Data bit 0
3	D2	Data bit 2
4	D4	Data bit 4
5	D6	Data bit 6
6	GND	Ground
7	D8	Data bit 8
8	D10	Data bit 10
9	D12	Data bit 12
10	D14	Data bit 14
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	+5V	5V Power

19	+5V	5V Power
20	GND	Ground
21	D1	Data bit 1
22	D3	Data bit 3
23	D5	Data bit 5
24	D7	Data bit 7
25	GND	Ground
26	D9	Data bit 9
27	D11	Data bit 11
28	D13	Data bit 13
29	D15	Data bit 15
30	/IOW	I/O Write
31	/IOR	I/O Read
32	IDE-IRQ	Interrupt Request
33	IDE-A2	Address bit 2
34	IDE-A1	Address bit 1
35	IDE-A0	Address bit 0
36	/BICS1	Chip Select 1
37	/BICS0	Chip Select 0

Contributor: [Joakim Ögren](#)

Source:

[SX-1 External IDE connector](#), Usenet posting by [Mike Pinso](#) at Paravision.

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# SCSI Information

## Background

It all started back in 1979 when the diskdrive manufacturer come with the bright idea to make a new transfer protocol. The protocol was named Shugart Associates Systems Interface, SASI. This protocol wasn't an ANSI standard, so NCR join Shugart and the ANSI committee X3T9.2 was formed. The new name for the protocol was, Small Computer Systems Interface, SCSI.

Common Command Set, CCS, was added in 1985. ANSI finished the SCSI standard in 1986. SCSI-II devices was released in 1988 and was an official standard in 1994. SCSI-III is currently not yet official.

## Usage

SCSI is used to connect peripherals to an computer. It allows you to connect harddisks, tape devices, CD-ROMs, CD-R units, DVD, scanners, printers and many other devices. SCSI is in opposite to IDE/ATA very flexible. Today SCSI is most often used servers and other computers which require very good performance. IDE/ATA is more popular due to the fact that IDE/ATA devices tend to be cheaper.

## Definitions

### SCSI

Short for Small Computer Systems Interface. The original SCSI protocol. ANSI standard X3.131-1996. Busspeed 5 MHz. Datwidth 8 bits.

### SCSI-II

SCSI-II adds support for CD-ROM's, scanners and tapedrives.

### Fast SCSI-II

Uses the busspeed of 10MHz instead of the original 5MHz.

## Wide SCSI-II

Uses 16 bits instead of the original 8 bits.

## Ultra SCSI-III

Uses the busspeed of 20MHz.

*Contributors:* [Joakim Ögren](#)

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*Document last modified:* 2001-06-07











# Apple SCSI HDI-30

## 30 PIN UNKNOWN CONNECTOR

Pin	Name	Dir	Description
1	n/c		Reserved for SCSI disk mode.
2	/DB0		Bit 0 of SCSI data bus
3	GND		Ground
4	/DB1		Bit 1 of SCSI data bus
5	TPWR		Termination power
6	/DB2		Bit 2 of SCSI data bus
7	/DB3		Bit 3 of SCSI data bus
8	GND		Ground
9	/ACKS		Handshake signal. When low acknowledges a request for data transfer
10	GND		Ground
11	/DB4		Bit 4 of SCSI data bus
12	GND		Ground
13	GND		Ground
14	/DB5		Bit 5 of SCSI data bus
15	GND		Ground
16	/DB6		Bit 6 of SCSI data bus
17	GND		Ground
18	/DB7		Bit 7 of SCSI data bus
19	/DBP		SCSI data bus parity bit
20	GND		Ground
21	/REQ		Request for a data transfer
22	GND		Ground
23	/BSY		When active (low) indicates that the SCSI data bus is busy
24	GND		Ground

25	/ATN		When active (low) indicates an attention condition
26	/C/D		When active (low) indicates that data is on the SCSI bus. When high, indicates that control signals are on the bus
27	/RST		SCSI bus reset
28	/MSG		Indicates the message phase
29	/SEL		SCSI select
30	/I/O		Controls the direction of data output. When high, data is input

*Note: Direction is Device relative Bus (other Devices).*

Contributor: [Joakim Ögren](#)

Source:  
[Apple Tech Info Library 12929: Duo Dock/Duo Dock II, External Pinouts](#) at [Apple TIL homepage](#)

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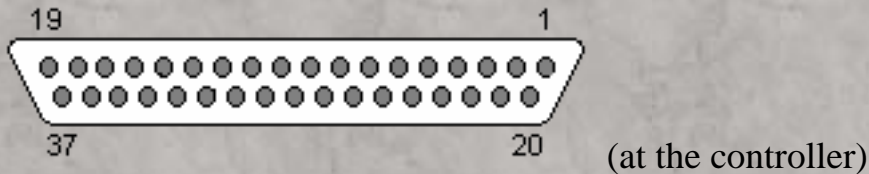
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# Novell and Procomp External SCSI

This interface is nowadays considered obsolete.



37 PIN D-SUB FEMALE at the controller.

Pin	Name	Dir	Description
1	GND	—	Ground
2	GND	—	Ground
3	GND	—	Ground
4	GND	—	Ground
5	GND	—	Ground
6	GND	—	Ground
7	GND	—	Ground
8	GND	—	Ground
9	GND	—	Ground
10	GND	—	Ground
11	GND	—	Ground
12	GND	—	Ground
13	GND	—	Ground
14	GND	—	Ground
15	GND	—	Ground
16	GND	—	Ground
17	GND	—	Ground
18	GND	—	Ground

19	TERMPWR		Termination Power
20	/DB0		Data Bus 0
21	/DB1		Data Bus 1
22	/DB2		Data Bus 2
23	/DB3		Data Bus 3
24	/DB4		Data Bus 4
25	/DB5		Data Bus 5
26	/DB6		Data Bus 6
27	/DB7		Data Bus 7
28	/DBP		Data Bus Parity
29	/ATN		Attention
30	/BSY		Busy
31	/ACK		Acknowledge
32	/RST		Reset
33	/MSG		Message
34	/SEL		Select
35	/C/D		Control/Data
36	/REQ		Request
37	/I/O		Input/Output

*Note: Direction is Device relative Bus (other Devices).*

*Contributor: [Joakim Ögren](#), [Randy Hoffman](#)*

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Black Box Corporation, FaxBack document for SCSI*

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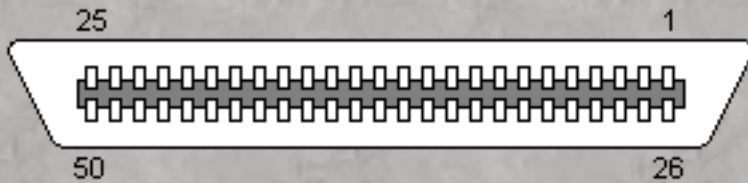
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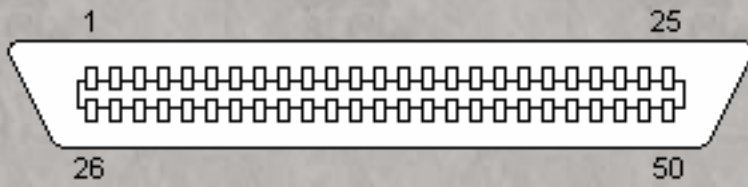




# SCSI External Centronics 50 (Differential)



(at the controller & devices)




































(at the cable)

50 PIN CENTRONICS FEMALE at the controller & devices.

50 PIN CENTRONICS MALE at the cable.

Pin	Name	Dir	Description
01	GND	—	Ground
02	+DB0	↔	+Data Bus 0
03	+DB1	↔	+Data Bus 1
04	+DB2	↔	+Data Bus 2
05	+DB3	↔	+Data Bus 3
06	+DB4	↔	+Data Bus 4
07	+DB5	↔	+Data Bus 5
08	+DB6	↔	+Data Bus 6
09	+DB7	↔	+Data Bus 7
10	+DBP	↔	+Data Bus Parity (odd Parity)
11	DIFFSENS	?	???
12	res	-	Reserved
13	TERMPWR	↔	Termination Power
14	res	-	Reserved
15	+ATN	←	+Attention

16	GND		Ground
17	+BSY		+Bus is busy
18	+ACK		+Acknowledge
19	+RST		+Reset
20	+MSG		+Message
21	+SEL		+Select
22	+C/D		+Control or Data
23	+REQ		+Request
24	+I/O		+In/Out
25	GND		Ground
26	GND		Ground
27	-DB0		-Data Bus 0
28	-DB1		-Data Bus 1
29	-DB2		-Data Bus 2
30	-DB3		-Data Bus 3
31	-DB4		-Data Bus 4
32	-DB5		-Data Bus 5
33	-DB6		-Data Bus 6
34	-DB7		-Data Bus Parity <sup>7</sup>
35	-DBP		-Data Bus Parity (odd Parity)
36	GND		Ground
37	res	-	Reserved
38	TERMPWR		Termination Power
39	res	-	Reserved
40	-ATN		-Attention
41	GND		Ground
42	-BSY		-Bus is busy
43	-ACK		-Acknowledge
44	-RST		-Reset
45	-MSG		-Message
46	-SEL		-Select
47	-C/D		-Control or Data

48	-REQ		-Request
49	-I/O		-In/Out
50	GND		Ground

*Note: Direction is Device relative Bus (other Devices).*

*Contributor: [Joakim Ögren](#), [Karsten Wenke](#)*

*Source:*

*?*

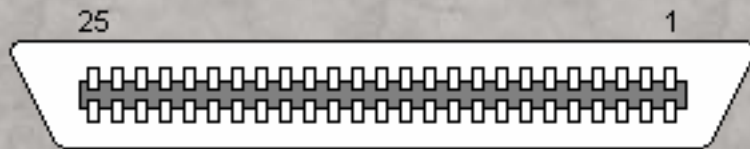
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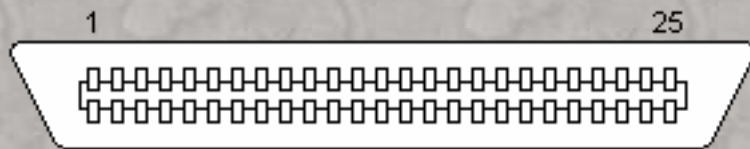
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# SCSI External Centronics 50 (Single-ended)



(at the controller & devices)














(at the cable)

50 PIN CENTRONICS FEMALE at the controller & devices.

50 PIN CENTRONICS MALE at the cable.

Pin	Name	Dir	Description
1-25	GND	—	Ground
26	DB0	↔	Data Bus 0
27	DB1	↔	Data Bus 1
28	DB2	↔	Data Bus 2
29	DB3	↔	Data Bus 3
30	DB4	↔	Data Bus 4
31	DB5	↔	Data Bus 5
32	DB6	↔	Data Bus 6
33	DB7	↔	Data Bus 7
34	PARITY	↔	Data Parity (odd Parity)
35	GND	—	Ground
36	GND	—	Ground
37	GND	—	Ground
38	TMPWR	↔	Termination Power



39	GND		Ground
40	GND		Ground
41	/ATN		Attention
42	n/c	-	Not connected
43	/BSY		Busy
44	/ACK		Acknowledge
45	/RST		Reset
46	/MSG		Message
47	/SEL		Select
48	/C/D		Control/Data
49	/REQ		Request
50	/I/O		Input/Output

*Note: Direction is Device relative Bus (other Devices).*

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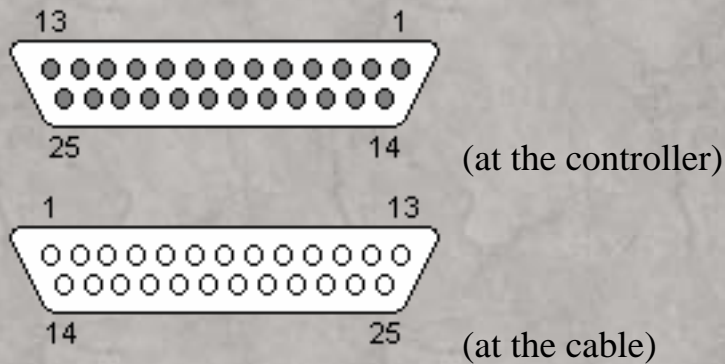
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# SCSI External D-Sub (Future Domain)












Seems to be available on some Future Domain SCSI-controllers only.



25 PIN D-SUB FEMALE at the controller.

25 PIN D-SUB MALE at the cable.

Pin	Name	Dir	Description
1	GND	—	Ground
2	DB1	↔	Data Bus 1
3	DB3	↔	Data Bus 3
4	DB5	↔	Data Bus 5
5	DB7	↔	Data Bus 7
6	GND	—	Ground
7	/SEL	↔	Select
8	GND	—	Ground
9	TMPWR	↔	Termination Power
10	/RST	↔	Reset
11	C/D	→	Control/Data
12	I/O	→	Input/Output
13	GND	—	Ground
14	DB0	↔	Data Bus 0

15	DB2		Data Bus 2
16	DB4		Data Bus 4
17	DB6		Data Bus 6
18	PARITY		Data Parity
19	GND		Ground
20	/ATN		Attention
21	/MSG		Message
22	/ACK		Acknowledge
23	BSY		Busy
24	/REQ		Request
25	GND		Ground

*Note: Direction is Device relative Bus (other Devices).*

*Contributor:* [Joakim Ögren](#)

*Source:*  
[TheRef TechTalk](#)

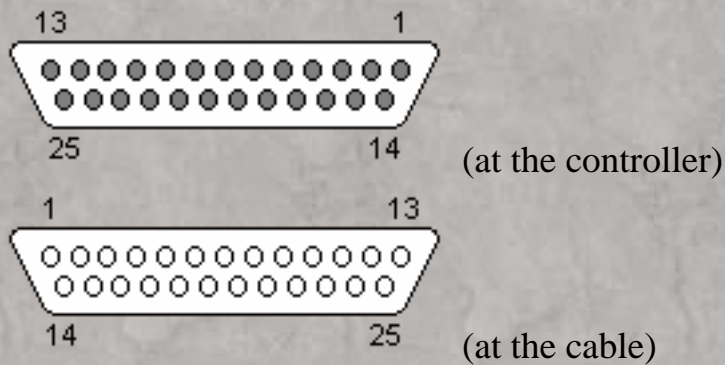
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# SCSI External D-Sub (PC/Amiga/Mac)












25 PIN D-SUB FEMALE at the controller.

25 PIN D-SUB MALE at the cable.

Pin	Name	Dir	Description
1	/REQ	→	Request
2	/MSG	→	Message
3	I/O	→	Input/Output
4	/RST	↔	Reset
5	/ACK	←	Acknowledge
6	BSY	↔	Busy
7	GND	—	Ground
8	DB0	↔	Data Bus 0
9	GND	—	Ground
10	DB3	↔	Data Bus 3
11	DB5	↔	Data Bus 5
12	DB6	↔	Data Bus 6
13	DB7	↔	Data Bus 7
14	GND	—	Ground
15	C/D	→	Control/Data
16	GND	—	Ground



17	/ATN		Attention
18	GND		Ground
19	/SEL		Select
20	PARITY		Data Parity
21	DB1		Data Bus 1
22	DB2		Data Bus 2
23	DB4		Data Bus 4
24	GND		Ground
25	TMPWR		Termination Power

*Note: Direction is Device relative Bus (other Devices).*

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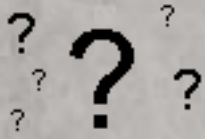
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# SCSI External IBM Burndy









Special invention by IBM for use on IBM RS/6000 and IBM PS/2




(at ???)

60 PIN BURNDY (C-60) at ???

Pin	Name	Dir	Description
1	GND	—	Ground
2	DB0	↔	Data Bus 0
3	GND	—	Ground
4	DB1	↔	Data Bus 1
5	GND	—	Ground
6	DB2	↔	Data Bus 2
7	GND	—	Ground
8	DB3	↔	Data Bus 3
9	GND	—	Ground
10	DB4	↔	Data Bus 4
11	GND	—	Ground
12	DB5	↔	Data Bus 5
13	GND	—	Ground
14	DB6	↔	Data Bus 6
15	GND	—	Ground
16	DB7	↔	Data Bus 7
17	GND	—	Ground
18	DPB	↔	Data Parity (odd Parity)

19	GND		Ground
20	GND		Ground
21	GND		Ground
22	GND		Ground
23	GND		Ground
24	GND		Ground
25	n/c		Not connected
26	TERMPWR		Termination Power
27	GND		Ground
28	GND		Ground
29	GND		Ground
30	GND		Ground
31	GND		Ground
32	/ATN		Attention
33	GND		Ground
34	GND		Ground
35	GND		Ground
36	/BSY		Busy
37	GND		Ground
38	/ACK		Acknowledge
39	GND		Ground
40	/RST		Reset
41	GND		Ground
42	/MSG		Message
43	GND		Ground
44	/SEL		Select
45	GND		Ground
46	/C/D		Control/Data
47	GND		Ground
48	/REQ		Request
49	GND		Ground
50	/I/O		Input/Output

51	GND		Ground
52	res		Reserved
53	res		Reserved
54	res		Reserved
55	res		Reserved
56	res		Reserved
57	res		Reserved
58	res		Reserved
59	res		Reserved
60	res		Reserved

*Note: Direction is Device relative Bus (other Devices).*

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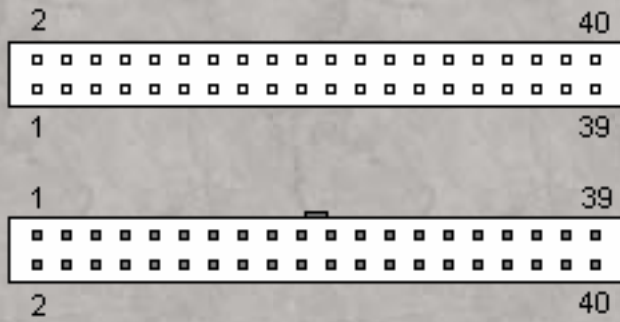
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# SCSI Internal (2.5")

This connector is for 2.5" internal harddisks.




























(at the controller & peripherals)

(at the cable)

40 PIN IDC (0.75") MALE at the controller & peripherals.

40 PIN IDC (0.75") FEMALE at the cable.

Pin	Name	Dir	Description
1	+5V	—	+5 VDC
1	+5V	—	+5 VDC
1	RET	—	Return (Ground?)
1	RET	—	Return (Ground?)
1	GND	↔	Ground
2	DB0	↔	Data Bus 0
1	GND	↔	Ground
4	DB1	↔	Data Bus 1
1	GND	↔	Ground
6	DB2	↔	Data Bus 2
1	GND	↔	Ground
8	DB3	↔	Data Bus 3
1	GND	↔	Ground
10	DB4	↔	Data Bus 4
1	GND	↔	Ground

12	DB5		Data Bus 5
1	GND		Ground
14	DB6		Data Bus 6
1	GND		Ground
16	DB7		Data Bus 7
1	GND		Ground
18	PARITY		Data Parity (odd Parity)
24	GND		Ground
26	TMPWR		Termination Power
32	/ATN		Attention
36	/BSY		Busy
24	GND		Ground
38	/ACK		Acknowledge
40	/RST		Reset
42	/MSG		Message
24	GND		Ground
44	/SEL		Select
50	/I/O		Input/Output
46	/C/D		Control/Data
24	GND		Ground
48	/REQ		Request
1	RET		Return (Ground?)
1	RET		Return (Ground?)
1	+5V		+5 VDC
1	+5V		+5 VDC

*Note: Direction is Device relative Bus (other Devices).*

Connector is: AMP 6-176135

Contributor: [Joakim Ögren](#)

Source:  
[Electrical Interface Spec for IBM DPRS-20810 and DPRS-21215](#) at [IBM Hard disk drive support](#)

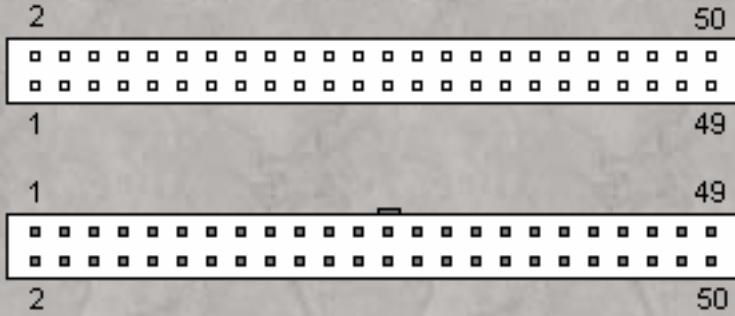
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# SCSI Internal (Differential)



(at the controller & harddisk.)




























(at the cable.)



50 PIN IDC MALE at the controller & harddisk.

50 PIN IDC FEMALE at the cable.

Pin	Name	Dir	Description
01	GND	—	Ground
02	GND	—	Ground
03	+DB0	↔	+Data Bus 0
04	-DB0	↔	-Data Bus 0
05	+DB1	↔	+Data Bus 1
06	-DB1	↔	-Data Bus 1
07	+DB2	↔	+Data Bus 2
08	-DB2	↔	-Data Bus 2
09	+DB3	↔	+Data Bus 3
10	-DB3	↔	-Data Bus 3
11	+DB4	↔	+Data Bus 4
12	-DB4	↔	-Data Bus 4
13	+DB5	↔	+Data Bus 5
14	-DB5	↔	-Data Bus 5
15	+DB6	↔	+Data Bus 6
16	-DB6	↔	-Data Bus 6



17	+DB7		+Data Bus 7
18	-DB7		-Data Bus Parity7
19	+DBP		+Data Bus Parity (odd Parity)
20	-DBP		-Data Bus Parity (odd Parity)
21	DIFFSENS	?	???
22	GND		Ground
23	res	-	Reserved
24	res	-	Reserved
25	TERMPWR		Termination Power
26	TERMPWR		Termination Power
27	res	-	Reserved
28	res	-	Reserved
29	+ATN		+Attention
30	-ATN		-Attention
31	GND		Ground
32	GND		Ground
33	+BSY		+Bus is busy
34	-BSY		-Bus is busy
35	+ACK		+Acknowledge
36	-ACK		-Acknowledge
37	+RST		+Reset
38	-RST		-Reset
39	+MSG		+Message
40	-MSG		-Message
41	+SEL		+Select
42	-SEL		-Select
43	+C/D		+Control or Data
44	-C/D		-Control or Data
45	+REQ		+Request
46	-REQ		-Request
47	+I/O		+In/Out
48	-I/O		-In/Out

49	GND		Ground
50	GND		Ground

*Note: Direction is Device relative Bus (other Devices).*

*Contributor: [Joakim Ögren](#), [Karsten Wenke](#)*

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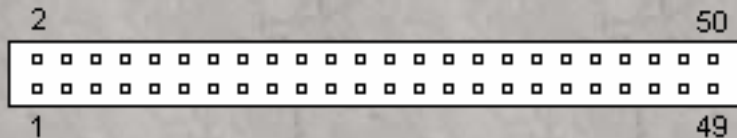
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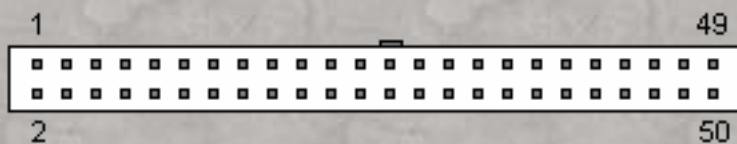
# SCSI Internal (Single-ended)

SCSI=Small Computer System Interface.

Based on an original design by Shugart Associates. SCSI was ratified in 1986.



(at the controller & harddisk)














(at the cable.)

50 PIN IDC MALE at the controller & harddisk.

50 PIN IDC FEMALE at the cable.

Pin	Name	Dir	Description
2	DB0	↔	Data Bus 0
4	DB1	↔	Data Bus 1
6	DB2	↔	Data Bus 2
8	DB3	↔	Data Bus 3
10	DB4	↔	Data Bus 4
12	DB5	↔	Data Bus 5
14	DB6	↔	Data Bus 6
16	DB7	↔	Data Bus 7
18	PARITY	↔	Data Parity (odd Parity)
20	GND	—	Ground
22	GND	—	Ground
24	GND	—	Ground
26	TMPWR	↔	Termination Power
28	GND	—	Ground

30	GND		Ground
32	/ATN		Attention
34	GND		Ground
36	/BSY		Busy
38	/ACK		Acknowledge
40	/RST		Reset
42	/MSG		Message
44	/SEL		Select
46	/C/D		Control/Data
48	/REQ		Request
50	/I/O		Input/Output

*Note: Direction is Device relative Bus (other Devices).*

*All odd-numbered pins, except pin 25, are connected to ground. Pin 25 is left open.*

*Contributor:* [Joakim Ögren](#)

*Source:*  
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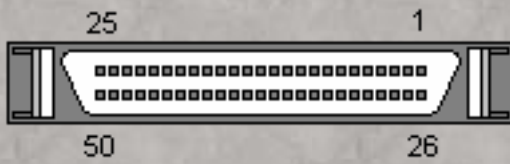
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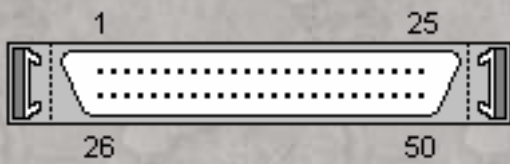




# SCSI-II External Hi D-Sub (Differential)



(at the controller & devices).



































(To the cable).

50 PIN HI-DENSITY D-SUB FEMALE at the controller & devices.

50 PIN HI-DENSITY D-SUB MALE at the cable.

Pin	Name	Dir	Description
01	GND	—	Ground
02	+DB0	↔	+Data Bus 0
03	+DB1	↔	+Data Bus 1
04	+DB2	↔	+Data Bus 2
05	+DB3	↔	+Data Bus 3
06	+DB4	↔	+Data Bus 4
07	+DB5	↔	+Data Bus 5
08	+DB6	↔	+Data Bus 6
09	+DB7	↔	+Data Bus 7
10	+DBP	↔	+Data Bus Parity (odd Parity)
11	DIFFSENS	?	???
12	res	-	Reserved
13	TERMPWR	↔	Termination Power
14	res	-	Reserved
15	+ATN	←	+Attention
16	GND	—	Ground

17	+BSY		+Bus is busy
18	+ACK		+Acknowledge
19	+RST		+Reset
20	+MSG		+Message
21	+SEL		+Select
22	+C/D		+Control or Data
23	+REQ		+Request
24	+I/O		+In/Out
25	GND		Ground
26	GND		Ground
27	-DB0		-Data Bus 0
28	-DB1		-Data Bus 1
29	-DB2		-Data Bus 2
30	-DB3		-Data Bus 3
31	-DB4		-Data Bus 4
32	-DB5		-Data Bus 5
33	-DB6		-Data Bus 6
34	-DB7		-Data Bus Parity <sup>7</sup>
35	-DBP		-Data Bus Parity (odd Parity)
36	GND		Ground
37	res	-	Reserved
38	TERMPWR		Termination Power
39	res	-	Reserved
40	-ATN		-Attention
41	GND		Ground
42	-BSY		-Bus is busy
43	-ACK		-Acknowledge
44	-RST		-Reset
45	-MSG		-Message
46	-SEL		-Select
47	-C/D		-Control or Data
48	-REQ		-Request

49	-I/O		-In/Out
50	GND		Ground

*Note: Direction is Device relative Bus (other Devices).*

*Contributor: [Joakim Ögren](#), [Karsten Wenke](#)*

*Source:*  
*?*

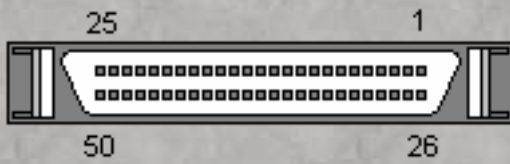
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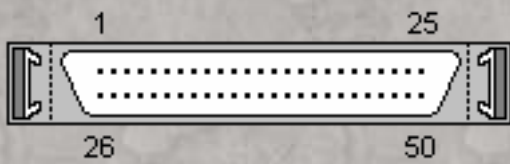
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# SCSI-II External Hi D-Sub (Single-ended)



(at the controller & devices).












(To the cable).

50 PIN HI-DENSITY D-SUB FEMALE at the controller & devices.

50 PIN HI-DENSITY D-SUB MALE at the cable.

Pin	Name	Dir	Description
1-25	GND	—	Ground
26	DB0	↔	Data Bus 0
27	DB1	↔	Data Bus 1
28	DB2	↔	Data Bus 2
29	DB3	↔	Data Bus 3
30	DB4	↔	Data Bus 4
31	DB5	↔	Data Bus 5
32	DB6	↔	Data Bus 6
33	DB7	↔	Data Bus 7
34	PARITY	↔	Data Parity (odd Parity)
35	GND	—	Ground
36	GND	—	Ground
37	GND	—	Ground
38	TMPWR	↔	Termination Power
39	GND	—	Ground
40	GND	—	Ground



41	/ATN		Attention
42	n/c	-	Not connected
43	/BSY		Busy
44	/ACK		Acknowledge
45	/RST		Reset
46	/MSG		Message
47	/SEL		Select
48	/C/D		Control/Data
49	/REQ		Request
50	/I/O		Input/Output

*Note: Direction is Device relative Bus (other Devices).*

*Contributor: [Joakim Ögren](#)*

*Source:  
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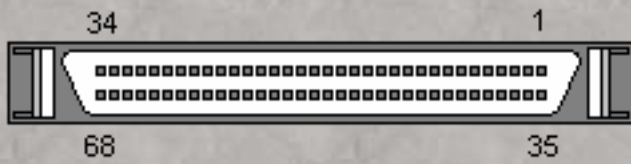
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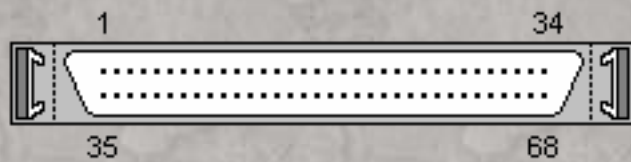
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# SCSI-III External Hi D-Sub (Differential)



(at the controller & devices).























































(To the cable).

68 PIN HI-DENSITY D-SUB FEMALE at the controller & devices.

68 PIN HI-DENSITY D-SUB MALE at the cable.

Pin	Name	Dir	Description
1	+DB12	↔	Data Bus 12
2	+DB13	↔	Data Bus 13
3	+DB14	↔	Data Bus 14
4	+DB15	↔	Data Bus 15
5	+DPB1	↔	Data Parity (odd Parity)
6	GND	—	Ground
7	+DB0	↔	Data Bus 0
8	+DB1	↔	Data Bus 1
9	+DB2	↔	Data Bus 2
10	+DB3	↔	Data Bus 3
11	+DB4	↔	Data Bus 4
12	+DB5	↔	Data Bus 5
13	+DB6	↔	Data Bus 6
14	+DB7	↔	Data Bus 7
15	+DPB	↔	Data Parity (odd Parity)
16	DIFFSENSE	?	Diff Sense?

17	TERMPWR		Termination Power
18	TERMPWR		Termination Power
19	res		reserved
20	+ATN		Attention
21	GND		Ground
22	+BSY		Busy
23	+ACK		Acknowledge
24	+RST		Reset
25	+MSG		Message
26	+SEL		Select
27	+C/D		Control/Data
28	+REQ		Request
29	+I/O		Input/Output
30	GND		Ground
31	+DB8		Data Bus 8
32	+DB9		Data Bus 9
33	+DB10		Data Bus 10
34	+DB11		Data Bus 11
35	-DB12		Data Bus 12
36	-DB13		Data Bus 13
37	-DB14		Data Bus 14
38	-DB15		Data Bus 15
39	-DPB1		Data Parity (odd Parity)
40	GND		Ground
41	-DB0		Data Bus 0
42	-DB1		Data Bus 1
43	-DB2		Data Bus 2
44	-DB3		Data Bus 3
45	-DB4		Data Bus 4
46	-DB5		Data Bus 5
47	-DB6		Data Bus 6
48	-DB7		Data Bus 7

49	-DPB		Data Parity (odd Parity)
50	GND		Ground
51	TERMPWR		Termination Power
52	TERMPWR		Termination Power
53	res		reserved
54	-ATN		Attention
55	GND		Ground
56	-BSY		Busy
57	-ACK		Acknowledge
58	-RST		Reset
59	-MSG		Message
60	-SEL		Select
61	-C/D		Control/Data
62	-REQ		Request
63	-I/O		Input/Output
64	GND		Ground
65	-DB8		Data Bus 8
66	-DB9		Data Bus 9
67	-DB10		Data Bus 10
68	-DB11		Data Bus 11

*Note: Direction is Device relative Bus (other Devices).*

Contributor: [Joakim Ögren](#)

Source:

[SCSI 68 Pin Differential pinout](#) at [The Pin-Out directory](#)

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
















# SCSI-III External Hi D-Sub (Differential)























SCA=Single Connector Attachment

Drive connector: AMP Champ 557613-1 or AMP Champ 557114-5

Cable connector: AMP Champ 2-557103-1 or AMP Champ 2-557101-1

Pin	Name	Dir	Description
1	12V		+12 VDC
2	12V		+12 VDC
3	12V		+12 VDC
4	12V		+12 VDC
5	3.3V		+3.3 VDC
6	3.3V		+3.3 VDC
7	-DB(11)		Data Bus 11
8	-DB(10)		Data Bus 10
9	-DB(9)		Data Bus 9
10	-DB(8)		Data Bus 8
11	-I/O		Input/Output
12	-REQ		Request
13	-C/D		Control/Data
14	-SEL		Select
15	-MSG		Message
16	-RST		Reset
17	-ACK		Acknowledge
18	-BSY		Busy
19	-ATN		Attention
20	-P_CRCA	?	
21	-DB(7)		Data Bus 7

22	-DB(6)		Data Bus 6
23	-DB(5)		Data Bus 5
24	-DB(4)		Data Bus 4
25	-DB(3)		Data Bus 3
26	-DB(2)		Data Bus 2
27	-DB(1)		Data Bus 1
28	-DB(0)		Data Bus 0
29	-DB(P1)	?	
30	-DB(15)		Data Bus 15
31	-DB(14)		Data Bus 14
32	-DB(13)		Data Bus 13
33	-DB(12)		Data Bus 12
34	5V		Ground (Signal)
35	5V		Ground (Signal)
36	5V CHARGE		Ground (Signal)
37	SPINDLE SYNC	?	Spindle Sync
38	RMT_START	?	Remote Start
39	SCSI ID (0)		SCSI ID Bit 0
40	SCSI ID (2)		SCSI ID Bit 2
41	12V GROUND		+12 VDC Ground
42	12V GROUND		+12 VDC Ground
43	12V GROUND		+12 VDC Ground
44	MATED 1	?	
45	3.3V CHARGE		+3.3 VDC Charge
46	DIFFSNS		Differential Sense
47	+DB(11)		Data Bus 11
48	+DB(10)		Data Bus 10
49	+DB(9)		Data Bus 9
50	+DB(8)		Data Bus 8
51	+I/O		Input/Output
52	+REQ		Request
53	+C/D		Control/Data

54	+SEL		Select
55	+MSG		Message
56	+RST		Reset
57	+ACK		Acknowledge
58	+BSY		Busy
59	+ATN		Attention
60	+P_CRCA	?	
61	+DB(7)		Data Bus 7
62	+DB(6)		Data Bus 6
63	+DB(5)		Data Bus 5
64	+DB(4)		Data Bus 4
65	+DB(3)		Data Bus 3
66	+DB(2)		Data Bus 2
67	+DB(1)		Data Bus 1
68	+DB(0)		Data Bus 0
69	+DB(P1)	?	
70	+DB(15)		Data Bus 15
71	+DB(14)		Data Bus 14
72	+DB(13)		Data Bus 13
73	+DB(12)		Data Bus 12
74	MATED 2	?	
75	5V GROUND		+5 VDC Ground
76	5V GROUND		+5 VDC Ground
77	ACTIVE LED OUT	?	
78	DLYD_START	?	
79	SCSI ID (1)		SCSI ID Bit 1
80	SCSI ID (3)		SCSI ID Bit 3

5: RESERVED/NC 6: RESERVED/NC 20: -DB(P0) 36: 5 VOLT 44: 12 V GROUND 45: RESERVED/NC 46: RESERVED/NC 74: 5 V GROUND

*Note: Direction is Device relative Bus (other Devices).*

*Contributor:* [Joakim Ögren](#)

*Source:*

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
















# SCSI-III External Hi D-Sub (Single-ended)

























SCA=Single Connector Attachment

Drive connector: AMP Champ 557613-1 or AMP Champ 557114-5

Cable connector: AMP Champ 2-557103-1 or AMP Champ 2-557101-1

Pin	Name	Dir	Description
1	12V		+12 VDC
2	12V		+12 VDC
3	12V		+12 VDC
4	12V		+12 VDC
5	3.3V		+3.3 VDC
6	3.3V		+3.3 VDC
7	-DB(11)		Data Bus 11
8	-DB(10)		Data Bus 10
9	-DB(9)		Data Bus 9
10	-DB(8)		Data Bus 8
11	-I/O		Input/Output
12	-REQ		Request
13	-C/D		Control/Data
14	-SEL		Select
15	-MSG		Message
16	-RST		Reset
17	-ACK		Acknowledge
18	-BSY		Busy
19	-ATN		Attention
20	-P_CRCA	?	
21	-DB(7)		Data Bus 7

22	-DB(6)		Data Bus 6
23	-DB(5)		Data Bus 5
24	-DB(4)		Data Bus 4
25	-DB(3)		Data Bus 3
26	-DB(2)		Data Bus 2
27	-DB(1)		Data Bus 1
28	-DB(0)		Data Bus 0
29	-DB(P1)	?	
30	-DB(15)		Data Bus 15
31	-DB(14)		Data Bus 14
32	-DB(13)		Data Bus 13
33	-DB(12)		Data Bus 12
34	5V		Ground (Signal)
35	5V		Ground (Signal)
36	5V CHARGE		Ground (Signal)
37	SPINDLE SYNC	?	Spindle Sync
38	RMT_START	?	Remote Start
39	SCSI ID (0)		SCSI ID Bit 0
40	SCSI ID (2)		SCSI ID Bit 2
41	12V GROUND		+12 VDC Ground
42	12V GROUND		+12 VDC Ground
43	12V GROUND		+12 VDC Ground
44	MATED 1	?	
45	3.3V CHARGE		+3.3 VDC Charge
46	GROUND		Ground
47	SIGNAL RETURN		Ground (Signal)
48	SIGNAL RETURN		Ground (Signal)
49	SIGNAL RETURN		Ground (Signal)
50	SIGNAL RETURN		Ground (Signal)
51	SIGNAL RETURN		Ground (Signal)
52	SIGNAL RETURN		Ground (Signal)
53	SIGNAL RETURN		Ground (Signal)

54	SIGNAL RETURN		Ground (Signal)
55	SIGNAL RETURN		Ground (Signal)
56	SIGNAL RETURN		Ground (Signal)
57	SIGNAL RETURN		Ground (Signal)
58	SIGNAL RETURN		Ground (Signal)
59	SIGNAL RETURN		Ground (Signal)
60	SIGNAL RETURN		Ground (Signal)
61	SIGNAL RETURN		Ground (Signal)
62	SIGNAL RETURN		Ground (Signal)
63	SIGNAL RETURN		Ground (Signal)
64	SIGNAL RETURN		Ground (Signal)
65	SIGNAL RETURN		Ground (Signal)
66	SIGNAL RETURN		Ground (Signal)
67	SIGNAL RETURN		Ground (Signal)
68	SIGNAL RETURN		Ground (Signal)
69	SIGNAL RETURN		Ground (Signal)
70	SIGNAL RETURN		Ground (Signal)
71	SIGNAL RETURN		Ground (Signal)
72	SIGNAL RETURN		Ground (Signal)
73	SIGNAL RETURN		Ground (Signal)
74	MATED 2	?	
75	5V GROUND		+5 VDC Ground
76	5V GROUND		+5 VDC Ground
77	ACTIVE LED OUT	?	
78	DLYD_START	?	
79	SCSI ID (1)		SCSI ID Bit 1
80	SCSI ID (3)		SCSI ID Bit 3

5: RESERVED/NC 6: RESERVED/NC 20: -DB(P0) 36: 5 VOLT 44: 12 V GROUND 45: RESERVED/NC 46: RESERVED/NC 74: 5 V GROUND

*Note: Direction is Device relative Bus (other Devices).*

*Contributor:* [Joakim Ögren](#)

*Source:*

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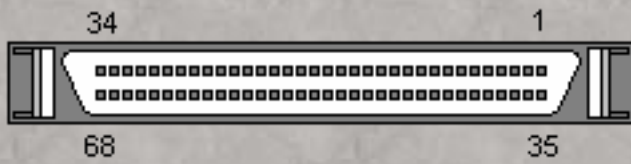
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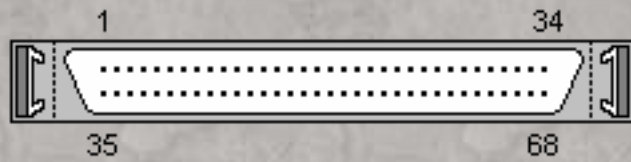




# SCSI-III External Hi D-Sub (Single-ended)



(at the controller & devices).


























(To the cable).

68 PIN HI-DENSITY D-SUB FEMALE at the controller & devices.

68 PIN HI-DENSITY D-SUB MALE at the cable.

Pin	Name	Dir	Description
1-16	GND	—	Ground
17	TERMPWR	↔	Termination Power
18	TERMPWR	↔	Termination Power
19	res	↔	reserved
20-34	GND	—	Ground
35	DB12	↔	Data Bus 12
36	DB13	↔	Data Bus 13
37	DB14	↔	Data Bus 14
38	DB15	↔	Data Bus 15
39	DPB1	↔	Data Parity (odd Parity)
40	DB0	↔	Data Bus 0
41	DB1	↔	Data Bus 1
42	DB2	↔	Data Bus 2
43	DB3	↔	Data Bus 3
44	DB4	↔	Data Bus 4
45	DB5	↔	Data Bus 5

46	DB6		Data Bus 6
47	DB7		Data Bus 7
48	DPB		Data Parity (odd Parity)
49	GND		Ground
50	GND		Ground
51	TERMPWR		Termination Power
52	TERMPWR		Termination Power
53	res		reserved
54	GND		Ground
55	/ATN		Attention
56	GND		Ground
57	/BSY		Busy
58	/ACK		Acknowledge
59	/RST		Reset
60	/MSG		Message
61	/SEL		Select
62	/C/D		Control/Data
63	/REQ		Request
64	/I/O		Input/Output
65	DB8		Data Bus 8
66	DB9		Data Bus 9
67	DB10		Data Bus 10
68	DB11		Data Bus 11

*Note: Direction is Device relative Bus (other Devices).*

Contributor: [Joakim Ögren](#)

Source:

[SCSI FAQ](#)

[SCSI 68 Pin Normal pinout](#) at [The Pin-Out directory](#)

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# Adaptec RAIDport

## 60 PIN UNKNOWN CONNECTOR

Pin	Description
Pin	Signal
B01	n/c
B02	n/c
B03	Ground
B04	n/c
B05	REQ[A]#
B06	RSVD
B07	REQ[B]#
B08	REQ[C]#
B09	LED[A]#
B10	n/c
B11	n/c
B12	RSVD
B13	CLK40
B14	Ground
B15	MRW
B16	MD[0]
B17	MD[2]
B18	MD[4]
B19	Ground
B20	MD[6]
B21	MA[14]
B22	MA[12]
B23	MA[10]

B24	MA[8]
B25	PRSNT1
B26	MA[6]
B27	MA[4]
B28	Ground
B29	MA[2]
B30	MA[0]
A01	n/c
A02	n/c
A03	n/c
A04	n/c
A05	ACK[A]#
A06	RSVD
A07	ACK[B]#
A08	ACK[C]#
A09	IDDAT
A10	n/c
A11	n/c
A12	SY_RST#
A13	ROMCS[A]#
A14	RAMCS#
A15	Ground
A16	MDP
A17	MD[1]
A18	RAMPS#
A19	MD[3]
A20	MD[5]
A21	MA[13]
A22	MD[7]
A23	MA[11]
A24	MA[9]
A25	MA[7]



A26	Ground
A27	MA[5]
A28	MA[3]
A29	SEECs[A]
A30	MA[1]

*Contributor:* [Joakim Ögren](#)

*Source:*  
?

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*Document last modified:* 2000-07-07



# IEEE488

## 12 PIN UNKNOWN CONNECTOR at the Computer

1	2	3	4	5	6	
=	=	=	=	=	=	
#####	#####	#####	#####	#####	#####	(At the computer)
=	=	=	=	=	=	
A	B	C	D	E	F	

Pin	Description
A or 1	GND
B or 2	+5v
C or 3	Motor (computer controlled +6v for datasette motor)
D or 4	Read line from cassette
E or 5	Write line cassette
F or 6	Cassette Switch Sense (monitors cassette play/ff/rew buttons)

Contributor: [Joakim Ögren](#)

Source:

[Commodore PET FAQ](#)

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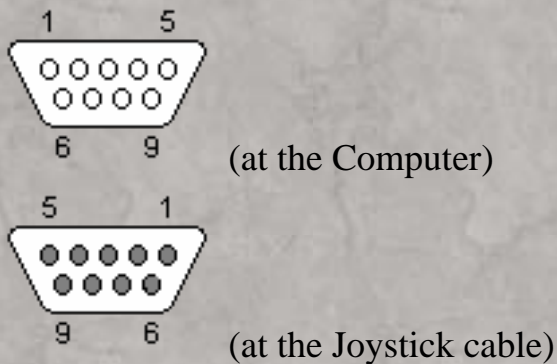
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Document last modified: 2000-07-07



# Amstrad Digital Joystick

Available at the Amstrad CPC6128 and CPC6128 Plus.




9 PIN D-SUB MALE at the Computer.

9 PIN D-SUB FEMALE at the Joystick cable.

## Digital Joystick 1

Pin	Name	Dir	Description
1	UP		Up
2	DOWN		Down
3	LEFT		Left
4	RIGHT		Right
5	n/c	-	Not connected
6	FIRE2		Fire button 2
7	FIRE1		Fire button 1
8	GND		Ground
9	GND		Ground

## Digital Joystick 2

Pin	Name	Dir	Description
1	UP		Up
2	DOWN		Down
3	LEFT		Left
4	RIGHT		Right
5	n/c	-	Not connected
6	FIRE2		Fire button 2
7	FIRE1		Fire button 1
8	GND		Ground
9	n/c	-	Not connected

*Note: Direction is Computer relative Joystick.*

*Contributor: [Joakim Ögren](#), [Colin Gaunt](#), [Agnello Guarracino](#)*

*Source:*

*Amstrad 6128 Plus Home Computer Manual*

*Amstrad CPC6128 User Instructions Manual*

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*Document last modified: 2001-06-07*





# Apple IIc Joystick

## 9 PIN UNKNOWN CONNECTOR

Pin	Name	Description
1	GAMESW1	Switch input 1 (sometimes called paddle button 1).
2	+5V	+5 VDC (max 100mA)
3	GND	System ground.
4	n/a	Not used
5	PDL0	Paddle 0 hand controller input. Must be connected to a 150K ohm variable resistor connected to +5V.
6	n/c	Not connected
7	GAMESW0	Switch input 0 (sometimes called paddle button 0).
8	PDL1	Paddle 1 hand controller input; must be connected to a 150K ohm variable resistor connected to +5V.
9	n/a	Not used

Contributor: [Joakim Ögren](#)

Source:

[Apple Tech Info Library 1419: Apple IIc, External Pinouts](#) at [Apple TIL homepage](#)

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Document last modified: 2000-07-09



# Atari 2600 Controller Pinouts

A lot of different controllers was available for the Atari 2600 VCS system.

## Sticks

Pin	Description
1	Up
2	Down
3	Left
4	Right
5	NC
6	Fire
7	NC
8	Ground
9	NC

## Paddles

Pin	Description
1	NC
2	NC
3	2P Fire
4	1P Fire
5	NC
6	NC
7	+5v (pot common)
8	Ground

9	2P Paddle
---	-----------

## Omega Race Controller

Pin	Description
1	Up thru
2	Down thru
3	Left thru
4	Right thru
5	Front trigger
6	Fire thru
7	+5v (triggers)
8	Ground
9	Top trigger

## Kids Controller (Touch Pad)

Pin #	5	9	6
1	1	2	3
2	4	5	6
3	7	8	9
4	*	0	#
7	+5v pulls pins 5 & 9 through 4.7k resistors		

Contributor: [Joakim Ögren](#)

Source:

[Atari 2600 Controllers](#) at [GamesX](#)  
[Jay Tilton's web site](#)

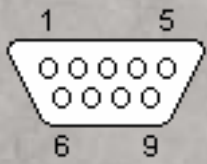
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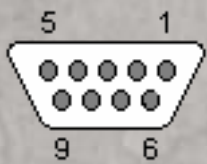
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# Atari 2600 Joystick



(at the Atari)



(at the joystick cable)

9 PIN D-SUB MALE at the Atari.

9 PIN D-SUB FEMALE at the joystick cable.

Pin	Color	Dir	Description
1	WHT	←	Up
2	BLU	↓	Down
3	GRN	←	Left
4	BRN	→	Right
5	n/c	-	Not connected
6	ORG	←	Button
7	n/c	-	Not connected
8	BLK	—	Ground(-)
9	n/c	-	Not connected

*Note: Direction is Computer relative Joystick.*

*Note: Connect Direction/Button to Ground for action.*

Contributor: [Joakim Ögren](#)

Source:

Classic Atari 2600/5200/7800 Game Systems FAQ - Pinout by [Greg Alt](#)



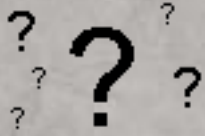
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# Atari 5200 Joystick



(at the Atari)

UNKNOWN CONNECTOR at the Atari.

Pin	Description
1	Keypad -- right column
2	Keypad -- middle column
3	Keypad -- left column
4	Start, Pause, and Reset common
5	Keypad -- third row and Reset
6	Keypad -- second row and Pause
7	Keypad -- top row and Start
8	Keypad -- bottom row
9	Pot common
10	Horizontal pot (POT0, 2, 4, 6)
11	Vertical pot (POT1, 3, 5, 7)
12	5 volts DC
13	Bottom side buttons (TRIG0, 1, 2, 3)
14	Top side buttons
15	0 volts -- ground

Contributor: [Joakim Ögren](#), [Eric Parent](#)

Source:  
*Classic Atari 2600/5200/7800 Game Systems FAQ*

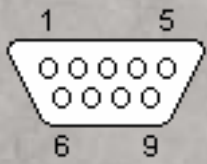
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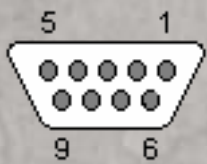
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# Atari 7800 Joystick



(at the Atari)



(at the joystick cable)

9 PIN D-SUB MALE at the Atari.

9 PIN D-SUB FEMALE at the joystick cable.

Pin	Color	Dir	Description
1	WHT	←	Up
2	BLU	←	Down
3	GRN	←	Left
4	BRN	←	Right
5	RED	←	Button (R)ight (-)
6	ORG	?	Both buttons (+)
7	n/c	-	Not connected
8	BLK	—	Ground(-)
9	YLW	←	Button (L)eft (-)

*Note: Direction is Computer relative Joystick.*

*Note: Connect Direction and Button(L/R) to Ground for action. And Both Button to Button L and Button R for action.*

Contributor: [Joakim Ögren](#)

Source:  
*Classic Atari 2600/5200/7800 Game Systems FAQ*



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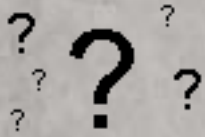
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# Atari Enhanced Joystick

Can be found at Atari Falcon, Jaguar & STe.



(at the computer)

UNKNOWN CONNECTOR at the computer.

Pin	Name	Description
1	UP0	Up 0
2	DOWN0	Down 0
3	LEFT0	Left 0
4	RIGHT0	Right 0
5	PAD0Y	Paddle 0 Y
6	FIRE0/LIGHT GUN	Fire 0/Lightgun
7	VCC	+5 VDC
8	n/c	Not connected
9	GND	Ground
10	FIRE2	Fire 2
11	UP2	Up 2
12	DOWN2	Down 2
13	LEFT2	Left 2
14	RIGHT2	Right 2
15	PAD0X	Paddle 0 X

Contributor: [Joakim Ögren](#)

Source:

*Do-It-Yourself Atari Jaguar Controller by [Andrew Hague](#)*

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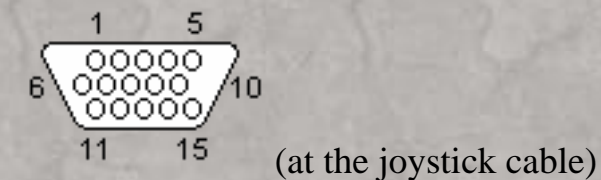
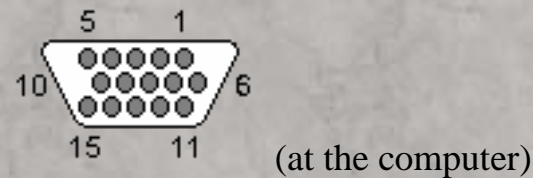
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# Atari Enhanced Joystick

Can be found at Atari Falcon, Jaguar & STe.



15 PIN HIGHDENSITY D-SUB FEMALE at the computer.

15 PIN HIGHDENSITY D-SUB MALE at the joystick cable.

Pin	Name	Description
1	UP0	Up 0
2	DOWN0	Down 0
3	LEFT0	Left 0
4	RIGHT0	Right 0
5	PAD0Y	Paddle 0 Y
6	FIRE0/LIGHT GUN	Fire 0/Lightgun
7	VCC	+5 VDC
8	n/c	Not connected
9	GND	Ground
10	FIRE2	Fire 2
11	UP2	Up 2
12	DOWN2	Down 2
13	LEFT2	Left 2
14	RIGHT2	Right 2



15 PAD0X

Paddle 0 X

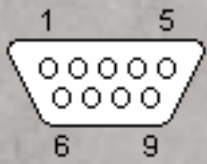
*Contributor:* [Joakim Ögren](#)

*Source:*  
*Atari Enhanced Joystick Ports FAQ*

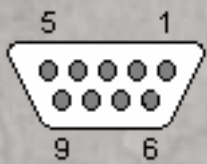
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# Atari Mouse/Joy



(at the computer)



(at the mouse/joy cable)

9 PIN D-SUB MALE at the computer.

9 PIN D-SUB FEMALE at the mouse/joy cable.

Pin	Mouse	Joystick	Dir	Comment
1	XB	UP	←	
2	XA	DOWN	←	
3	YA	LEFT	←	
4	YB	RIGHT	←	
5	n/c	n/c	-	
6	LEFTBUTTON	FIRE	←	
7	+5V	+5V	→	
8	GND	GND	—	
9	RIGHTBUTTON	res	←	

*Note: Direction is Computer relative Device.*

Contributor: [Joakim Ögren](#), [Steve & Sally Blair](#)

Source:  
?

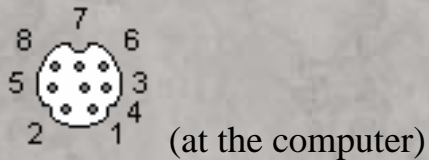
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# C16/C116/+4 Joystick

Available on the Commodore C16, C116 and +4 computers.



8 PIN MINI-DIN FEMALE at the computer.



## Joystick 1

Pin	Name	Dir	Comment
1	JOYA0	←	
2	JOYA1	←	
3	JOYA2	←	
4	JOYA3	←	
5	+5VDC	→	
6	BUTTON A	?	
7	GND	—	
8	COMMON A ?	?	Is connected to DATA2 thru a buffer.

## Joystick 2

Pin	Name	Dir	Comment
1	JOYB0	←	
2	JOYB1	←	
3	JOYB2	←	
4	JOYB3	←	



5	+5VDC		
6	BUTTON B	?	
7	GND		
8	COMMON B ?	?	Is connected to DATA1 thru a buffer.

*Note: Direction is Computer relative Device.*

*Contributor: [Joakim Ögren](#), [Arwin Vosselman](#)*

*Source:  
SAMS Computerfacts CC8 Commodore 16.*

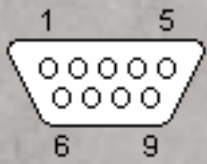
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# C64 Control Port



(at the computer)



(at the joystick cable)

9 PIN D-SUB MALE at the computer.









9 PIN D-SUB FEMALE at the joystick cable.

## Control Port 1

Pin	Name	Dir	Comment
1	JOYA0	←	
2	JOYA1	←	
3	JOYA2	←	
4	JOYA4	←	
5	POT AY	↔	
6	BUTTON A/LP	↔	
7	+5V	→	50 mA max
8	GND	—	
9	POT AX	↔	

## Control Port 2

Pin	Name	Dir	Comment
1	JOYB0	←	

2	JOYB1		
3	JOYB2		
4	JOYB4		
5	POT BY		
6	BUTTON B		
7	+5V		50 mA max
8	GND		
9	POT BX		

*Note: Direction is Computer relative Device.*

*Note: Pot is a linear 470 kOhm ( $\pm 10\%$ )*

*Contributor: [Joakim Ögren](#), [Arwin Vosselman](#)*

*Sources:*

*Amiga 4000 User's Guide from Commodore*

*Commodore 64 Programmer's Reference Guide*

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# MSX Joystick



(at the computer)



(at the joystick cable)

9 PIN D-SUB MALE at the computer.  
9 PIN D-SUB FEMALE at the joystick cable.

Pin	Name	Dir	Description
1	/FORWARD	←	Forward
2	/BACK	←	Backward
3	/LEFT	←	Left
4	/RIGHT	←	Right
5	+5V	→	+5 VDC (50mA max)
6	/TRG1	↔	Trigger A / Output 1
7	/TRG2	↔	Trigger A / Output 1
8	OUTPUT	→	Output 3
9	GND	—	Signal Ground

*Note: Direction is Computer relative Joystick.*

*Warning: Pin 5 is +5V on MSX and Mouse Button 2 on Amiga. Since Amiga mousebutton is active low, connecting an Amiga mouse to a MSX and pressing mousebutton 2 will shortcut the supply voltage.*

Contributor: [Joakim Ögren](#)

Source:



*Mayer's SV738 X'press I/O map*

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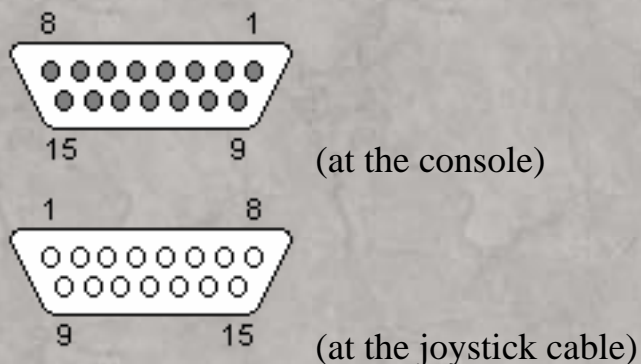
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# NeoGeo Joystick

Available on the NeoGeo videogame.



15 PIN D-SUB FEMALE at the console.

15 PIN D-SUB MALE at the joystick cable.

Pin	Name	Dir	Description
1	GND		Ground
2	n/c	-	Not connected
3	SELECT		Select Button
4	BUTTOND		"D" Button
5	BUTTONB		"B" Button
6	RIGHT		Right
7	DOWN		Down
8	n/c	-	Not connected
9	BUTTOND		"D" Button, again?
10	n/c	-	Not connected
11	START		Start Button
12	BUTTONC		"C" Button
13	BUTTONA		"A" Button
14	LEFT		Left



*Note: Direction is Computer relative Joystick.*

*Note: Signals are active high (connect to +5V).*

*Contributor: [Joakim Ögren](#), [Enzo](#)*

*Source:*

*[NeoGeo Controller pinout](#) at [GamesX](#)*

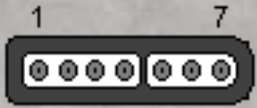
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# Nintendo SNES Controller



(at the Console)

7 PIN SNES SPECIAL FEMALE at the Console.

Pin	Description	Wire Color
1	+5v	White
2	Data Clock	Yellow
3	Data Latch	Orange
4	Serial Data	Red
5	N/C	-
6	N/C	-
7	Ground	Brown

Contributor: [Joakim Ögren](#), [Jim Christy](#)

Source:  
[SNES / Super Famicom Joystick Data](#) at [GamesX](#)

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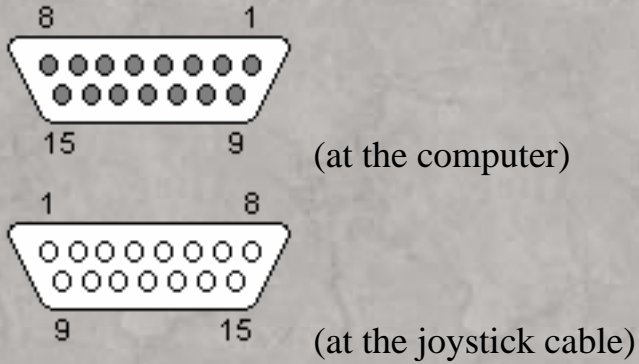
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# PC Gameport



15 PIN D-SUB FEMALE at the computer.

15 PIN D-SUB MALE at the joystick cable.

Pin	Name	Dir	Description
1	+5V	→	+5 VDC
2	/B1	←	Button 1
3	X1	←	Joystick 1 - X
4	GND	—	Ground
5	GND	—	Ground
6	Y1	←	Joystick 1 - Y
7	/B2	←	Button 2
8	+5V	→	+5 VDC
9	+5V	→	+5 VDC
10	/B4	←	Button 4
11	X2	←	Joystick 2 - X
12	GND	—	Ground
13	Y2	←	Joystick 2 - Y
14	/B3	←	Button 3
15	+5V	→	+5 VDC

*Note: Direction is Computer relative Joystick.*

*Note: Use 100kohm resistor.*

*Contributor: [Joakim Ögren](#)*

*Source:*

*?*

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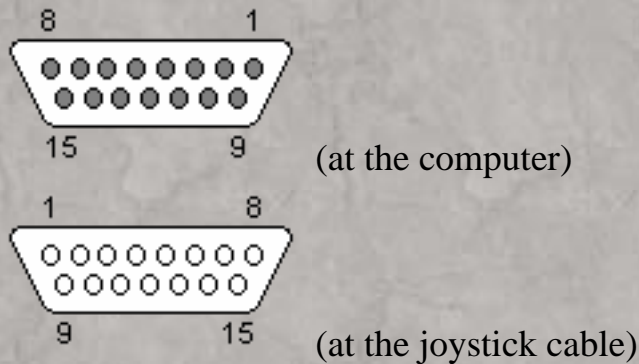
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*Document last modified: 2001-06-07*



# PC Gameport+MIDI

Some soundcards have some MIDI signals included in their Gameport. Ground and VCC has been used for this.



15 PIN D-SUB FEMALE at the computer.  
15 PIN D-SUB MALE at the joystick cable.

Pin	Name	Dir	Description
1	+5V	→	+5 VDC
2	/B1	←	Button 1
3	X1	←	Joystick 1 - X
4	GND	—	Ground
5	GND	—	Ground
6	Y1	←	Joystick 1 - Y
7	/B2	←	Button 2
8	+5V	→	+5 VDC
9	+5V	→	+5 VDC
10	/B4	←	Button 4
11	X2	←	Joystick 2 - X
12	MIDITXD	→	MIDI Transmit
13	Y2	←	Joystick 2 - Y
14	/B3	←	Button 3

15	MIDIRXD		MIDI Receive
----	---------	--	--------------

*Note: Direction is Computer relative Joystick.*

*Note: Use 100 kohm resistor.*

*Contributor: [Joakim Ögren](#)*

*Source:*

*?*

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*Document last modified: 2001-06-07*





# Sega Genesis Controller

9 PIN DSUB ??

Pin	Name (Select=GND)	Name (Select=+5V)
1	Up	Up
2	Down	Down
3	Gnd / Left	
4	Gnd / Right	
5	+5VDC	+5VDC
6	Button A	Button B
7	Select	Select
8	Ground	Ground
9	Start	Button C

The chip inside the controller is a 74HC157. This is a high-speed cmos quad 2-line to 1-line multiplexer. The console can with help of the Select-pin choose from two functions on each input.

Contributor: [Joakim Ögren](#), [Neal Patrick Howland](#)

Source:

[SEGA Genesis A/V pinout](#) at [GamesX](#)

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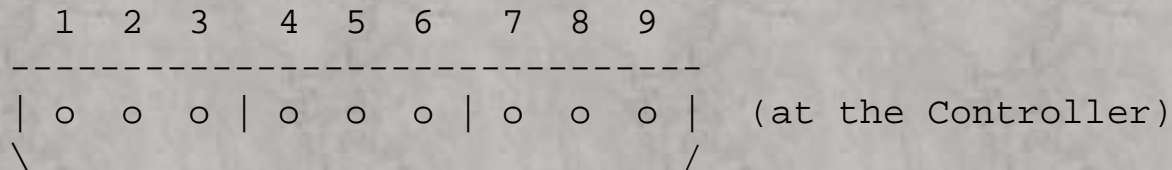
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Document last modified: 2000-07-09



# Sony Playstation Controller Port

## 9 PIN UNKNOWN CONNECTOR



Pin	Name	Description
1	DATA	Data
2	CMD	Command
3	N/C (9 V unused)	Not connected
4	GND	Ground
5	VCC	Vcc
6	ATT	ATT select
7	CLK	Clock
8	N/C	Not connected
9	ACK	Acknowledge

## Signals description:

### DATA

Signal from Controller to PSX. This signal is an 8 bit serial transmission synchronous to the falling edge of clock (That is both the incoming and outgoing signals change on a high to low transition of clock. All the reading of signals is done on the leading edge to allow settling time.)

### COMMAND

Signal from PSX to Controller. This signal is the counter part of DATA. It is again an 8 bit serial transmission on the falling edge of clock.

## VCC

VCC can vary from 5V down to 3V and the official SONY Controllers will still operate. The controllers outlined here really want 5V. The main board in the PSX also has a surface mount 750mA fuse that will blow if you try to draw too much current through the plug (750mA is for both left, right and memory cards).

## ATT

ATT is used to get the attention of the controller. This signal will go low for the duration of a transmission. I have also seen this pin called Select, DTR and Command.

## CLOCK

Signal from PSX to Controller. Used to keep units in sync.

## ACK

Acknowledge signal from Controller to PSX. This signal should go low for at least one clock period after each 8 bits are sent and ATT is still held low. If the ACK signal does not go low within about 60 us the PSX will then start interrogating other devices.

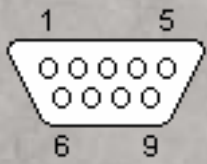
*Contributor:* [Joakim Ögren](#)

*Source:*  
*Sony Playstation Controller Information*

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# TI-99/4A Joystick Port



(At the computer)



(At the joystick cable)

9 PIN D-SUB MALE at the computer.

9 PIN D-SUB FEMALE at the joystick cable.

Pin	Dir	Name
1	-	N.C.
2	OUT	Test joystick 2
3	IN	UP
4	IN	Fire button pressed
5	IN	Left
6	-	N.C.
7	OUT	Test joystick
8	IN	Down
9	IN	Right

*Note: Direction is Computer relative Device.*

Contributor: [Joakim Ögren](#)

Source:  
?

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Document last modified: 2001-06-08*



# Vectrex Controller

## 9 PIN UNKNOWN CONNECTOR

Pin	Description
1	Button 1
2	Button 2
3	Button 3
4	Button 4
5	Horizontal Pot
6	Vertical Pot
7	+5V
8	GND
9	-5V

The joystick potentiometers work by voltage division between -5V and +5V. Actually, it uses a couple of resistors on each side to make it more like -3.4V to 3.4V.

## Vertical Pin 6:

Voltage	Direction
-3.4 V	Down
0 V	Center
+3.4 V	Up

## Horizontal Pin 5:

Voltage	Direction
-3.4 V	Left
0 V	Center

+3.4 V	Right
--------	-------

Contributor: [Joakim Ögren](#), Jay Tilton

Source:

[Vectrex Controller Pinout](#) at [GamesX](#)

[Jay Tilton's Website](#)

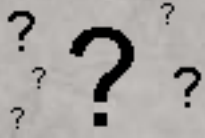
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# AT&T 6300 Keyboard



(at the Computer)

9 PIN D-SUB ??? at the Computer.

Pin	Name	Description
1	DATA	Data
2	CLOCK	Clock
3	GND	Ground
4	GND	Ground
5	+12V	+12 VDC
6	n/c	Not connected
7	n/c	Not connected
8	n/c	Not connected
9	n/c	Not connected

Contributor: [Joakim Ögren](#)

Source:  
[Tommy's pinout Collection](#) by [Tommy Johnson](#)

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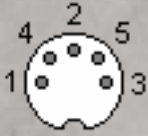
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Document last modified: 2001-06-07





# Keyboard (5 Amiga)



(at the computer)

5 PIN DIN 180° (DIN41524) FEMALE (A1000/A2000/A3000) at the computer.

Pin	A1000	A2000/A3000
1	+5 Volts	KCLK
2	CLOCK	KDAT
3	DATA	n/c
4	GND	GND
5	n/c	+5 Volts

Contributor: [Joakim Ögren](#), [Rob Gill](#)

Source:  
?

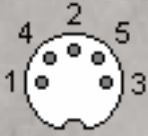
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# Keyboard (5 PC)



(at the computer)

5 PIN DIN 180° (DIN41524) FEMALE at the computer.

Pin	Name	Description	Technical
1	CLOCK	Clock	CLK/CTS, Open-collector
2	DATA	Data	RxD/TxD/RTS, Open-collector
3	n/c	Not connected	Reset on some very old keyboards.
4	GND	Ground	
5	VCC	+5 VDC	

Contributor: [Joakim Ögren](#)

Source:  
?

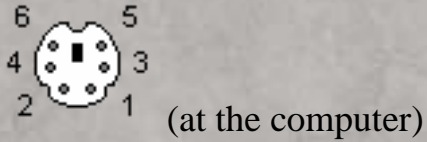
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# Keyboard (6 Amiga)



6 PIN MINI-DIN FEMALE (PS/2 STYLE) (A4000/CDTV) at the computer.

Pin	Name	Dir	Description
1	/DATA		Data
2	n/c	-	Not connected
3	GND		Ground
4	+5V		+5 Volts DC (100 mA max)
5	CLOCK		Clock
6	n/c	-	Not connected

*Note: Direction is Computer relative Keyboard.*

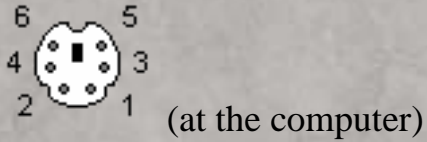
Contributor: [Joakim Ögren](#), [Dirk Duesterberg](#)

Source:  
Amiga 4000 User's Guide from Commodore

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# Keyboard (6 PC)



6 PIN MINI-DIN FEMALE (PS/2 STYLE) at the computer.

Pin	Name	Dir	Description
1	DATA		Key Data
2	n/c	-	Not connected
3	GND		Ground
4	VCC		Power , +5 VDC
5	CLK		Clock
6	n/c	-	Not connected

*Note: Direction is Computer relative Keyboard.*

Contributor: [Joakim Ögren](#), [Gilles Ries](#)

[Source:](#)

[?](#)

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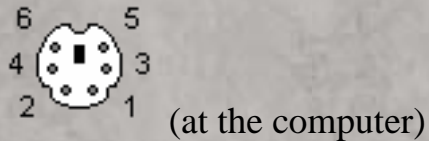
*Document last modified: 2001-06-07*





# Keyboard (Amiga CD32)

The Amiga CD<sup>32</sup> keyboard connector also includes a serialport.



6 PIN MINI-DIN FEMALE (PS/2 STYLE) at the computer.

Pin	Name	Dir	Description
1	/DATA	↔	Data
2	/TxD	→	Transmit Data (0-5V and reversed)
3	GND	—	Ground
4	+5V	→	+5 Volts DC (100 mA max)
5	CLOCK	←	Clock
6	/RxD	←	Receive Data (0-5V and reversed)

*Note: Direction is Computer relative Keyboard.*

Contributor: [Joakim Ögren](#), [Dirk Duesterberg](#)

Source:  
[CD32 keyboard port info](#), Usenet posting by [Klaus Hegemann](#)

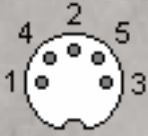
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# Keyboard (XT)



(at the computer)

5 PIN DIN 180° (DIN41524) FEMALE at the computer.

Pin	Name	Description	Technical
1	CLK	Clock	CLK/CTS, Open-collector
2	DATA	Data	RxD, Open-collector
3	/RESET	Reset	
4	GND	Ground	
5	VCC	+5 VDC	

Contributor: [Joakim Ögren](#)

Source:  
?

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# Macintosh Keyboard

Available on Macintosh Mac Plus and earlier.

**NOT  
DRAWN  
YET...**



(at the Computer)



**NOT  
DRAWN  
YET...**



(at the Keyboard)

RJ11 FEMALE CONNECTOR at the Computer.

RJ11 MALE CONNECTOR at the Keyboard.

Pin	Name	Dir	Description
1	CGND		Chassis ground
2	KBD1	?	Keyboard clock
3	KBD2	?	Keyboard data
4	+5V		+5 VDC

*Note: Direction is Computer relative Keyboard.*

Contributor: [Ben Harris](#)

Source:

Apple Tech Info Library, Article ID: TECHINFO-0001424

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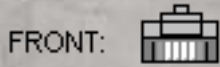
# Macintosh Keyboard Connector



(at the computer)



TOP:



FRONT:

(at the keyboard cable)

RJ11 FEMALE CONNECTOR at the computer.  
RJ11 MALE CONNECTOR at the keyboard cable.

Pin	Name	Description
1	GND	Ground
2	KBD1	Keyboard clock
3	KBD2	Keyboard data
4	+5V	+5 VDC

Contributor: [Joakim Ögren](#)

Source:

[Technote HW19: Pinouts](#) at [Apple Technical Notes](#)

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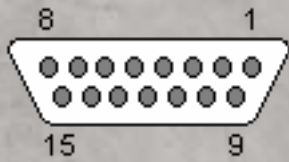
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# SUN Keyboard/Mouse

Available on SUN3's and older

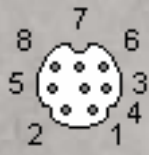


(at the computer)

15 PIN DSUB FEMALE at the computer.









Pin	Name	Dir	Description
1	Keyboard In	←	Keyboard In
2	GND	—	Ground
3	Keyboard Out	→	Keyboard Out
4	GND	—	Ground
5	Mouse In	←	Mouse In
6	GND	—	Ground
7	Mouse Out	→	Mouse Out (!)
8	GND	—	Ground
9	GND	—	Ground
10	VCC	→	Power , +5 VDC
11	VCC	→	Power , +5 VDC
12	VCC	→	Power , +5 VDC
13	VCC	→	Power , +5 VDC
14	VCC	→	Power , +5 VDC
15	VCC	→	Power , +5 VDC

Available on newer SUN machines (3/80 and Sparcs)



(at the computer)

8 PIN MINI-DIN FEMALE at the computer.

Pin	Name	Dir	Description
1	GND		Ground
2	GND		Ground
3	VCC		Power , +5 VDC
4	Mouse In		Mouse In
5	Keyboard Out		Keyboard Out
6	Keyboard In		Keyboard In
7	Power On		Power On (Configurable as Mouse Out on 3/80, 4300, 4400 and 600MP CPUs!)
8	VCC		Power, +5 VDC

*Note: Direction is Computer relative Keyboard/Mouse.*

Contributor: [Joakim Ögren](#)

Source:

*SUN SPARCengine Ultra 20 OEM Manual*

*SUN Field Engineer Handbook, VolumeII, 12/15/93*

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# TI-99/4A Keyboard

UNKNOWN connector (inside the console) Red wire is #15

Pin	12	13	14	15	9	8	6
5	=	.	,	M	N	/	
4	space	L	K	J	H	;	
1	enter	O	I	U	Y	P	
2		9	8	7	6	0	
7	fctn	2	3	4	5	1	lock
3	shift	S	D	F	G	A	
10	ctrl	W	E	R	T	Q	
11		X	C	V	B	Z	

*Note:*

*Pressing a key closes the contact between corresponding row + column. Since there are no diodes to prevent current going backwards, pressing 3 keys at a time often results in appearance of a "phantom" key at the 4th corner of the square formed by these keys (e.g 8+7+3=phantom 4: current goes pin15-7-8-3-pin7 as if 4 were pressed).*

*Contributor:* [Joakim Ögren](#)

*Source:*  
?

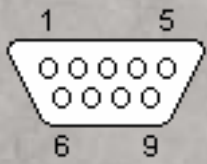
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# Amiga Mouse/Joy



(at the computer)



(at the mouse/joy cable)

9 PIN D-SUB MALE at the computer.

9 PIN D-SUB FEMALE at the mouse/joy cable.

Pin	Mouse/Trackball	Lightpen	Digital Joystick	Paddle	Dir	Comment
1	V-pulse	n/c	/FORWARD	BUTTON 3	←	
2	H-pulse	n/c	/BACK	n/c	←	
3	VQ-pulse	n/c	/LEFT	BUTTON 1	←	
4	HQ-pulse	n/c	/RIGHT	BUTTON 2	←	
5	BUTTON 3(M)	Penpress	n/c	PotX	↔	
6	BUTTON 1(L)	/Beamtrigger	/BUTTON 1	n/c	↔	
7	+5V	+5V	+5V	+5V	→	50 mA max
8	GND	GND	GND	GND	—	
9	BUTTON 2(R)	BUTTON 2	BUTTON 2	PotY	↔	

*Note: Direction is Computer relative Device.*

*Note: Pot is a linear 470 kOhm ( $\pm 10\%$ )*

Contributor: [Joakim Ögren](#)

Source:

*Amiga 4000 User's Guide from Commodore*



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# Apple Macintosh Mouse Connector

## 9 PIN D-SUB CONNECTOR

Pin	Name	Description
1	Ground	
2	+5V	+5 VDC
3	GND	Ground
4	X2	Horizontal movement line (connected to VIA PB4 line)
5	X1	Horizontal movement line (connected to SCC DCDA- line)
6	?	?
7	SW-	Mouse button line (connected to VIA PB3)
8	Y2	Vertical movement line (connected to VIA PB5 line)
9	Y1	Vertical movement line (connected to SCC DCDB- line)

Contributor: [Joakim Ögren](#)

Source:

[Technote HW19: Pinouts](#) at [Apple Technical Notes](#)

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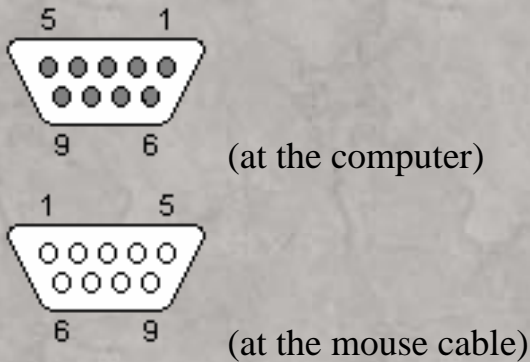
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# Macintosh Mouse

Available on Macintosh Mac Plus and earlier.



9 PIN D-SUB FEMALE at the computer.

9 PIN D-SUB MALE at the mouse cable.

Pin	Name	Dir	Description
1	CGND		Chassis ground
2	+5V		+5 VDC
3	CGND		Chassis ground
4	X2		Horizontal movement line (connected to VIA PB4 line)
5	X1		Horizontal movement line (connected to SCC DCDA-line)
6	n/c	-	Not connected
7	SW-		Mouse button line (connected to VIA PB3)
8	Y2		Vertical movement line (connected to VIA PB5 line)
9	Y1		Vertical movement line (connected to SCC DCDB-line)

*Note: Direction is Computer relative Mouse.*

Contributor: [Ben Harris](#)

Source:

Apple Tech Info Library, Article ID: TECHINFO-0001424

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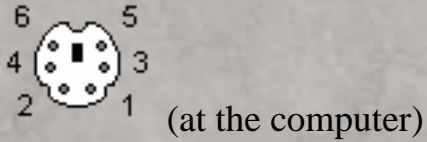
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# Mouse (PS/2)



6 PIN MINI-DIN FEMALE (PS/2 STYLE) at the computer.

Pin	Name	Dir	Description
1	DATA	↔	Key Data
2	n/c	-	Not connected
3	GND	—	Ground
4	VCC	→	Power , +5 VDC
5	CLK	→	Clock
6	n/c	-	Not connected

*Note: Direction is Computer relative Mouse.*

*Contributor:* [Joakim Ögren](#), [Gilles Ries](#)

*Source:*  
?

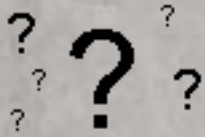
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# SGI Mouse (Model 021-0004-002) Connector



(at the Computer)

9 PIN D-SUB ??? at the Computer.

Pin	Name	Dir	Description
1	+5V		+5 VDC
2	-5V		-5 VDC
3	n/c	-	Not connected
4	n/c	-	Not connected
5	MTXD		Data
6	n/c	-	Not connected
7	n/c	-	Not connected
8	n/c	-	Not connected
9	GND		Ground

*Note: Direction is Computer relative Mouse.*

Contributor: [Joakim Ögren](#)

Source:  
[Tommy's pinout Collection](#) by [Tommy Johnson](#)

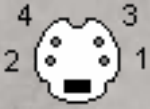
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# Apple Desktop Bus (ADB)



(at the computer)

4 PIN MINI-DIN FEMALE at the computer.

Pin	Name	Description
1	Data	Data, grounded by an open collector or pulled to +5 V through 470
2	Power On	Power on, fed by +5 V through 100 k; connect to pin 4 to turn on the system
3	+5V	+5 V at 500 mA maximum drain; protected by a 1.25-A circuit breaker
4	GND	Ground return

At least available on: Power Macintosh 9500

Contributor: [Joakim Ögren](#)

Source:

[Apple Tech Info Library 18207: Power Macintosh 9500 Pinouts](#) at [Apple TIL homepage](#)

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We receive many e-mails every day, please help us categorize them:

<b>Pinout</b>	<a href="mailto:pinout@hardwarebook.net">pinout@hardwarebook.net</a>	Connector pinouts.
<b>Cable</b>	<a href="mailto:cable@hardwarebook.net">cable@hardwarebook.net</a>	Cable & adapters descriptions.
<b>Circuits</b>	<a href="mailto:circuit@hardwarebook.net">circuit@hardwarebook.net</a>	Circuits for the Circuit section.
<b>Error/Bugs</b>	<a href="mailto:error@hardwarebook.net">error@hardwarebook.net</a>	Error/bugs found in HwB.
<b>Mirror</b>	<a href="mailto:mirror@hardwarebook.net">mirror@hardwarebook.net</a>	Apply to become a mirror of HwB.
<b>General</b>	<a href="mailto:hwb@hardwarebook.net">hwb@hardwarebook.net</a>	General info for HwB.

Please don't send questions like "Do you have the pinout to Xyz", "Can you help us to repair my Xyz" or "Where can I buy an Xyz", please redirect these to a UseNet newsgroup instead. Try [Groups.Google.com](http://Groups.Google.com)

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[ [Audio/Video](#) | [Loopback plugs](#) | [Misc](#) | [Networks](#) | [Parallel](#) | [Serial](#) | [Storage](#) ]

What does the information that is listed for each connector mean? See the [tutorial](#).

## Audio/Video

### Home Audio/Video

[Amiga to SCART](#)

[C128/C64C to SCART \(S-Video\)](#)

[NeoGeo to SCART](#)

[Video to TV SCART](#)

### Video

[9 to 15 pin VGA](#)

[Amiga to C1084 Monitor](#)

[C128/C64C to CBM 1902A Monitor](#)

## Loopback plugs

### Parallel

[Parallel Port Loopback \(CheckIt\)](#)

[Parallel Port Loopback \(Norton\)](#)

### Serial

[Serial Port Loopback \(25 CheckIt\)](#)

[Serial Port Loopback \(25 Norton\)](#)

[Serial Port Loopback \(9 CheckIt\)](#)

[Serial Port Loopback \(9 Norton\)](#)

# Misc

## MIDI

[MIDI](#)

## Serial

[Mac to HP48](#)

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# Networks

## AUI

[AAUI to AUI](#)

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## Ethernet

[Ethernet 10/100/1000Base-T and 100Base-T4 Crossover](#)

[Ethernet 10/100/1000Base-T Straight Thru](#)

# Parallel

[64NET](#)

[C64 Centronics Printer](#)

[GEOCable](#)

[LapLink/InterLink Parallel](#)

[ParNet Parallel](#)

[ParaLoad](#)

[Printer](#)

# Serial

## Information

[Defintion: DTE & DCE](#)

## Modem (Straight)

[Mac to C64 Nullmodem](#)

[Macintosh Modem \(With DTR\)](#)

[Macintosh Modem \(Without DTR\)](#)

[Modem \(25-25\)](#)

[Modem \(9-15\)](#)

[Modem \(9-25\)](#)

[Nullmodem \(25-25\)](#)

[Nullmodem \(9-25\)](#)

[Nullmodem \(9-9\)](#)

[Two-Wire Modem \(25-25\)](#)

[Two-Wire Modem \(9-25\)](#)

## Nullmodem (Crossed)

[Mac to C64 Nullmodem](#)

[Nullmodem \(25-25\)](#)

[Nullmodem \(9-25\)](#)

[Nullmodem \(9-9\)](#)

[Cisco Console \(25\)](#)

[Cisco Console \(9\)](#)

[Conrad Electronics MM3610D \(25\)](#)

[Conrad Electronics MM3610D \(9\)](#)

[RocketPort Serial \(25\)](#)

[Serial Printer \(25-25\)](#)

[Serial Printer \(9-25\)](#)

## Storage

### Floppy

[Floppy](#)

[X1541](#)

## Harddrive

[ESDI](#)

[ST506/412](#)

## IDE/ATA

[IDE](#)

[Paravision SX1 to IDE](#)

## SCSI

[SCSI Cable \(Amiga/Mac\)](#)

[SCSI Cable \(D-Sub to Hi D-Sub\)](#)

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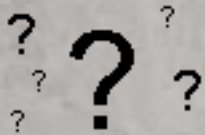
# Short tutorial

## Heading

First at each page there a short heading describing the cable.

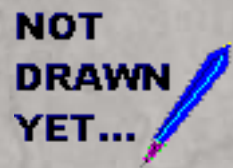
## Pictures of the connectors

After that there is at each page there is one or more pictures of the connectors. Sometimes there is some question marks only. This means that we don't know what kind of connector it is or how it looks.



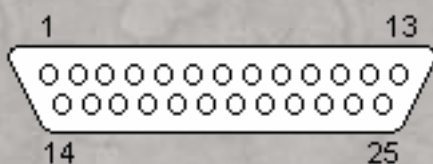
(to the computer)

There may be some pictures we haven't drawn yet. We illustrate this with the following advanced picture:

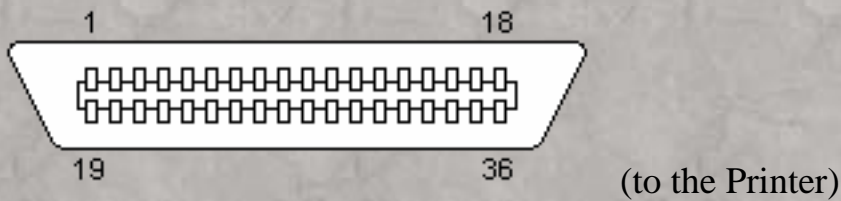


(to the computer)

Normally are one or more pictures. **These are seen from the front, and NOT the soldside. Holes (female connectors usually) are darkened.** Look at the example below. The first is a female connector and the send a male. The texts inside parentheses will tell you at which kind of the device it will look like that.



(to the Computer)



## Texts describing the connectors

Below the pictures there is texts that describes the connectors. Including the name of the physical connector.

25 PIN D-SUB MALE to the Computer

36 PIN CENTRONICS MALE to the Printer.

## Pin table

The pin table is perhaps the information you are looking for. Should be simple to read. Contains mostly the following three columns; Name, Pin 1, Pin 2. Sometimes when not the same pin is connected to each side there is another column describing the name at connector 2.

	<b>25-DSub</b>	<b>36-Cen</b>
Strobe	1	1
Data Bit 0	2	2
Data Bit 1	3	3
Data Bit 2	4	4
Data Bit 3	5	5
Data Bit 4	6	6
Data Bit 5	7	7
Data Bit 6	8	8
Data Bit 7	9	9
...	...	...

## Contributor & Source

All persons that helped us or sent us information about the connector will be listed here. The source of the information is perhaps a book or another site.

*Contributor:* [Joakim Ögren](#)

*Source:* *Amiga 4000 User's Guide from Commodore*

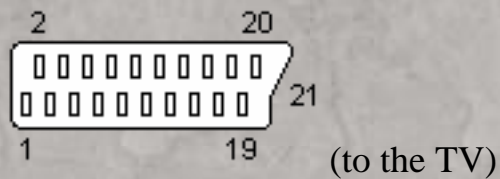
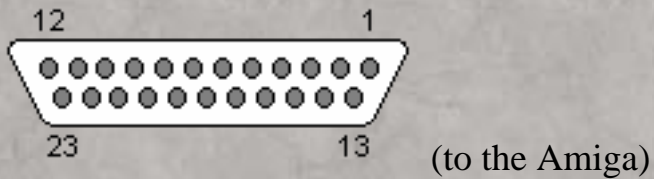
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*Document last modified:* 2001-06-07



# Amiga to SCART



23 PIN D-SUB FEMALE to the Amiga

21 PIN SCART MALE to the TV

	Amiga	TV	
Analog Red	3	15	RGB Red In
Analog Green	4	11	RGB Green In
Analog Blue	5	7	RGB Blue In
Composite Sync	10	20	Video In
Video GND	17	17	Video GND
GND	19	18	Blanking GND
+12V	22	16	Blanking (Connect via a 150 Ohm resistor)
+12V	22	8	Audio/RGB switch (Connect via a 1 kOhm resistor)
Phono Right		2	Audio IN Right
Phono Right GND		4	GND
Phono Left		6	Audio IN Left
Phono Left GND		4	GND

Contributor: [Joakim Ögren](#)



*Source:*

*?*

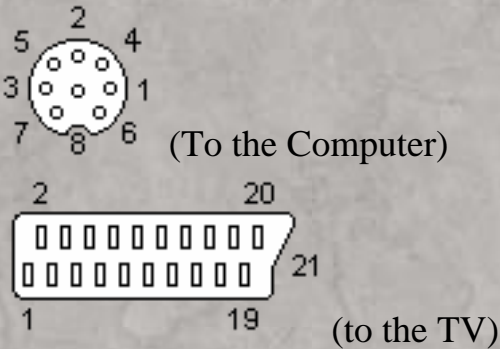
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*Document last modified: 2001-06-07*



# C128/C64C to SCART (S-Video)



8 PIN DIN (DIN45326) MALE at the Computer.  
 21 PIN SCART MALE to the TV

	Computer	TV	
LUM	1	20	LUM
CHROMA	8	15	CHROMA
GND	2	4+17	GND
AOUT	3	2+6	AUDIO

Contributor: [Joakim Ögren](#), [Claudio Brazzale](#)

Source:  
 ?

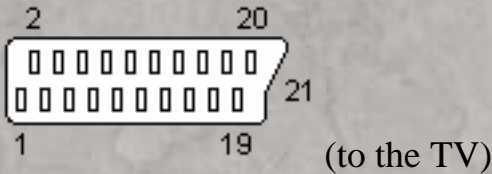
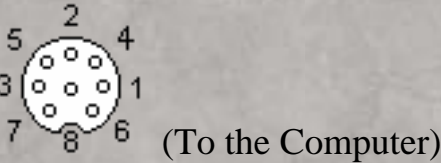
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# NeoGeo to SCART



8 PIN DIN (DIN45326) MALE to the Computer.  
21 PIN SCART MALE to the TV

	NeoGeo	TV	
Audio Out	1	6+2	Audio In Left+Right
Ground	2	18	Blanking Signal Ground
Composite Video Out	3	20	Composite Video In
?	4	16	Blanking Signal
Green	5	11	RGB Green In
Red	6	15	RGB Red In
Blue	8	7	RGB Blue In

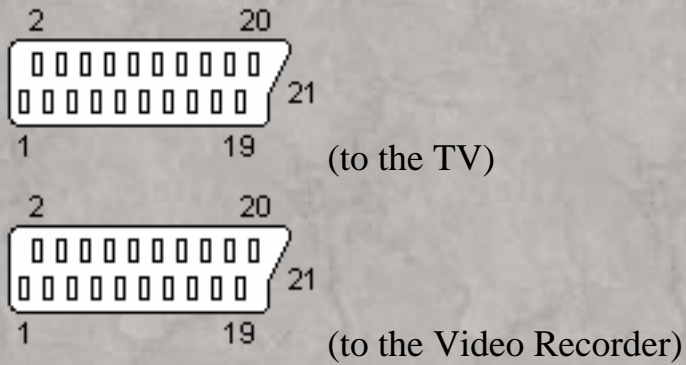
Contributor: [Joakim Ögren](#), [Enzo](#), [Steffen Kupfer](#)

Source:  
?

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# Video to TV SCART



21 PIN SCART MALE to the TV.

21 PIN SCART MALE to the Video Recorder.

	TV	VCR	
Audio Right Out	1	2	Audio Right In
Audio Right In	2	1	Audio Right Out
Audio Left Out	3	6	Audio Left In
Audio Left In	6	3	Audio Left Out
Audio Ground	4	4	Audio Ground
Red	15	15	Red
Red Ground	13	13	Red Ground
Green	11	11	Green
Green Ground	9	9	Green Ground
Blue	7	7	Blue
Blue Ground	5	5	Blue Ground
Status / 16:9	8	8	Status / 16:9
Reserved	10	10	Reserved
Reserved	12	12	Reserved
Fast Blanking Ground	14	14	Fast Blanking Ground
Fast Blanking	16	16	Fast Blanking



Video Out Ground	17	18	Video In Ground
Video In Ground	18	17	Video Out Ground
Video Out	19	20	Video In
Video In	20	19	Video Out
Ground	21	21	Ground

*Contributor:* [Joakim Ögren](#)

*Source:*  
?

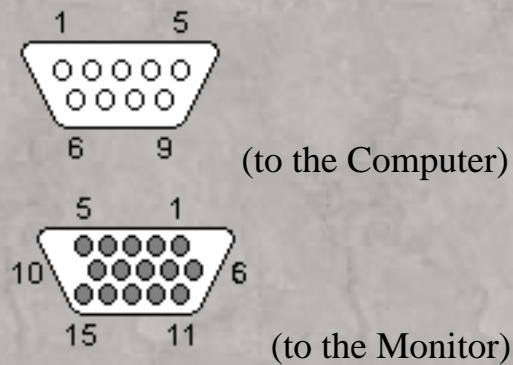
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# 9 to 15 pin VGA



9 PIN D-SUB MALE to the Computer

15 PIN HIGH DENSITY D-SUB FEMALE to the Monitor

	9-Pin	15-Pin
Red Video	1	1
Green Video	2	2
Blue Video	3	3
Horizontal Sync	4	13
Vertical Sync	5	14
Red GND	6	6
Green GND	7	7
Blue GND	8	8
Sync GND	9	10 + 11

Contributor: [Joakim Ögren](#)

Source:  
?

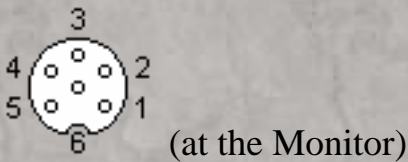
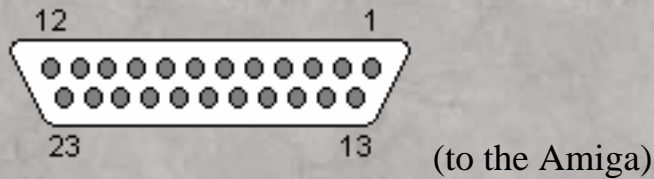
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# Amiga to C1084 Monitor



23 PIN D-SUB FEMALE to the Amiga.  
6 PIN DIN MALE at the Monitor.

	Amiga	C1084	
R	3	4	R
G	4	1	G
B	5	5	B
SYNC	10	2	HSYNC
GND	16	3	GND

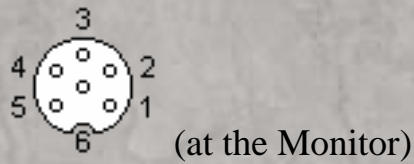
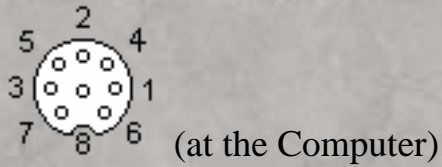
Contributor: [Joakim Ögren](#)

Source:  
Usenet posting in [sfnet.harrastus.elektroniikka](#), Philips 1084 monarin kytkenta by [Kari Hautanen](#)

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Document last modified: 2001-06-08



# C128/C64C to CBM 1902A Monitor



8 PIN DIN (DIN45326) MALE at the Computer.  
6 PIN DIN MALE at the Monitor.

	Computer	C1902A	
LUM	1	6	LUM
CHROMA	8	4	CHROMA
GND	2	3	GND
AOUT	3	2	AUDIO

Contributor: [Joakim Ögren](#)

Source:  
[cbm.comp.sys General FAQ v3.1 Part 7](#)

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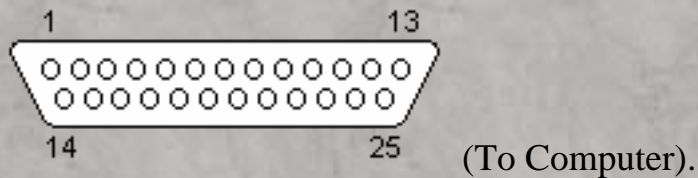
Document last modified: 2001-06-08





# Parallel Port Loopback (CheckIt)

Used to verify that a port is working. This one works with CheckIt.



25 PIN D-SUB MALE to Computer.

Name	Pin	Pin	Name
Busy	11	17	Select Input
Acknowledge	10	16	Initialize
Paper end	12	14	Auto Feed
Select	13	1	Strobe
Data Bit 0	2	15	Error

Contributor: [Joakim Ögren](#), "[Coolsys](#)"

Source:  
?

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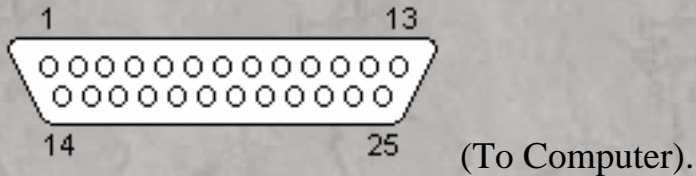
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Document last modified: 2001-06-07



# Parallel Port Loopback (Norton)

Used to verify that a port is working. This one works with Norton Utilities: Norton Diagnostics from Symantec.



25 PIN D-SUB MALE to Computer.

Name	Pin	Pin	Name
Data Bit 0	2	15	Error
Data Bit 1	3	13	Select
Data Bit 2	4	12	Paper Out
Data Bit 3	5	10	Acknowledge
Data Bit 4	6	11	Busy

Contributor: [Joakim Ögren](#)

Source:  
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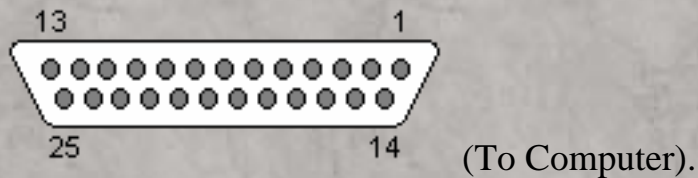
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# Serial Port Loopback (25 CheckIt)

Used to verify that a port is working. This one works with CheckIt.



25 PIN D-SUB FEMALE to Computer.

Name	Pin	Pin	Pin	Pin
Jumpering 1	2	3		
Jumpering 2	4	5		
Jumpering 3	6	8	20	22

Contributor: [Joakim Ögren](#), "[Coolsys](#)"

Source:

?

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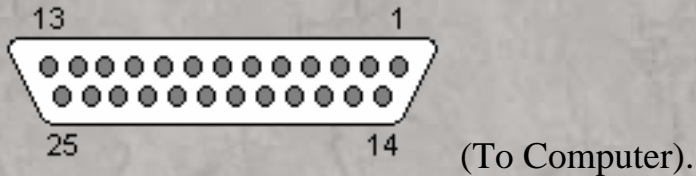
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Document last modified: 2001-06-07



# Serial Port Loopback (25 Norton)

Used to verify that a port is working. This one works with Norton Utilities: Norton Diagnostics from Symantec.



25 PIN D-SUB FEMALE to Computer.

Name	Pin	Pin	Pin	Pin
Jumpering 1	2	3		
Jumpering 2	4	5		
Jumpering 3	6	8	20	22

Contributor: [Joakim Ögren](#)

Source:

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# Serial Port Loopback (9 CheckIt)

Used to verify that a port is working. This one works with CheckIt.



(To Computer).

9 PIN D-SUB FEMALE to Computer.

Name	Pin	Pin	Name
CD	1	6	DSR
CD	1	9	RI
RXD	2	3	TXD
DTR	4	6	DSR
RTS	7	8	CTS

Contributor: [Joakim Ögren](#), "[Coolsys](#)"

Source:  
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# Serial Port Loopback (9 Norton)

Used to verify that a port is working. This one works with Norton Utilities: Norton Diagnostics from Symantec.



(To Computer).

9 PIN D-SUB FEMALE to Computer.

Name	Pin	Pin	Pin	Pin
Jumpering 1	2	3		
Jumpering 2	7	8		
Jumpering 3	1	4	6	9

Contributor: [Joakim Ögren](#)

Source:  
?

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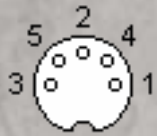
Document last modified: 2001-06-08



# MIDI



(to the 1st peripheral)



(to the 2nd peripheral)

5 PIN DIN 180° (DIN41524) MALE to the 1st peripheral.

5 PIN DIN 180° (DIN41524) MALE to the 1st peripheral.

	1st	2nd
Shield	2	2
Current Source	4	4
Current Sink	5	5

*Note: Although that pin 2 only is connected at MIDI Out it's simpler to connect it to both ends.*

Contributor: [Joakim Ögren](#)

Source:

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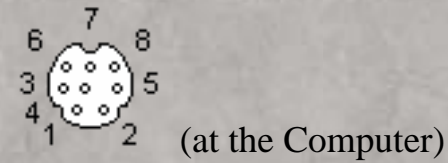
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# Mac to HP48



**NOT  
DRAWN  
YET...**



(to the HP48).

8 PIN MINI-DIN MALE to the Computer.

4 PIN ??? FEMALE to the HP48

	Mac	HP48	
TxD-	3		RxD
RxD-	5		TxD
GND+RxD+	4+8		GND
Shield	SHIELD	SHIELD	Shield

Contributor: [Joakim Ögren](#), [Pierre Olivier](#)

Sources:

Usenet posting in comp.sys.cbm, Mac to C64 Interface by Tomas Moberg

Usenet posting in comp.sys.cbm, A very simple C64 to Macintosh serial cable by [Chris Baird](#)

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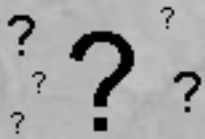




# Misc Unsupported Cables

These cables may or may not be correctly constructed. Handle with care.

## Amiga to IBM RGBI Cable



(to the Monitor).



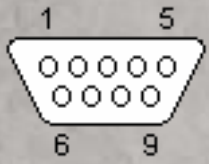
(to the Amiga).

9 PIN D-SUB ?? to the Monitor.

23 PIN D-SUB FEMALE to the Amiga.

	9 Pin	23 Pin	Comment
Ground	1	16	
Ground	2	16	
Digital Red	3	9	(Via 2 Hex Inverters, i.e 74LS04)
Digital Green	4	8	(Via 2 Hex Inverters, i.e 74LS04)
Digital Blue	5	9	(Via 2 Hex Inverters, i.e 74LS04)
Digital Intensity	6	6	(Via 2 Hex Inverters, i.e 74LS04)
Horizontal Sync	8	11	(Via 1 Hex Inverters, i.e 74LS04)
Verical Sync	9	12	(Via 1 Hex Inverters, i.e 74LS04)
+5V		23	(Power for the IC)

# C128 80 columns to 1702 monitor Cable



(to the C128).

**NOT  
DRAWN  
YET...**



(to the C1702).

9 PIN D-SUB MALE to the C128.

PHONO MALE to the Monitor.

	C128	C1702	
Ground	1	1	Ground
Monochrome out	7	2	Signal

Contributor: [Joakim Ögren](#)

Source:

[Gordon](#)

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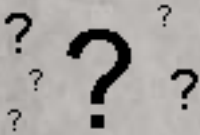
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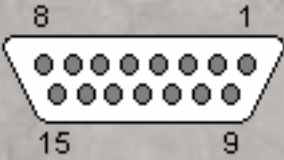


# AAUI to AUI

Is the directions right???



(to the Macintosh)



(to the Transciever)

14 PIN UNKNOWN CONNECTOR to the Macintosh (AAUI)  
15 PIN D-SUB FEMALE to the Transciever (AUI)

Description	AAUI	AUI
control in circuit A	5	2
data out circuit A	9	3
data in circuit shield	shell	4
data in circuit A	2	5
voltage common	4	6
control out circuit shield	shell	8
control in circuit B	6	9
data out circuit B	10	10
data out circuit shield	shell	11
data in circuit B	3	12
voltage plus	1	13
voltage shield	shell	14

Contributor: [Joakim Ögren](#)

*Source:*

*[Apple Tech Info Library 9980: AAUI, Pinout Equivalents to AUI](#) at [Apple TIL homepage](#)*

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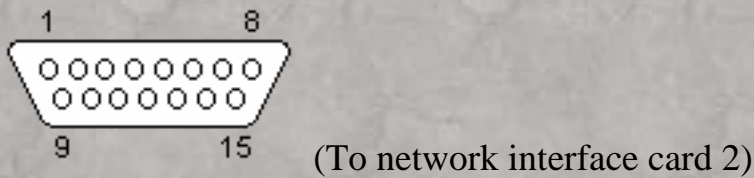
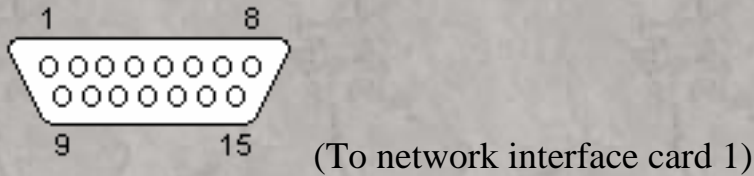
*Document last modified: 2001-06-07*





# Ethernet AUI to AUI

This cable can be used to connect to network interface cards (with AUI connector) together, without use of transceivers.



15 PIN D-SUB MALE to network interface card 1.

15 PIN D-SUB MALE to network interface card 2.

Name	AUI1	AUI2	Name
TxD A	3	5	RxD A
RxD A	5	3	TxD A
TxD B	10	12	RxD B
RxD B	12	10	TxD B

And make the following jumper at each end:

Name	Pin
Vc	6
Collision Detect B	9

Contributor: [René Guzmán](#)

Source:

Usenet posting by [Andrew J V Yeomans](#)

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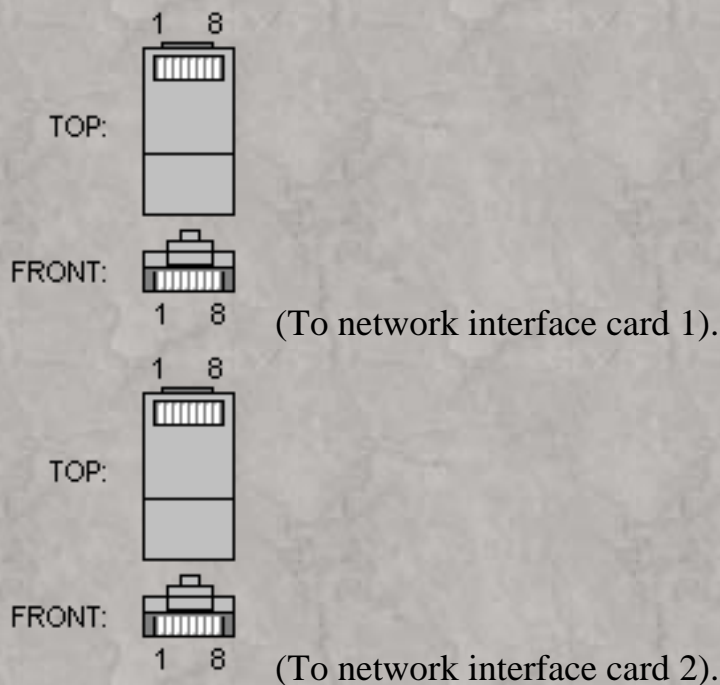
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*Document last modified: 2001-06-08*



# Ethernet 10/100/1000Base-T and 100Base-T4 Crossover

This cable can be used to cascade hubs, or for connecting two Ethernet stations back-to-back without a hub. It works with 10Base-T, 100Base-TX, 100Base-T4 and 1000Base-T. Use a good enough cable, if you are confused about categories of cables then use category 5e(nhanced) and you'll be fine even at 1000Base-T.



RJ45 MALE CONNECTOR to network interface card 1.

RJ45 MALE CONNECTOR to network interface card 2.

(1000Base-T names in parentheses)

Name	NIC1	Color	NIC2	Name
TX+ (BI_DA+)	1	White/Orange	3	RX+ (BI_DB+)
TX- (BI_DA-)	2	Orange	6	RX- (BI_DB-)
RX+ (BI_DB+)	3	White/Green	1	TX+ (BI_DA+)
- (BI_DC+)	4	Blue	7	- (BI_DD+)

- (BI_DC-)	5	White/Blue	8	- (BI_DD-)
RX- (BI_DB-)	6	Green	2	TX- (BI_DA-)
- (BI_DD+)	7	White/Brown	4	- (BI_DC+)
- (BI_DD-)	8	Brown	5	- (BI_DC-)

That means that the white/orange cable connected to NIC 1 pin 1 should go to NIC 2 pin 3 and NIC 1 pin 2 to NIC 2 pin 6 etc.

*Note 1: It's important that each pair is kept as a pair. TX+ & TX- must be in the pair, and RX+ & RX- must together in another pair. (Just as the table above shows).*

*Note 2: While 10Base-T and 100Base-TX only uses 2 pairs, please connect all four since 100Base-T4 and 1000Base-T needs them and save yourself some future debugging :)*

*Note 3: The colors originate from the numbering and name on NIC1.*

*Contributors:* [Joakim Ögren](#), [Niklas Edmundsson](#), [Jim C?](#), [Jason D. Pero](#), [Oscar Fernandez Sierra](#), [Cayce Balara](#), [Jeffrey R. Broido](#), [Patrick Smart](#), [Jeffrey R. Broido](#), [Kim Scholte](#)

*Source:*  
*IEEE Std 802.3, 2000 Edition*

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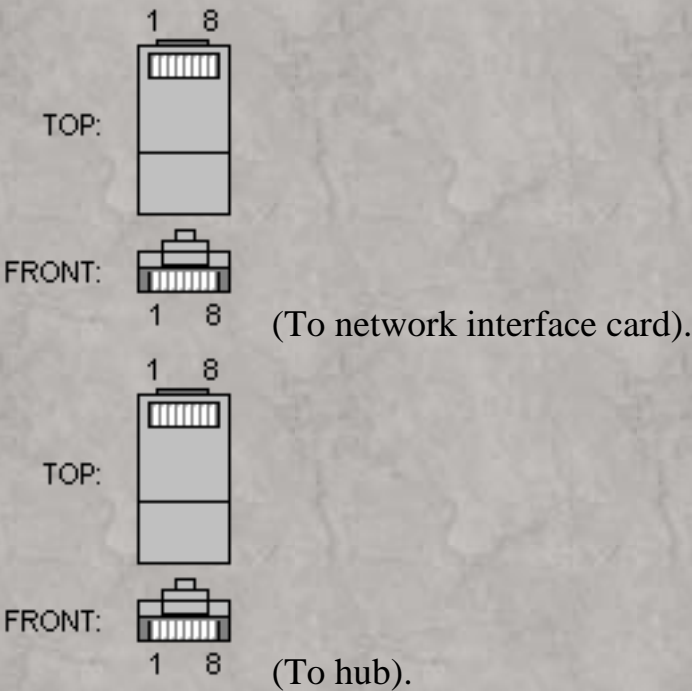


# Ethernet 10/100/1000Base-T Straight Thru

Wiring scheme: EIA/TIA 568B

This cable will work with 10Base-T, 100Base-TX and 1000Base-T and is used to connect a network interface card to a hub or network outlet. These cables are sometimes called "whips".

Note: While 10BaseT and 100Base-TX only uses two pairs, please do connect all pairs since 1000BaseT uses all of them, and save yourself some future debugging :)



RJ45 MALE CONNECTOR to network interface card).  
RJ45 MALE CONNECTOR to hub).

Name	Pin	Cable Color	Pin	Name
TX+	1	White/Orange	1	TX+
TX-	2	Orange	2	TX-
RX+	3	White/Green	3	RX+

	4	Blue	4	
	5	White/Blue	5	
RX-	6	Green	6	RX-
	7	White/Brown	7	
	8	Brown	8	

*Note: It's important that each pair is kept as a pair. TX+ & TX- must be in the pair, and RX+ & RX- must together in another pair. (Just as the table above shows).*

Just for your information, this is how the pairs are named:

Pair	Pins	Common color
1	4 & 5	Blue
2	1 & 2	Orange
3	3 & 6	Green
4	7 & 8	Brown

The + side of each pair is called the "tip" and the - side is called the "ring", a reference to old telephone connectors.

*Contributor:* [Joakim Ögren](#), [Oscar Fernandez Sierra](#), [Jeffrey R. Broido](#)

*Source:*  
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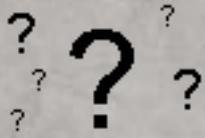
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# 64NET



(To C64).



(To PC).

DZM 12 DREH to the C64 UserPort.

25 PIN D-SUB MALE to the PC

	C64	Dir	PC	
GND	A	—	25	GND
PB0	C	→	10	/ACK
PB1	D	→	11	BUSY
PB2	E	→	12	PE
PB3	F	←	5	D3
PB4	H	←	6	D4
PB5	J	←	7	D5
PB6	K	←	8	D6
PB7	L	←	9	D7

Contributor: [Joakim Ögren](#)

Source:

64NET v1.82.58 documentation by [Paul Gardner-Stephen](#)

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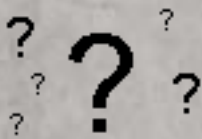
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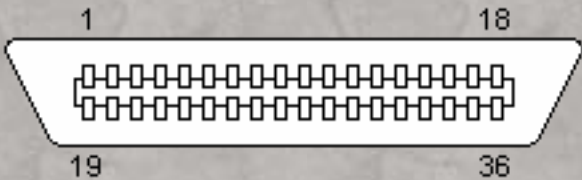


# C64 Centronics Printer

Requires a cartridge with Centronics support (TFCIII or ActionReplay.)



(to the C64).



(to the Printer)

DZM 12 DREH to the C64 UserPort.  
36 PIN CENTRONICS MALE to the Printer.

	C64	Dir	Printer	
GND	1,12,A,N	→	19-30,33	Ground
FLAG2	B	←	10	Acknowledge
PB0	C	→	2	Data 0
PB1	D	→	3	Data 1
PB2	E	→	4	Data 2
PB3	F	→	5	Data 3
PB4	H	→	6	Data 4
PB5	J	→	7	Data 5
PB6	K	→	8	Data 6
PB7	L	→	9	Data 7
PA2	M	→	1	Strobe
GND	3	→	31	Initialize Printer

Contributor: [Joakim Ögren](#)



*Source:*

*CBM Memorial Page Pinouts - pinout by [Roy Kannady](#)*

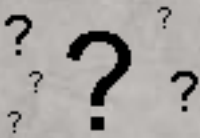
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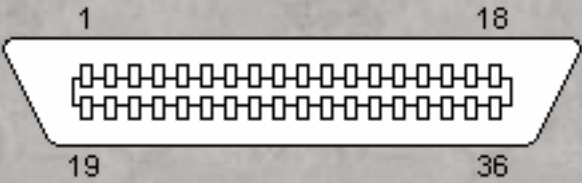
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# GEOCable



(to the C64).



(to the Printer)

DZM 12 DREH to the C64 UserPort.  
36 PIN CENTRONICS MALE at the Printer.

	C64	Printer	
Ground	A	33	Ground
Flag 2	B	11	Busy
PB0	C	2	Data 1
PB1	D	3	Data 2
PB2	E	4	Data 3
PB3	F	5	Data 4
PB4	H	6	Data 5
PB5	J	7	Data 6
PB6	K	8	Data 7
PB7	L	9	Data 8
PA2	M	1	Strobe
Ground	N	16	Ground

Contributor: [Joakim Ögren](#)

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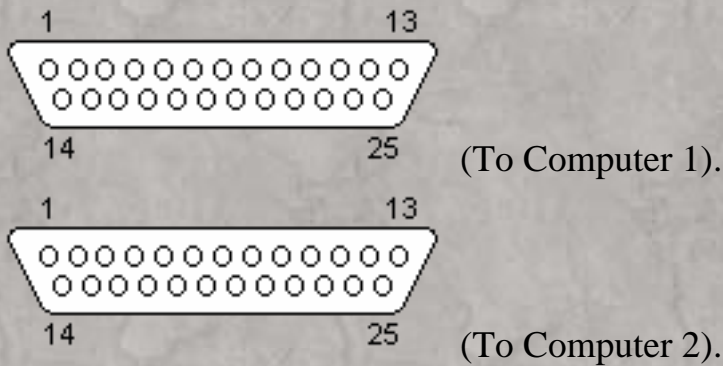
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# LapLink/InterLink Parallel

Will work with:

- LapLink from Travelling Software
- MS-DOS v6.0 InterLink from Microsoft
- Windows 95 Direct Cable connection from Microsoft
- Norton Commander v4.0 & v5.0 from Symantec



25 PIN D-SUB MALE to Computer 1.

25 PIN D-SUB MALE to Computer 2.

Name	Pin	Pin	Name
Data Bit 0	2	15	Error
Data Bit 1	3	13	Select
Data Bit 2	4	12	Paper Out
Data Bit 3	5	10	Acknowledge
Data Bit 4	6	11	Busy
Acknowledge	10	5	Data Bit 3
Busy	11	6	Data Bit 4
Paper Out	12	4	Data Bit 2
Select	13	3	Data Bit 1
Error	15	2	Data Bit 0
Reset	16	16	Reset



Select	17	17	Select
Signal Ground	25	25	Signal Ground

*Contributor:* [Joakim Ögren](#)

*Source:*  
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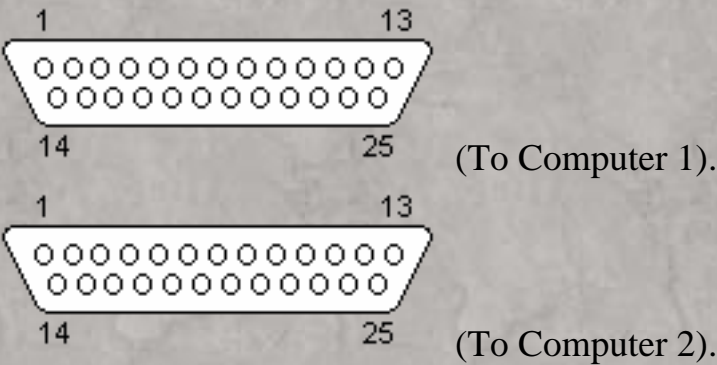
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# ParNet Parallel



25 PIN D-SUB MALE to Computer 1.  
25 PIN D-SUB MALE to Computer 2.

Name	Pin	Pin	Name
Data Bit 0	2	2	Data Bit 0
Data Bit 1	3	3	Data Bit 1
Data Bit 2	4	4	Data Bit 2
Data Bit 3	5	5	Data Bit 3
Data Bit 4	6	6	Data Bit 4
Data Bit 5	7	7	Data Bit 5
Data Bit 6	8	8	Data Bit 6
Data Bit 7	9	9	Data Bit 7
Acknowledge + Select	10+13	10+13	Acknowledge + Select
Busy	11	11	Busy
Paper Out	12	12	Paper Out
Signal Ground	17-25	17-25	Signal Ground

Contributor: [Joakim Ögren](#)

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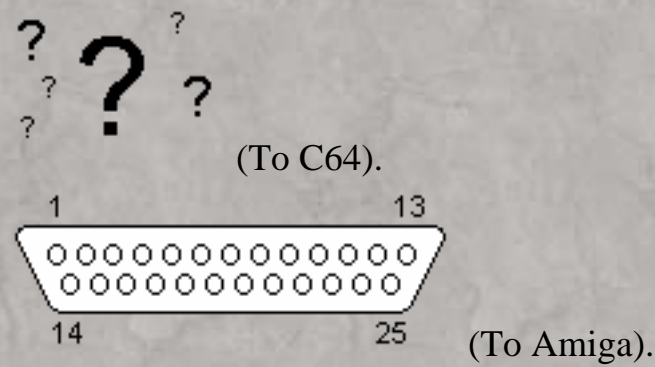
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# ParaLoad



DZM 12 DREH at the C64 UserPort.  
25 PIN D-SUB MALE at the Amiga

	C64	Amiga	
Ground	A	17-25	Ground
FLAG2	B	1	Strobe
PB0	C	2	D0
PB1	D	3	D1
PB2	E	4	D2
PB3	F	5	D3
PB4	H	6	D4
PB5	J	7	D5
PB6	K	8	D6
PB7	L	9	D7
PA2	M	11	Busy

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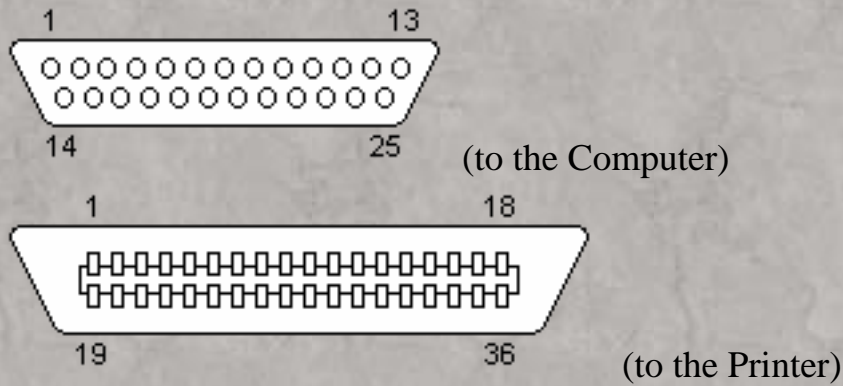
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# Printer



25 PIN D-SUB MALE to the Computer  
 36 PIN CENTRONICS MALE to the Printer.

	25-DSub	36-Cen
Strobe	1	1
Data Bit 0	2	2
Data Bit 1	3	3
Data Bit 2	4	4
Data Bit 3	5	5
Data Bit 4	6	6
Data Bit 5	7	7
Data Bit 6	8	8
Data Bit 7	9	9
Acknowledge	10	10
Busy	11	11
Paper Out	12	12
Select	13	13
Autofeed	14	14
Error	15	32
Reset	16	31

Select	17	36
Signal Ground	18	33
Signal Ground	19	19,20
Signal Ground	20	21,22
Signal Ground	21	23,24
Signal Ground	22	25,26
Signal Ground	23	27
Signal Ground	24	28,29
Signal Ground	25	30,16
Shield	Shield	Shield+17

Contributor: [Joakim Ögren](#), [Petr Krc](#)

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# Defintion: DTE & DCE

## DTE

DTE is acronym for Data Terminal Equipment.

Examples of DTE is computers, printers & terminals.

## DCE

DCE is acronym for Data Communication Equipment.

Examples of DCE is modems.

## Wiring

Wiring a cable for DTE to DCE communication is easy. All wires goes straight from pin x to pin x.

But wiring a cable for DTE to DTE (nullmodem) or DCE to DCE requires that some wires are crossed. A signal should be wired from pin x to the opposite signal at the other end. With opposite signals means for example Transmit & Receive.

*Contributors:* [Joakim Ögren](#), [Richard L. Lane](#), [Rob Gill](#)

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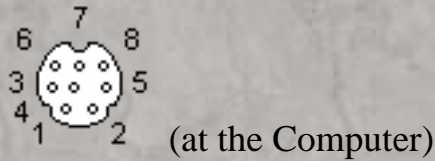
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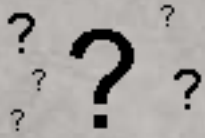


# Mac to C64 Nullmodem

The RS-232 standard on the C64 is a little bit strange. It uses inverted TTL level for the signals. The RS-422 ports on the Macintosh has both an inverted and non-inverted input. By using the inverted instead of non-inverted the inverted C64 level is back to normal.



(at the Computer)



(to the C64).

8 PIN MINI-DIN MALE to the Macintosh.

DZM 12 DREH to the C64 UserPort.

	Mac	C64	
GND+RXD-	4+5	1+12+A+N	GND
RXD+	8	M	TXD (PA2)
TXD+	6	B+C	RXD (FLAG2+PB0)
		D+E	RTS+DTR (PB1+PB2)

Contributor: [Joakim Ögren](#), [Pierre Olivier](#)

Source:

Usenet posting in comp.sys.cbm, A very simple C64 to Macintosh serial cable by [Chris Baird](#)

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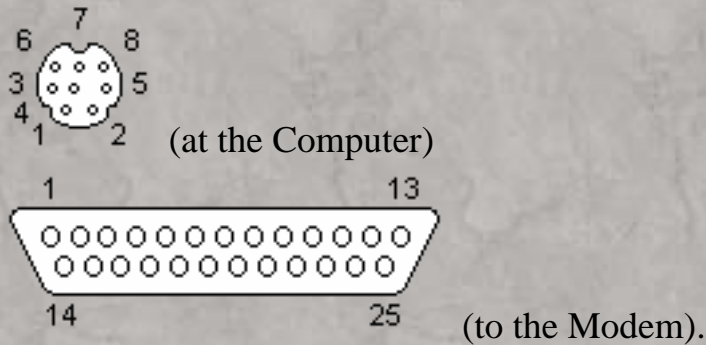
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# Macintosh Modem (With DTR)

This cable should be used for [DTE to DCE](#) (for instance computer to modem) connections with DTR.



8 PIN MINI-DIN MALE to the Computer.

25 PIN D-SUB MALE to the Modem

	Mac	Dir	Modem	
HSK <sub>o</sub>	1	→	4+20	RTS+DTR
HSK <sub>i</sub>	2	←	5	CTS
TxD-	3	→	2	TxD
RxD-	5	←	3	RxD
GND+RxD+	4+8	-	7	GND
GPi	7	←	8	DCD

Contributor: [Joakim Ögren](#), [Pierre Olivier](#)

Source:

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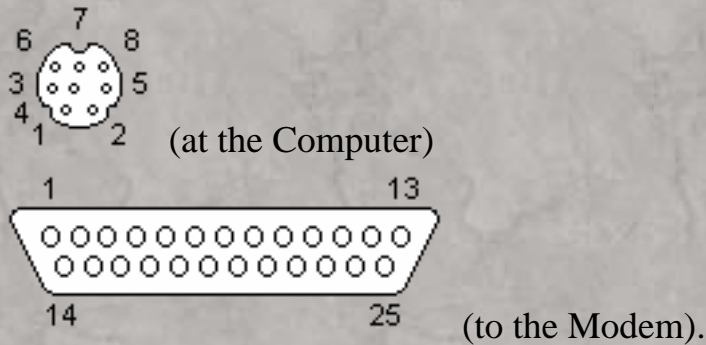
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# Macintosh Modem (Without DTR)

This cable should be used for [DTE to DCE](#) (for instance computer to modem) connections without DTR.



8 PIN MINI-DIN MALE to the Computer.

25 PIN D-SUB MALE to the Modem

	Mac	Dir	Modem	
HSK <sub>o</sub>	1	→	4	RTS
HSK <sub>i</sub>	2	←	5	CTS
TxD-	3	→	2	TxD
RxD-	5	←	3	RxD
GND+RxD+	4+8	-	7	GND
			6+20	DSR+DTR

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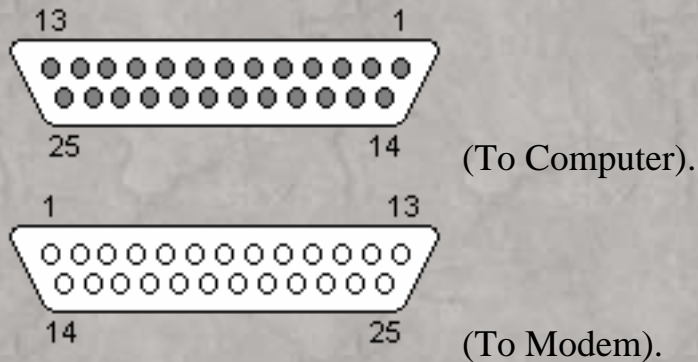
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# Modem (25-25)

This cable should be used for [DTE to DCE](#) (for instance computer to modem) connections with hardware handshaking.



25 PIN D-SUB FEMALE to the Computer

25 PIN D-SUB MALE to the Modem

	Female	Male	Dir
Shield Ground	1	1	—
Transmit Data	2	2	→
Receive Data	3	3	←
Request to Send	4	4	→
Clear to Send	5	5	←
Data Set Ready	6	6	←
System Ground	7	7	—
Carrier Detect	8	8	←
Data Terminal Ready	20	20	→
Ring Indicator	22	22	←

Contributor: [Joakim Ögren](#), [Søren Graversen](#)

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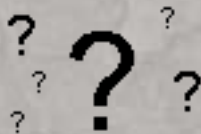


# Modem (9-15)

This cable should be used to connect an internal 14.4kbps Speedster modem to a computer.



(To Computer).



(at the modem)

9 PIN D-SUB FEMALE to the Computer  
15 PIN FEMALE ??? to the modem.

	9 pin	15 pin	Dir
Carrier Detect	1	11	←
Receive Data	2	13	←
Transmit Data	3	12	→
Data Terminal Ready	4	10	→
System Ground	5	1+8+15	—
Data Set Ready	6	3	←
Request to Send	7	4	→
Clear to Send	8	5	←
Ring Indicator	9	6	←

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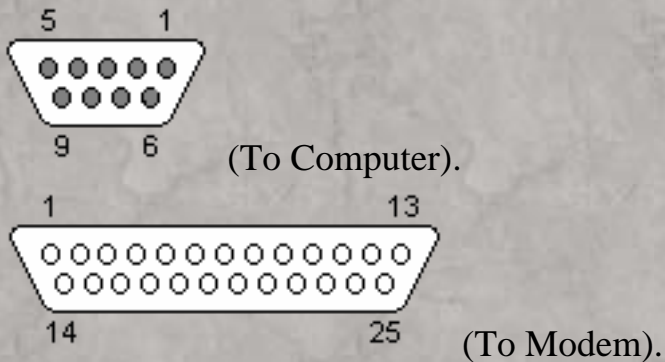
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# Modem (9-25)

This cable should be used for [DTE to DCE](#) (for instance computer to modem) connections with hardware handshaking.



9 PIN D-SUB FEMALE to the Computer

25 PIN D-SUB MALE to the Modem

	Female	Male	Dir
Shield		1	—
Transmit Data	3	2	→
Receive Data	2	3	←
Request to Send	7	4	→
Clear to Send	8	5	←
Data Set Ready	6	6	←
System Ground	5	7	—
Carrier Detect	1	8	←
Data Terminal Ready	4	20	→
Ring Indicator	9	22	←

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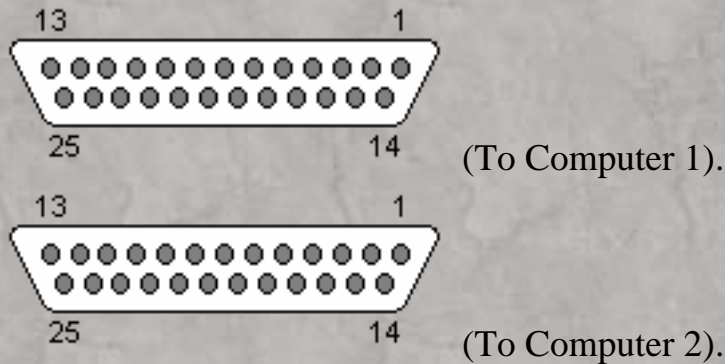
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# Nullmodem (25-25)

Use this cable between two [DTE](#) devices (for instance two computers).



25 PIN D-SUB FEMALE to Computer 1.

25 PIN D-SUB FEMALE to Computer 2.

	D-Sub 1	D-Sub 2	
Receive Data	3	2	Transmit Data
Transmit Data	2	3	Receive Data
Data Terminal Ready	20	6+8	Data Set Ready + Carrier Detect
System Ground	7	7	System Ground
Data Set Ready + Carrier Detect	6+8	20	Data Terminal Ready
Request to Send	4	5	Clear to Send
Clear to Send	5	4	Request to Send

*Note: DSR & CD are jumpered to fool the programs to think that they are online.*

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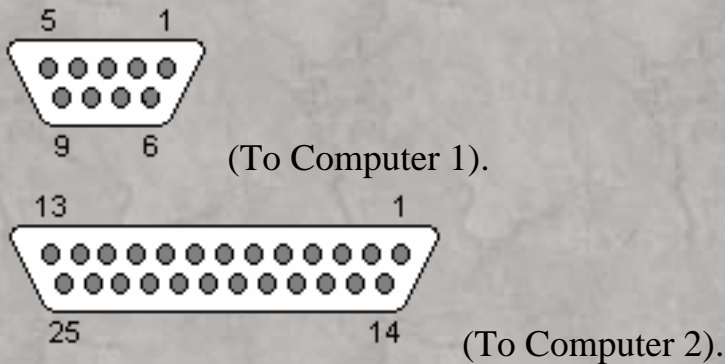
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# Nullmodem (9-25)

Use this cable between two [DTE](#) devices (for instance two computers).



9 PIN D-SUB FEMALE to Computer 1.

25 PIN D-SUB FEMALE to Computer 2.

	D-Sub 9	D-Sub 25	
Receive Data	2	2	Transmit Data
Transmit Data	3	3	Receive Data
Data Terminal Ready	4	6+8	Data Set Ready + Carrier Detect
System Ground	5	7	System Ground
Data Set Ready + Carrier Detect	6+1	20	Data Terminal Ready
Request to Send	7	5	Clear to Send
Clear to Send	8	4	Request to Send

*Note: DSR & CD are jumpered to fool the programs to think that they are online.*

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# Nullmodem (9-9)

Use this cable between two [DTE](#) devices (for instance two computers).



(To Computer 1).



(To Computer 2).

9 PIN D-SUB FEMALE to Computer 1.

9 PIN D-SUB FEMALE to Computer 2.

	D-Sub 1	D-Sub 2	
Receive Data	2	3	Transmit Data
Transmit Data	3	2	Receive Data
Data Terminal Ready	4	6+1	Data Set Ready + Carrier Detect
System Ground	5	5	System Ground
Data Set Ready + Carrier Detect	6+1	4	Data Terminal Ready
Request to Send	7	8	Clear to Send
Clear to Send	8	7	Request to Send

*Note: DSR & CD are jumpered to fool the programs to think that they are online.*

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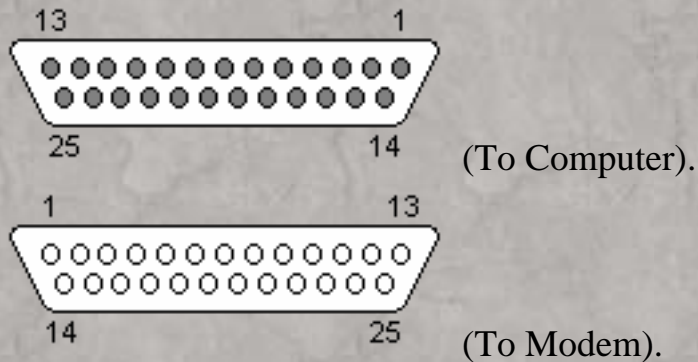
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# Two-Wire Modem (25-25)

This cable should be used for [DTE to DCE](#) (for instance computer to modem) connections without hardware handshaking.





25 PIN D-SUB FEMALE to the Computer

25 PIN D-SUB MALE to the Modem

	Female	Male	Dir
Shield Ground	1	1	
Transmit Data	2	2	→
Receive Data	3	3	←
System Ground	7	7	
<b>Jumper these:</b>			
Request to Send	4		→
Clear to Send	5		←
Data Set Ready	6		←
Carrier Detect	8		←
Data Terminal Ready	20		→
Request to Send		4	→
Clear to Send		5	←
Data Set Ready		6	←



Carrier Detect	8	
Data Terminal Ready	20	

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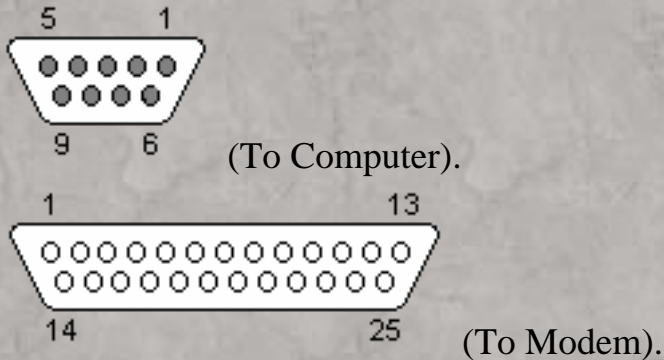
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# Two-Wire Modem (9-25)

This cable should be used for [DTE to DCE](#) (for instance computer to modem) connections without hardware handshaking.



9 PIN D-SUB FEMALE to the Computer

25 PIN D-SUB MALE to the Modem

	Female	Male	Dir
Shield Ground		1	
Transmit Data	3	2	→
Receive Data	2	3	←
System Ground	5	7	
<b>Jumper these:</b>			
Request to Send	7		→
Clear to Send	8		←
Data Set Ready	6		←
Carrier Detect	1		←
Data Terminal Ready	4		→
Request to Send		4	→
Clear to Send		5	←
Data Set Ready		6	←

Carrier Detect	8	
Data Terminal Ready	20	

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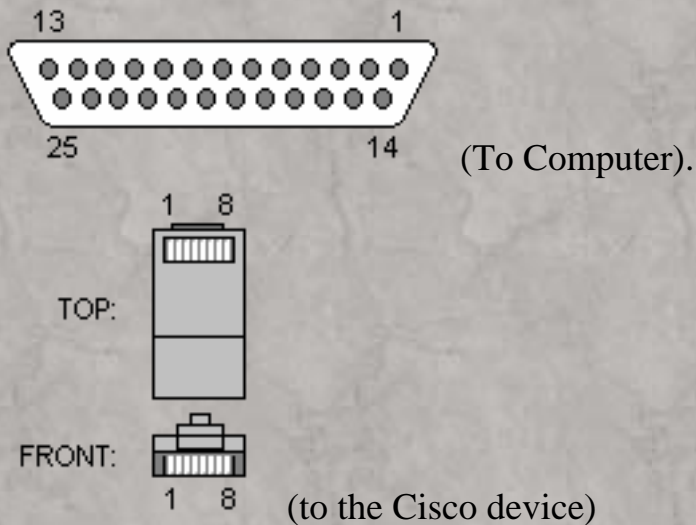
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# Cisco Console (25)

Use this cable to configure a Cisco device using the Console port.



25 PIN D-SUB FEMALE to the Computer  
RJ45 MALE CONNECTOR to the Cisco device.

	DB25F	RJ45	Dir
Shield Ground	1		—
Transmit Data	2	6	→
Receive Data	3	3	←
Request to Send	4	8	→
Clear to Send	5	1	←
Data Set Ready	6	2	←
Ground	7	4	—
Ground	7	5	—
Data Terminal Ready	20	7	→

Contributor: [Joakim Ögren](#), [Damien Miller](#) [Dave Peverley](#)

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*Cisco Catalyst 1900 Series Installation and Configuration Guide v9.x*

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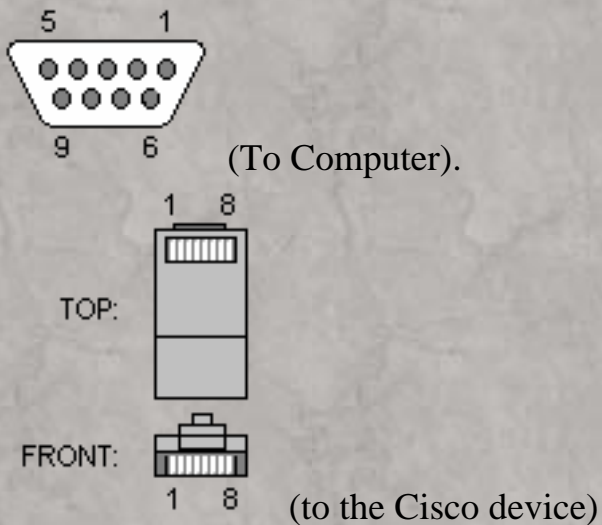
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# Cisco Console (9)

Use this cable to configure a Cisco device using the Console port.



9 PIN D-SUB FEMALE to the Computer  
RJ45 MALE CONNECTOR to the Cisco device.

	DB9F	RJ45	Dir
Receive Data	2	3	←
Transmit Data	3	6	→
Data Terminal Ready	4	7	→
Ground	5	4	—
Ground	5	5	—
Data Set Ready	6	2	←
Request to Send	7	8	→
Clear to Send	8	1	←

Contributor: [Joakim Ögren](#), [Damien Miller](#) [Dave Peverley](#)

Source:  
Cisco Catalyst 1900 Series Installation and Configuration Guide v9.x

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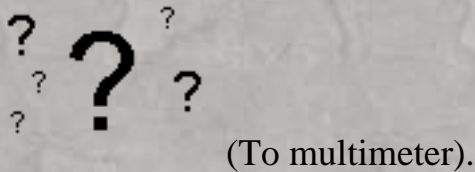
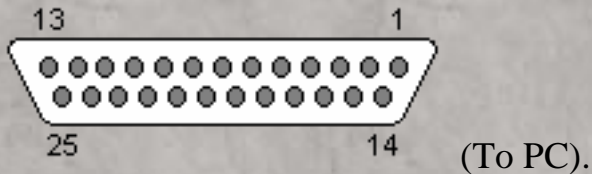
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*Document last modified: 2001-06-28*



# Conrad Electronics MM3610D (25)

Use this cable to connect a Conrad Electronics Multimeter 3610D to a PC:s serialport.



25 PIN D-SUB FEMALE to PC.

5 PIN UNKNOWN CONNECTOR to the multimeter

	PC	Conrad	Dir
Request To Send	4	1	→
Receive Data	3	2	←
Transmit Data	2	3	→
Data Terminal Ready	20	4	→
Ground	7	5	—

Contributor: [Joakim Ögren](#), [Anselm Belz](#)

Source:  
?

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Document last modified: 2001-06-07



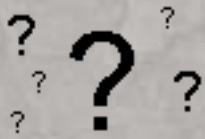


# Conrad Electronics MM3610D (9)

Use this cable to connect a Conrad Electronics Multimeter 3610D to a PC:s serialport.



(To PC).



(To multimeter).

9 PIN D-SUB FEMALE to PC.

5 PIN UNKNOWN CONNECTOR to the multimeter

	PC	Conrad	Dir
Request To Send	7	1	→
Receive Data	2	2	←
Transmit Data	3	3	→
Data Terminal Ready	4	4	→
Ground	5	5	—

Contributor: [Joakim Ögren](#), [Anselm Belz](#)

Source:

?

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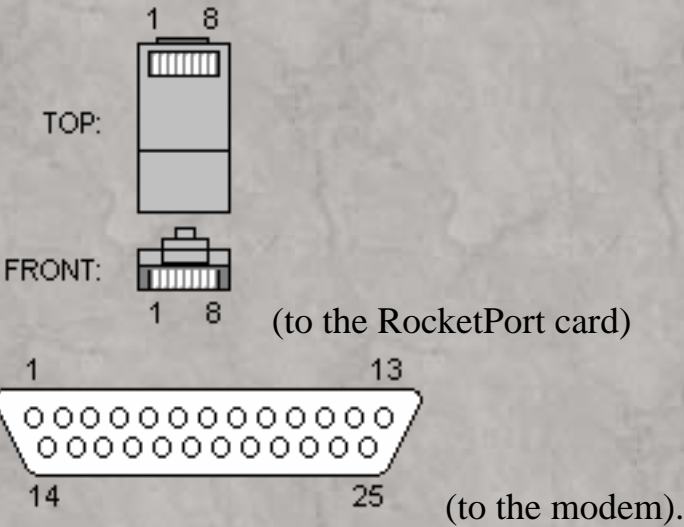
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Document last modified: 2001-06-08



# RocketPort Serial (25)

Use this cable to connect a RocketPort serialport card to a modem.



RJ45 MALE CONNECTOR to the RocketPort card.  
25 PIN D-SUB MALE to the modem

Description	RJ45	D-Sub	Dir
Request To Send	1	4	→
Data Terminal Ready	2	20	→
Ground	3	7	→
Tranceive Data	3	2	→
Receive Data	6	3	←
Data Carrier Detect	6	8	←
Data Set Ready	7	6	←
Clear To Send	8	5	←

Contributor: [Joakim Ögren](#), [Karl Asha](#)

Source:  
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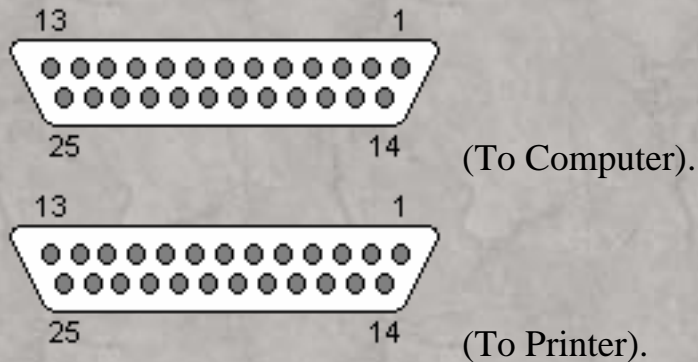
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*Document last modified: 2001-06-07*



# Serial Printer (25-25)

Use this cable between two a computer ([DTE](#)) and a printer ([DTE](#)) devices.



25 PIN D-SUB FEMALE to Computer.

25 PIN D-SUB FEMALE to Printer.

	D-Sub 1	D-Sub 2	
Receive Data	2	3	Transmit Data
Transmit Data	3	2	Receive Data
Clear To Send + Data Set Ready	5 + 6	20	Data Terminal Ready
Carrier Detect + Data Terminal Ready	8 + 20		
Ground	7	7	Ground

Contributor: [Joakim Ögren](#)

Source:

?

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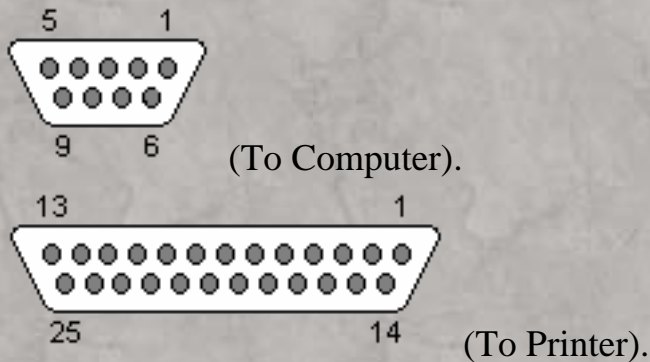
Document last modified: 2001-06-08





# Serial Printer (9-25)

Use this cable between two a computer ([DTE](#)) and a printer ([DTE](#)) devices.



9 PIN D-SUB FEMALE to Computer.

25 PIN D-SUB FEMALE to Printer.

	D-Sub 1	D-Sub 2	
Receive Data	3	3	Transmit Data
Transmit Data	2	2	Receive Data
Clear To Send + Data Set Ready	8 + 6	20	Data Terminal Ready
Carrier Detect + Data Terminal Ready	1 + 4		
Ground	5	7	Ground

Contributor: [Joakim Ögren](#)

Source:

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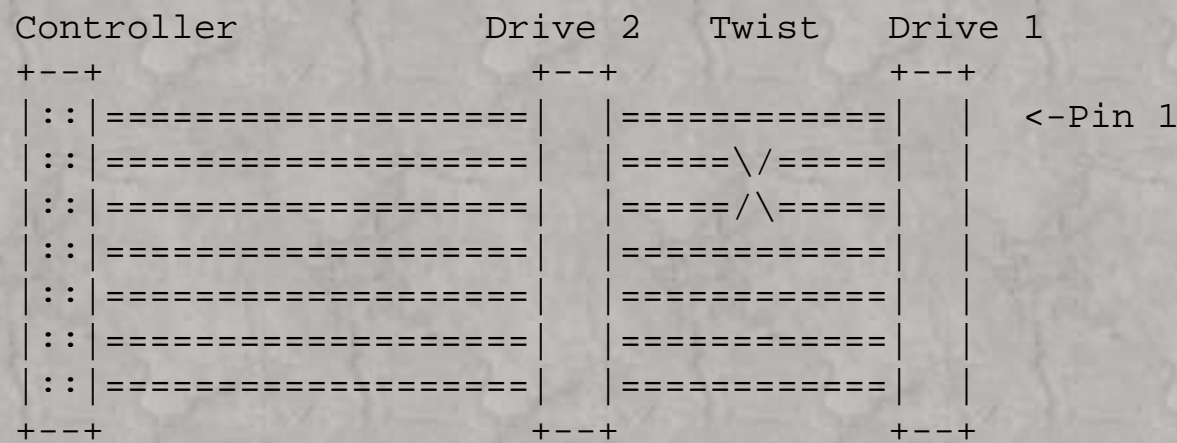


# Floppy

The original floppy cable required that each drive was jumpered to the right ID. But IBM come up with an idea to avoid jumpering the floppies.

If wire 10-16 are twisted before the last connector the jumpering is avoided. Each drive should be jumpered to act as Drive 2. If only one drive is used then leave the middle connector free.

The IDC could also be an edge connector on some old drives.



2 34

(to the Controller)



2 34

(to the Drive 2)



2 34

(to the Drive 1)

34 PIN IDC FEMALE to the Controller.

34 PIN IDC FEMALE to the Drive 2.

34 PIN IDC FEMALE to the Drive 1.

Controller Drive 1 Drive 2

Wire 1-9	1-9	1-9	1-9
Wire 10	10	16	10
Wire 11	11	15	11
Wire 12	12	14	12
Wire 13	13	13	13
Wire 14	14	12	14
Wire 15	15	11	15
Wire 16	16	10	16
Wire 17-34	17-34	17-34	17-34

*Contributor:* [Joakim Ögren](#)

*Source:*  
[TheRef TechTalk](#)

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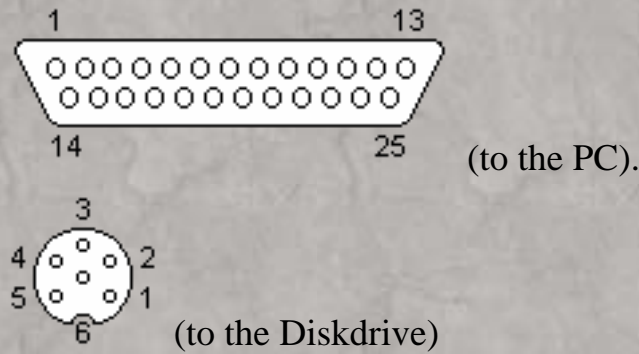
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*Document last modified:* 2001-06-08



# X1541

Used to transfer data from a Commodore 1541/1581 diskdrive to a PC. The X1541 software is written by [Leopoldo Ghielmetti](#).



25 PIN D-SUB MALE to the PC.  
6 PIN DIN (DIN45322) MALE to the Cable

	PC	Diskdrive	
GND	18-25	2	GND
STROBE	1	3	ATN
AUTOFEED	14	4	CLOCK
SELECTIN	17	5	DATA
INIT	16	6	RESET

Contributor: [Joakim Ögren](#), [Magnus Eriksson](#)

Source:  
*X1541 documentation*

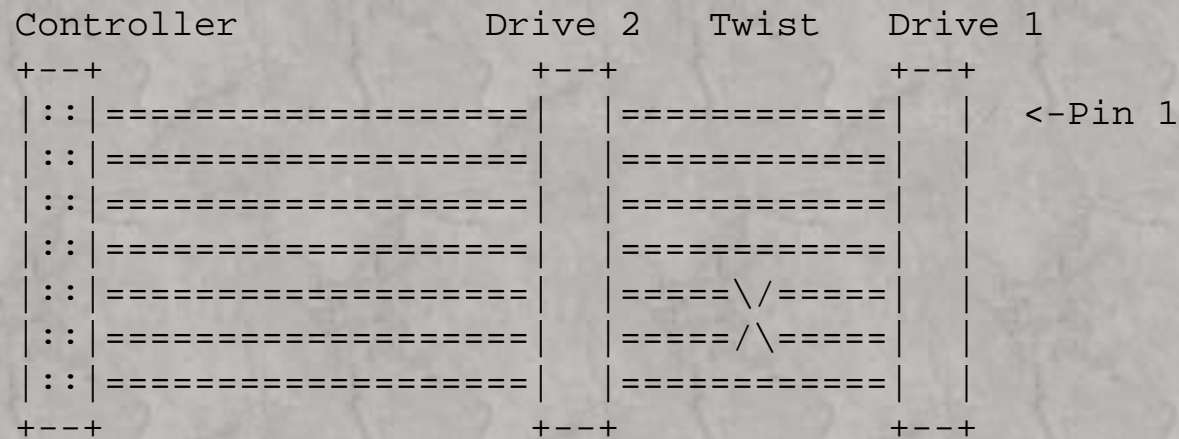
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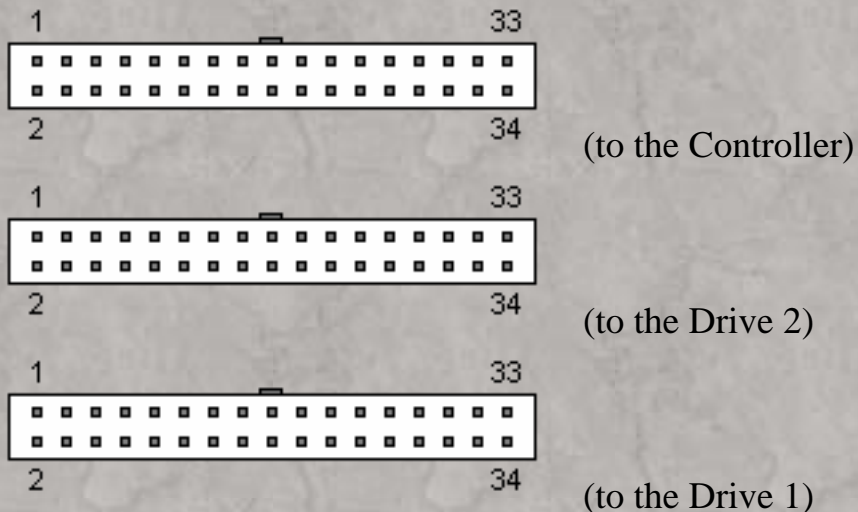


# ESDI

The ESDI interface requires two cables, one for control and one for data. The control cable is shared between the two drives. But each drive has each own data cable. By twisting some wires on the control cable it won't be necessary to set the ID for each drive, since the twist will do the job. Wires 25 to 29 should be twisted between drive 1 & drive 2.



## Control cable



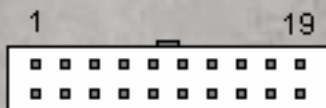
34 PIN IDC FEMALE to the Controller.  
 34 PIN IDC FEMALE to the Drive 2.  
 34 PIN IDC FEMALE to the Drive 1.

	Controller	Drive 1	Drive 2
Wire 1-24	1-9	1-9	1-9
Wire 25	25	29	25
Wire 26	26	28	26
Wire 27	27	27	27
Wire 28	28	26	28
Wire 29	29	25	29
Wire 30-34	30-34	30-34	30-34

## Data cable



(to the Controller)



(to the Drive)

20 PIN IDC FEMALE to the Controller.

20 PIN IDC FEMALE to the Drive.

	Controller	Drive
Wire 1-20	1-20	1-20

Contributor: [Joakim Ögren](#)

Source:

[TheRef TechTalk](#)

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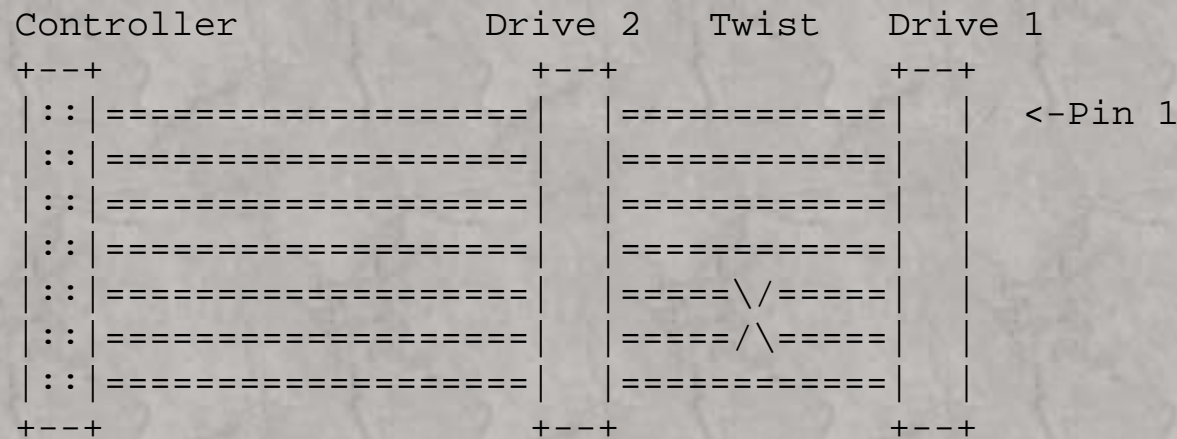
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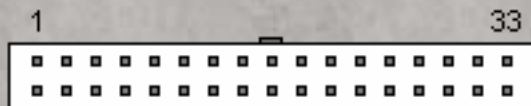


# ST506/412

The ST506/412 interface requires two cables, one for control and one for data. The control cable is shared between the two drives. But each drive has each own data cable. By twisting some wires on the control cable it won't be necessary to set the ID for each drive, since the twist will do the job. Wires 25 to 29 should be twisted between drive 1 & drive 2.

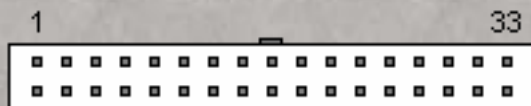


## Control cable



2 34

(to the Controller)



2 34

(to the Drive 2)



2 34

(to the Drive 1)

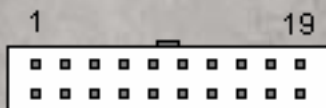
- 34 PIN IDC FEMALE to the Controller.
- 34 PIN IDC FEMALE to the Drive 2.
- 34 PIN IDC FEMALE to the Drive 1.

	Controller	Drive 1	Drive 2
Wire 1-24	1-9	1-9	1-9
Wire 25	25	29	25
Wire 26	26	28	26
Wire 27	27	27	27
Wire 28	28	26	28
Wire 29	29	25	29
Wire 30-34	30-34	30-34	30-34

## Data cable



(to the Controller)



(to the Drive)

20 PIN IDC FEMALE to the Controller.

20 PIN IDC FEMALE to the Drive.

	Controller	Drive
Wire 1-20	1-20	1-20

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Source:

[TheRef TechTalk](#)

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# IDE

The IDE interface requires only one cable. All pins straight from 1 to 1, 2 to 2 and so on. The drives can be connected in any order. Only remember that one should be jumpered as Master and the other as Slave. If only one drive is used, jumper it as Single (if such a mode exists, or most common Master else).



(to the Controller)



(to the Drive 1)



(to the Drive 2)

40 PIN IDC FEMALE to the Controller.  
 40 PIN IDC FEMALE to the Drive 1.  
 40 PIN IDC FEMALE to the Drive 2.

	Controller	Drive 1	Drive 2
Wire 1-40	1-40	1-40	1-40

*Contributor:* [Joakim Ögren](#)

*Source:*  
?

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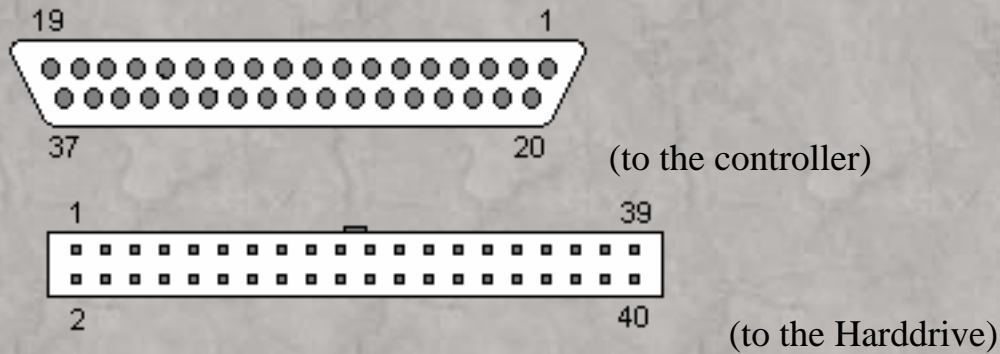
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*Document last modified:* 2001-06-07



# Paravision SX1 to IDE

Can be used to connect a normal IDE harddisk to the Paravision SX1. Paravision was formerly known as Microbotics.



37 PIN D-SUB FEMALE to the controller.

40 PIN IDC FEMALE to the harddisk.

Description	D-Sub	IDC
Drive Reset	1	1
Data bit 0	2	17
Data bit 2	3	13
Data bit 4	4	9
Data bit 6	5	5
Ground	6	2
Data bit 8	7	4
Data bit 10	8	8
Data bit 12	9	12
Data bit 14	10	16
Ground	11+12	19
Ground	13+14	22
Ground	15+16	24
Ground	17	26

5V Power	18	n/c
5V Power	19	n/c
Ground	20	30
Data bit 1	21	21
Data bit 3	22	22
Data bit 5	23	23
Data bit 7	24	24
Ground	25	40
Data bit 9	26	26
Data bit 11	27	27
Data bit 13	28	28
Data bit 15	29	29
I/O Write	30	23
I/O Read	31	25
Interrupt Request	32	31
Address bit 2	33	36
Address bit 1	34	33
Address bit 0	35	35
Chip Select 1	36	38
Chip Select 0	37	37

*Note: Pin 18+19 (+5V) can be used to power the harddisk. But most harddisks require both +5V and +12V.*

*Contributor: [Joakim Ögren](#)*

*Source:  
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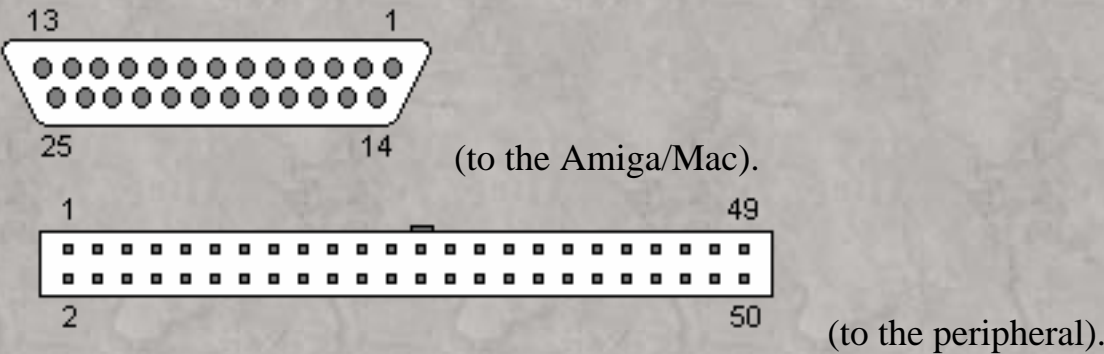
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# SCSI Cable (Amiga/Mac)



25 PIN D-SUB FEMALE to the Amiga/Mac.  
50 PIN IDC FEMALE to the peripheral.

	DSub	IDC
Request	1	48
Message	2	42
Input/Output	3	50
Reset	4	40
Acknowledge	5	38
Busy	6	36
Data Bus 0	8	2
Data Bus 3	10	8
Data Bus 5	11	12
Data Bus 6	12	14
Data Bus 7	13	16
Control/Data	15	46
Attention	17	32
Select	19	44
Data Parity	20	18
Data Bus 1	21	4

Data Bus 2	22	6
Data Bus 4	23	10
Termination Power	25	26

*Note: All the other pins (7+9+14+16+18+24) at the DSub should be connected to the all odd pins except 25 at the IDC connector.*

*Contributor:* [Joakim Ögren](#)

*Source:*  
?

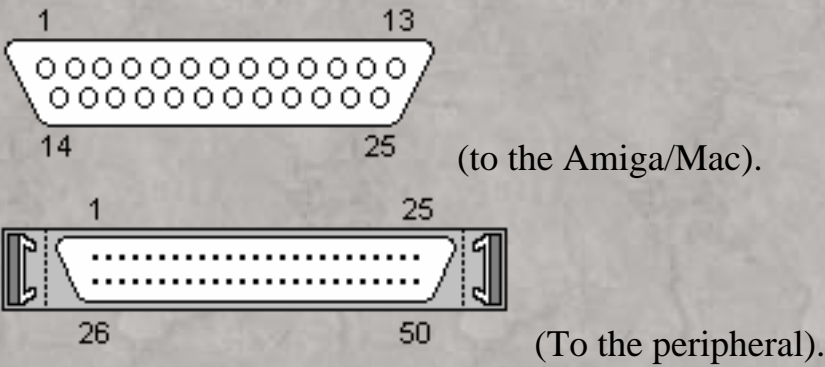
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# SCSI Cable (D-Sub to Hi D-Sub)



25 PIN D-SUB MALE to the Amiga/Mac.  
50 PIN HI-DENSITY D-SUB MALE to the peripheral.

	DSub	Hi DSub
Request	1	49
Message	2	46
Input/Output	3	50
Reset	4	45
Acknowledge	5	44
Busy	6	43
Data Bus 0	8	26
Data Bus 3	10	29
Data Bus 5	11	31
Data Bus 6	12	32
Data Bus 7	13	33
Control/Data	15	48
Attention	17	41
Select	19	47
Data Parity	20	34
Data Bus 1	21	27

Data Bus 2	22	28
Data Bus 4	23	30
Termination Power	25	38

*Note: All the other pins (7+9+14+16+18+24) at the DSub should be connected to pins 1-25 at the Hi-density D-Sub connector.*

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What does the information that is listed for each adapter mean? See the [tutorial](#).

## Audio/Video

### Video

[Macintosh Video to VGA](#)

## Parallel

### Parallel

[A1000 to Amiga Parallel](#)

[Centronics to LapLink](#)

## Serial

### Mouse

[PS/2 to Serial Mouse](#)

[Serial to PS/2 Mouse](#)

### Serial

[9 to 25 Serial](#)

[Nullmodem](#)

[Serial to PS/2 Mouse](#)

## Mice/Keyboards/Joysticks

### Joystick

[Amiga 4 Joysticks](#)

[PC 2 Joysticks](#)

## Keyboard

[DIN to Mini-DIN Keyboard](#)

[Mini-DIN to DIN Keyboard](#)

[PS/2 Keyboard \(Gateway\) Y](#)

[PS/2 Keyboard \(IBM Thinkpad\) Y](#)

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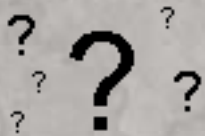
# Short tutorial

## Heading

First at each page there a short heading describing the adapter.

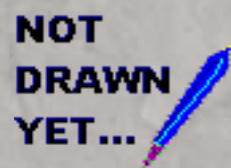
## Pictures of the connectors

After that there is at each page there is one or more pictures of the connectors, usually there's two connectors. Sometimes there is some question marks only. This means that we don't know what kind of connector it is or how it looks.



(to the computer)

There may be some pictures haven't been drawn yet. This is illustrated with the following advanced picture:

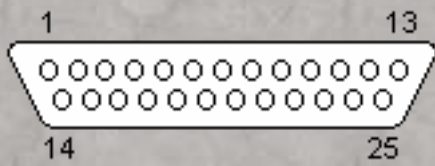


(to the computer)

Normally are one or more pictures. **These are seen from the front, and NOT the soldside. Holes (female connectors usually) are darkened.** Look at the example below. The first is a female connector and the send a male. The texts inside parentheses will tell you at which kind of the device it will look like that.



(to the Computer).



(to the Serialcable).

## Texts describing the connectors

Below the pictures there is texts that describes the connectors. Including the name of the physical connector.

9 PIN D-SUB FEMALE to the Computer.

25 PIN D-SUB MALE to the Serialcable.

## Pin table

The pin table is perhaps the information you are looking for. It should be quite simple to read. Contains mostly the following three columns; Name, Pin 1, Pin 2. Sometimes when not the same pin is connected to each side there is another column describing the name at connector 2.

	9-Pin	25-Pin
Carrier Detect	1	8
Receive Data	2	3
Transmit Data	3	2
Data Terminal Ready	4	20
System Ground	5	7
Data Set Ready	6	6
Request to Send	7	4
Clear to Send	8	5
Ring Indicator	9	22

## Contributor & Source

All persons that helped us or sent us information about the connector will be listed here. The source of the information is perhaps a book or another site.

Contributor: [Joakim Ögren](#)



*Source: Amiga 4000 User's Guide from Commodore*

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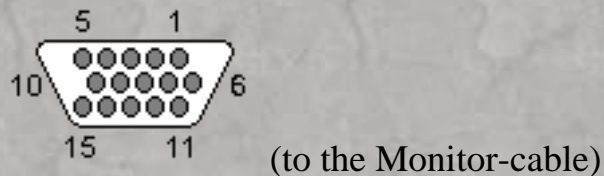
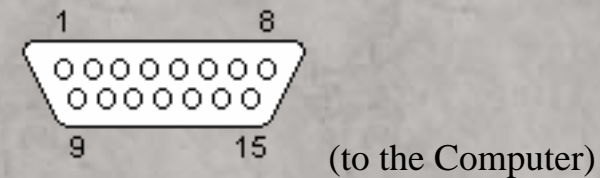
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# Macintosh Video to VGA

Use this adapter to connect a standard VGA (or higher) monitor to your Apple Macintosh.



15 PIN D-SUB MALE to the Computer.

15 PIN HIGHDENSITY D-SUB FEMALE to the Monitor-cable.

Description	Mac	VGA	Dir
Red Ground	1	6	—
Red	2	1	→
Composite sync	3	13	→
Monitor Sense 0	4	4	←
Green	5	2	→
Green Ground	6	7	—
Monitor Sense 1	7	11	←
No connection	8	n/c	
Blue	9	3	→
Monitor sense 2	10	12	←
Sync Ground	11	10	—
Vertical Sync	12	14	→
Blue Ground	13	8	—
Horizontal Sync Ground	14	n/c	

Horizontal Sync	15	n/c	
-----------------	----	-----	--

*Contributor:* [Joakim Ögren](#), [Michael Van den Acker](#)

*Source:*  
?

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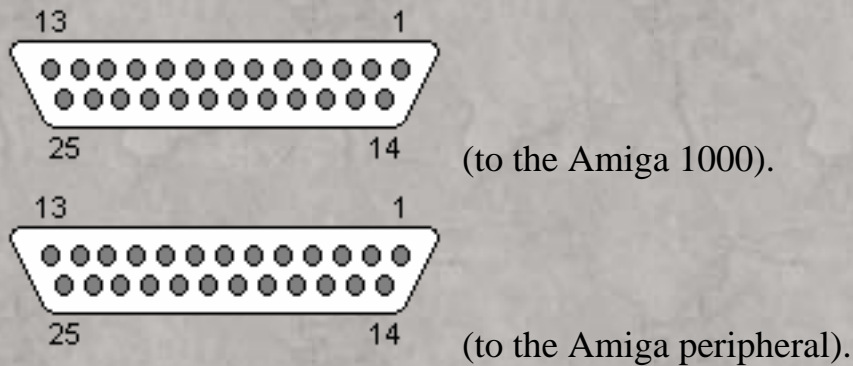
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# A1000 to Amiga Parallel

This adapter will enable you to connect normal Amiga peripherals to an Amiga 1000. The Amiga 1000 has a male connector at the computer instead of a normal female connector. And some signals has changed places.



25 PIN D-SUB FEMALE to the Amiga 1000.

25 PIN D-SUB FEMALE to the Amiga peripheral.

	A1000	Amiga
Ground	14	23
Ground	15	24
Ground	16	25
+5V	23	14
n/c	24	15
Reset	25	16

All other straight over, 1 to 1, 2 to 2...

Contributor: [Joakim Ögren](#)

Source:  
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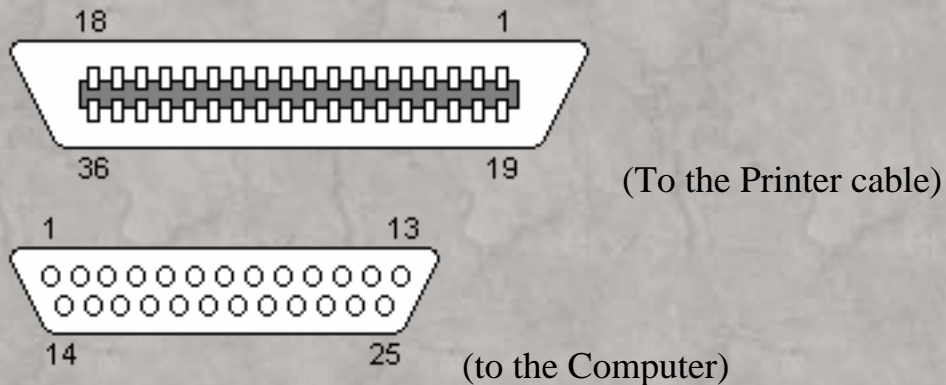


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Document last modified: 2001-06-07*



# Centronics to LapLink

This adapter will allow you to use a normal printercable (Centronics) as a LapLink/InterLink cable.



36 PIN CENTRONICS FEMALE to the Printer cable.

25 PIN D-SUB MALE to the Computer.

Name	36-Cen	25-DSub	Name
Data Bit 0	2	15	Error
Data Bit 1	3	13	Select
Data Bit 2	4	12	Paper Out
Data Bit 3	5	10	Acknowledge
Data Bit 4	6	11	Busy
Acknowledge	10	5	Data Bit 3
Busy	11	6	Data Bit 4
Paper Out	12	4	Data Bit 2
Select	13	3	Data Bit 1
Error	32	2	Data Bit 0
Reset	16	16	Reset
Select	17	17	Select
Signal Ground	19-30+33	18-25	Signal Ground

*Contributor:* [Joakim Ögren](#), [Petr Krc](#)

*Source:*

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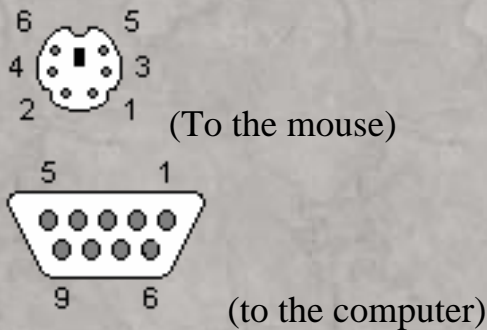
*Document last modified: 2001-06-07*



# PS/2 to Serial Mouse

This adapter will enable you to use a mouse with a 6 pin Mini-DIN (PS/2) connector to a computer with a 9 pin D-SUB (Serial) connector.

*This requires that the mouse handles both protocols. A mouse like this is sometimes referred to as a combo-mouse.*



6 PIN MINI-DIN FEMALE to the mouse.

9 PIN D-SUB FEMALE to the computer.

	Mini-DIN	D-SUB	
GND	3	5	GND
RxD	2	2	RxD
TxD	6	3	TxD
+5V	4	7	RTS

Contributor: [Joakim Ögren](#), [Tomas Ögren](#), [Thomas Eschenbacher](#)

Source:

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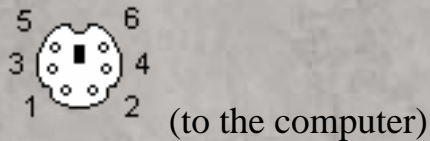
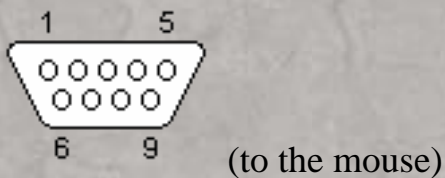




# Serial to PS/2 Mouse

This adapter will enable you to use a mouse with a 9 pin D-SUB (Serial) connector to a computer with a 6 pin Mini-DIN (PS/2) connector.

*This requires that the mouse handles both protocols. A mouse like this is sometimes referred to as a combo-mouse.*



9 PIN D-SUB MALE to the mouse.

6 PIN MINI-DIN MALE to the computer.

	Mini-DIN	D-SUB	
+5V	4	4+7+9	DTR+RTS+RI
Data	1	1	CD
Gnd	3	3+5	TXD+GND
Clock	5	6	DSR

Contributor: [Joakim Ögren](#), [Tomas Ögren](#), [Thomas Eschenbacher](#)

Source:

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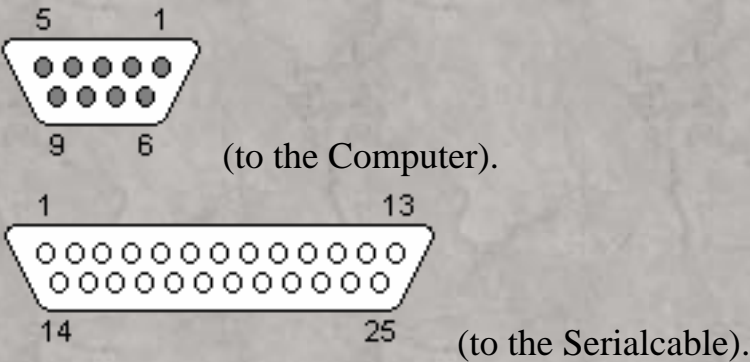
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# 9 to 25 Serial

This adapter will enable you to connect a 25 pin serialcable to a 9 pin connector at the computer.



9 PIN D-SUB FEMALE to the Computer.  
25 PIN D-SUB MALE to the Serialcable.

	9-Pin	25-Pin
Carrier Detect	1	8
Receive Data	2	3
Transmit Data	3	2
Data Terminal Ready	4	20
System Ground	5	7
Data Set Ready	6	6
Request to Send	7	4
Clear to Send	8	5
Ring Indicator	9	22

Contributor: [Joakim Ögren](#)

Source:  
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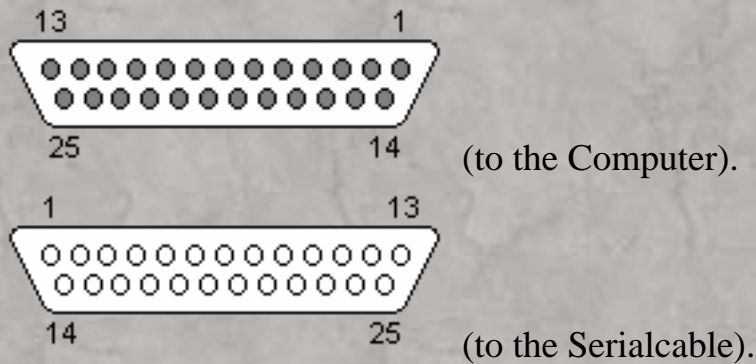
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# Nullmodem

This adapter will enable you to use a normal serialcable as a nullmodem.



25 PIN D-SUB FEMALE to the Computer.

25 PIN D-SUB MALE to the Serialcable.

	Female	Male	
Shield Ground	1	1	Shield Ground
Transmit Data	2	3	Receive Data
Receive Data	3	2	Transmit Data
Request to Send	4	5	Clear to Send
Clear to Send	5	4	Request to Send
Data Set Ready	6	20	Data Terminal Ready
Data Terminal Ready	20	6	Data Set Ready
Ground	7	7	Ground

Contributor: [Joakim Ögren](#)

Source:  
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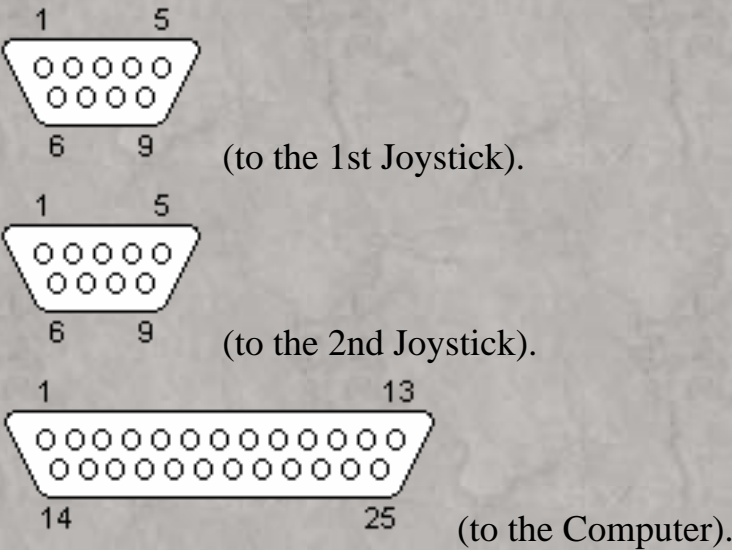
Document last modified: 2001-06-07





# Amiga 4 Joysticks

This adapter will make it possible to connect 2 extra joysticks to the Amiga. This requires that the game is aware of this Multi-Joystick Extender in order to use it. The adapter is connected to the parallelport of the Amiga.



- 9 PIN D-SUB MALE to the 1st Joystick.
- 9 PIN D-SUB MALE to the 2nd Joystick.
- 25 PIN D-SUB MALE to the Parallelcable.

	Parport	Joy 1	Joy 2
Up 1	2	1	
Down 1	3	2	
Left 1	4	3	
Right 1	5	4	
Up 2	6		1
Down 2	7		2
Left 2	8		3
Right 2	9		4
Fire 2	11		6

Fire 1	13	6	
Ground 2	18		8
Ground 1	19	8	

*Contributor:* [Joakim Ögren](#), [Rob Gill](#)

*Source:*  
[Tomi Engdahl's Joystick page](#)

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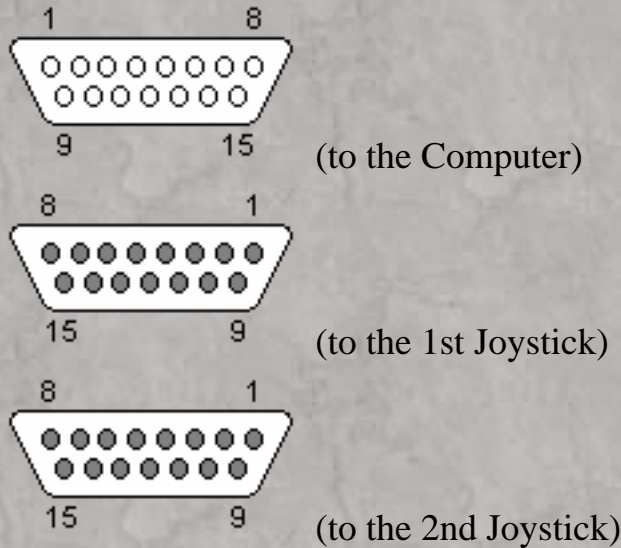
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# PC 2 Joysticks

This adapter will make it possible to connect 1 extra joystick to the PC. The gameport contains pins for two joysticks but you will need this adapter to be able to connect two joysticks to one connector.



15 PIN D-SUB MALE to the Computer.  
 15 PIN D-SUB FEMALE to the 1st Joystick.  
 15 PIN D-SUB FEMALE to the 2nd Joystick.

	PC	Joy 1	Joy 2
+5 VDC	1	1	-
Button 1	2	2	
Joystick 1 - X	3	3	
Ground	4	4	4
Ground	5	5	5
Joystick 1 - Y	6	6	
Button 2	7	7	
+5 VDC	8	8	
+5 VDC	9	9	1
Button 4	10	10	2

Joystick 2 - X	11	11	3
Ground	12	12	
Joystick 2 - Y	13	13	6
Button 3	14	14	7
+5 VDC	15	15	8

*Note: Since pin 12 is often used for MIDI-signals on gameport equipped soundcards it's better to use the ground from pin 4 & 5, pin 15 is also used for MIDI-signals...*

*Contributor:* [Joakim Ögren](#)

*Source:*  
[Tomi Engdahl's Joystick page](#)

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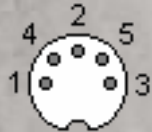
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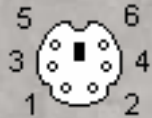


# DIN to Mini-DIN Keyboard

This adapter will enable you to use a keyboard with a 5 pin DIN connector to a computer with a 6 pin Mini-DIN connector.



(to the keyboard)



(to the computer)

5 PIN DIN 180° (DIN41524) FEMALE to the keyboard.

6 PIN MINI-DIN MALE (PS/2 STYLE) to the computer.

	DIN	Mini-DIN
Shield	Shield	Shield
Clock	1	5
Data	2	1
Ground	4	3
+5 VDC	5	4

Contributor: [Joakim Ögren](#), [Gilles Ries](#)

Source:  
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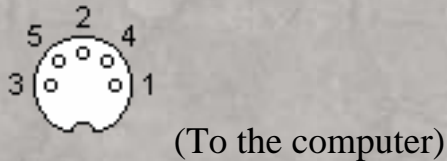
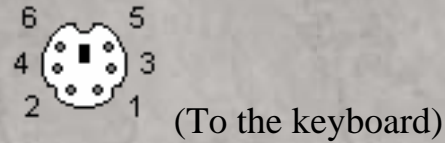
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# Mini-DIN to DIN Keyboard

This adapter will enable you to use a keyboard with a 6 pin Mini-DIN connector to a computer with a 5 pin DIN connector.



6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the keyboard.

5 PIN DIN 180° (DIN41524) MALE to the computer.

	Mini-DIN	DIN
Shield	Shield	Shield
Data	1	2
Ground	3	4
+5 VDC	4	5
Clock	5	1

Contributor: [Joakim Ögren](#), [Gilles Ries](#)

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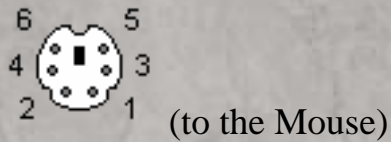
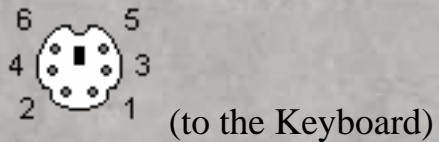
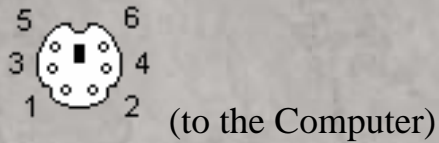
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# PS/2 Keyboard (Gateway) Y

This adapter will enable you to use a keyboard and mouse at the same time. For Gateway computer, may work with other computers (Let us know).



6 PIN MINI-DIN MALE (PS/2 STYLE) to the Computer.  
 6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the Keyboard.  
 6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the Mouse.

Computer	Keyboard	Mouse
1	2	-
2	-	2
3	3	3
4	4	4
5	6	-
6	-	6

Contributor: [Joakim Ögren](#), [Gilles Ries](#)

Source:  
[Tommy's pinout Collection](#) by [Tommy Johnson](#)

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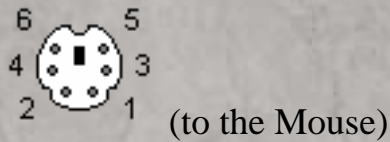
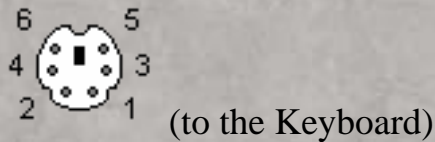
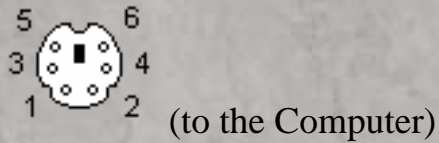
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# PS/2 Keyboard (IBM Thinkpad) Y

This adapter will enable you to use a keyboard and mouse at the same time. For IBM Thinkpad computer, may work with other computers (Let us know).



6 PIN MINI-DIN MALE (PS/2 STYLE) to the Computer.  
 6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the Keyboard.  
 6 PIN MINI-DIN FEMALE (PS/2 STYLE) to the Mouse.

Computer	Keyboard	Mouse
1	2	-
2	-	1,2
3	3	3
4	4	4
5	6	5
6	-	6

Contributor: [Joakim Ögren](#), [Gilles Ries](#)

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[ [Filter](#) | [Misc](#) | [Serial](#) ]

Need help with the circuits? See the [tutorial](#).

## Filter

[Active Filter: Bessel 12dB Highpass](#)

[Active Filter: Bessel 12dB Lowpass](#)

[Active Filter: Bessel 18dB Highpass](#)

[Active Filter: Bessel 18dB Lowpass](#)

[Active Filter: Bessel 24dB Highpass](#)

[Active Filter: Bessel 24dB Lowpass](#)

[Active Filter: Butterworth 12dB Highpass](#)

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[Active Filter: Butterworth 6dB Highpass](#)

[Active Filter: Butterworth 6dB Lowpass](#)

[Active Filter: Linkwitz 24dB Highpass](#)

[Active Filter: Linkwitz 24dB Lowpass](#)

## Misc

[Operation Amplifier: Addition](#)

[Operation Amplifier: Inverting Amplifier](#)

[Operation Amplifier: Non-inverting Amplifier](#)

## Serial

[C64 to RS232 Interface](#)

[CD32 Keyboard to Serial Interface 1](#)

## [CD32 Keyboard to Serial Interface 2](#)

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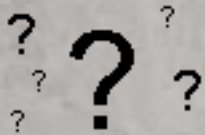
# Short tutorial

## Heading

First at each page there a short heading describing what the connector is.

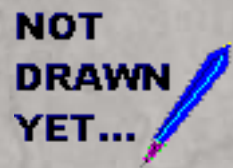
## Pictures of the connectors

After that there is at each page there is one or more pictures of the connectors. Sometimes there is some question marks only. This means that we don't know what kind of connector it is or how it looks.



(at the computer)

There may be some pictures we haven't drawn yet. We illustrate this with the following advanced picture:



(at the computer)

Normally are one or more pictures. **These are seen from the front, and NOT the soldside. Holes (female connectors usually) are darkened.** Look at the example below. The first is a female connector and the send a male. The texts inside parentheses will tell you at which kind of the device it will look like that.



(at the videocard)



(at the monitor cable)

## Texts describing the connectors

Below the pictures there is texts that describes the connectors. Including the name of the physical connector.

5 PIN DIN 180° (DIN41524) at the computer.

## Pin table

The pin table is perhaps the information you are looking for. Should be simple to read. Contains mostly the following three columns; Pin, Name & Description.

Pin	Name	Description
1	CLOCK	Key Clock
2	GND	GND
3	DATA	Key Data
4	VCC	+5 VDC
5	n/c	Not connected

## Contributor & Source

All persons that helped us or sent us information about the connector will be listed here. The source of the information is perhaps a book or another site.

Contributor: [Joakim Ögren](#)

Source: *Amiga 4000 User's Guide from Commodore*

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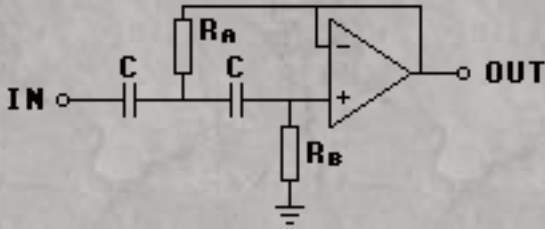
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# Active Filter: Bessel 12dB Highpass

## (2st order, 12 dB/octave, Highpass)



$C=4.7\text{n}-10\text{nF}$

$R_a=1.1017/(2*\pi*F_c*C)$

$R_b=1.4688/(2*\pi*F_c*C)$

Units:  $R_x$  [Ohm],  $C$  [F],  $F_c$  [Hz]

Contributor: [Joakim Ögren](#)

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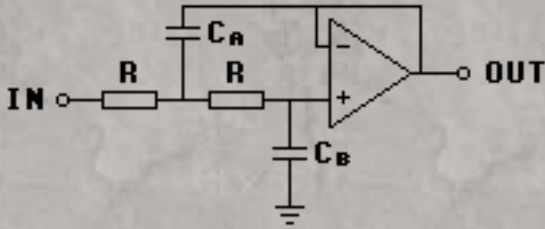
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# Active Filter: Bessel 12dB Lowpass

## (2nd order, 12 dB/octave, Lowpass)



$R=4.7k-10\text{ k}\Omega$

$C_A=0.9076/(2\pi F_c R)$

$C_B=0.6809/(2\pi F_c R)$

Units:  $R$  [ $\Omega$ ],  $C_x$  [F],  $F_c$  [Hz]

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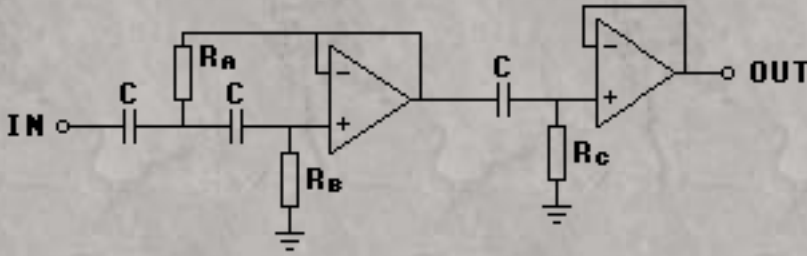
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# Active Filter: Bessel 18dB Highpass

## (3st order, 18 dB/octave, Highpass)



$$C=4.7\text{n}-10\text{nF}$$

$$R_a=1.0474/(2*\pi*F_c*C)$$

$$R_b=2.0008/(2*\pi*F_c*C)$$

$$R_c=1.3228/(2*\pi*F_c*C)$$

Units:  $R_x$  [Ohm],  $C$  [F],  $F_c$  [Hz]

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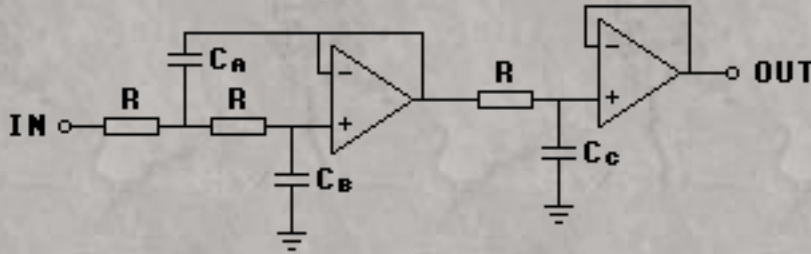
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# Active Filter: Bessel 18dB Lowpass

## (3st order, 18 dB/octave, Lowpass)



$R=4.7k-10\text{ k}\Omega$

$C_A=0.9548/(2\pi F_c R)$

$C_B=0.4998/(2\pi F_c R)$

$C_C=0.7560/(2\pi F_c R)$

Units:  $R$  [ $\Omega$ ],  $C_x$  [F],  $F_c$  [Hz]

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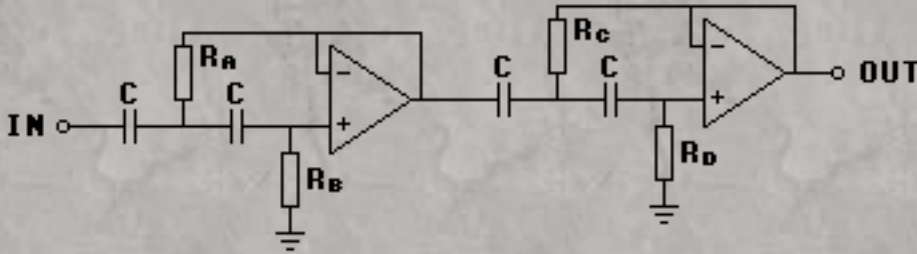
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# Active Filter: Bessel 24dB Highpass

## (4th order, 24 dB/octave, Highpass)



$$C=4.7\text{n}-10\text{nF}$$

$$R_a=1.3701/(2*\pi*F_c*C)$$

$$R_b=1.4929/(2*\pi*F_c*C)$$

$$R_c=0.9952/(2*\pi*F_c*C)$$

$$R_d=2.5830/(2*\pi*F_c*C)$$

Units:  $R_x$  [Ohm],  $C$  [F],  $F_c$  [Hz]

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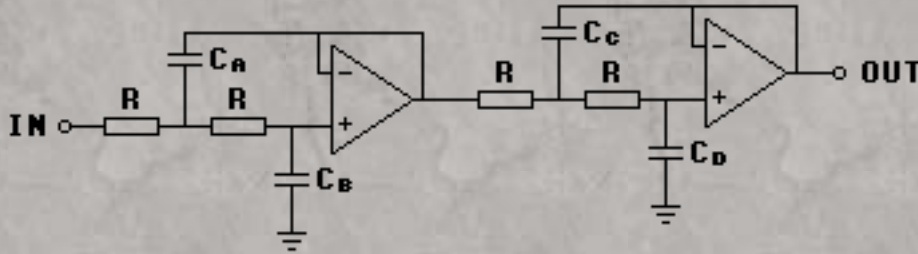
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# Active Filter: Bessel 24dB Lowpass

## (4th order, 24 dB/octave, Lowpass)



$R=4.7k-10\text{ k}\Omega$

$C_A=0.7298/(2\pi F_c R)$

$C_B=0.6699/(2\pi F_c R)$

$C_C=1.0046/(2\pi F_c R)$

$C_D=0.3872/(2\pi F_c R)$

Units:  $R$  [ $\Omega$ ],  $C_x$  [F],  $F_c$  [Hz]

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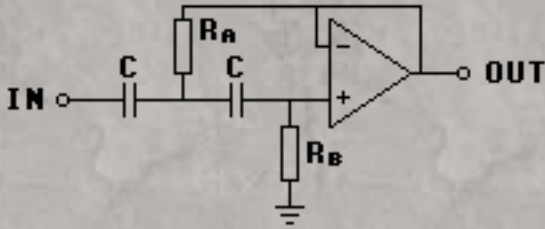
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# Active Filter: Butterworth 12dB Highpass

## (2st order, 12 dB/octave, Highpass)



$$C=4.7\text{n}-10\text{nF}$$

$$R_a=0.7071/(2*\pi*F_c*C)$$

$$R_b=1.414/(2*\pi*F_c*C)$$

Units:  $R_x$  [Ohm],  $C$  [F],  $F_c$  [Hz]

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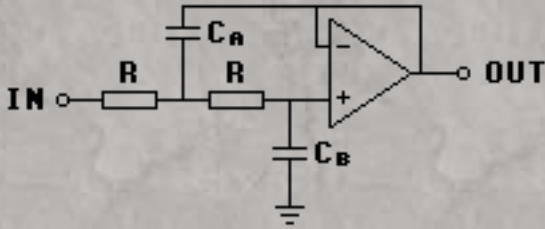
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# Active Filter: Butterworth 12dB Lowpass

## (2nd order, 12 dB/octave, Lowpass)



$R=4.7k-10\text{ k}\Omega$

$C_a=1.414/(2*\pi*F_c*R)$

$C_b=0.7071/(2*\pi*F_c*R)$

Units:  $R$  [ $\Omega$ ],  $C_x$  [F],  $F_c$  [Hz]

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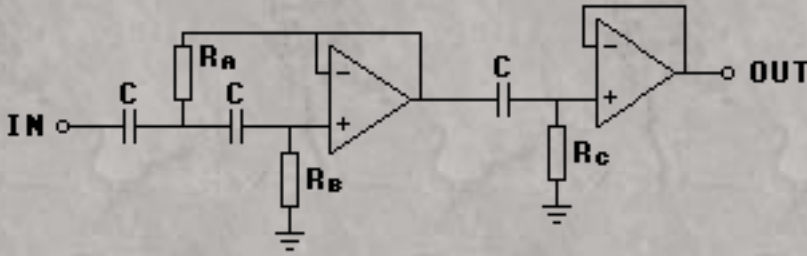
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# Active Filter: Butterworth 18dB Highpass

## (3st order, 18 dB/octave, Highpass)



$$C=4.7\text{n}-10\text{nF}$$

$$R_a=0.500/(2*\pi*F_c*C)$$

$$R_b=2.000/(2*\pi*F_c*C)$$

$$R_c=1.000/(2*\pi*F_c*C)$$

Units:  $R_x$  [Ohm],  $C$  [F],  $F_c$  [Hz]

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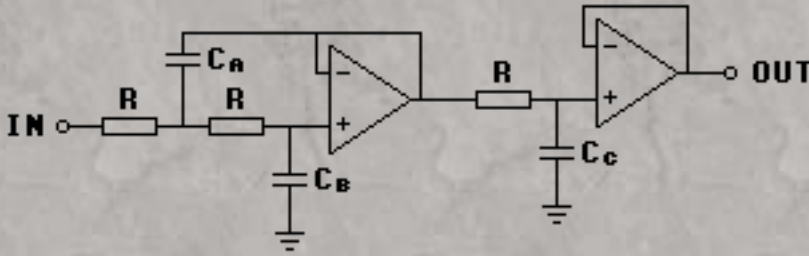
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# Active Filter: Butterworth 18dB Lowpass

## (3st order, 18 dB/octave, Lowpass)



$R=4.7k-10\text{ k}\Omega$

$C_A=2.000/(2\pi F_c R)$

$C_B=0.500/(2\pi F_c R)$

$C_C=1.000/(2\pi F_c R)$

Units:  $R$  [ $\Omega$ ],  $C_x$  [F],  $F_c$  [Hz]

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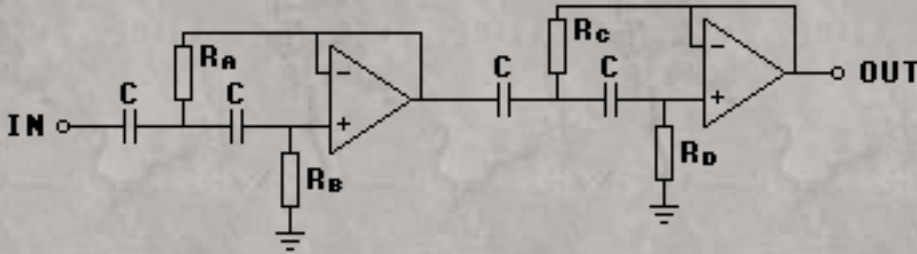
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# Active Filter: Butterworth 24dB Highpass

## (4th order, 24 dB/octave, Highpass)



$$C=4.7\text{n}-10\text{nF}$$

$$R_a=0.9239/(2*\pi*F_c*C)$$

$$R_b=1.0824/(2*\pi*F_c*C)$$

$$R_c=0.3827/(2*\pi*F_c*C)$$

$$R_d=2.6130/(2*\pi*F_c*C)$$

Units:  $R_x$  [Ohm],  $C$  [F],  $F_c$  [Hz]

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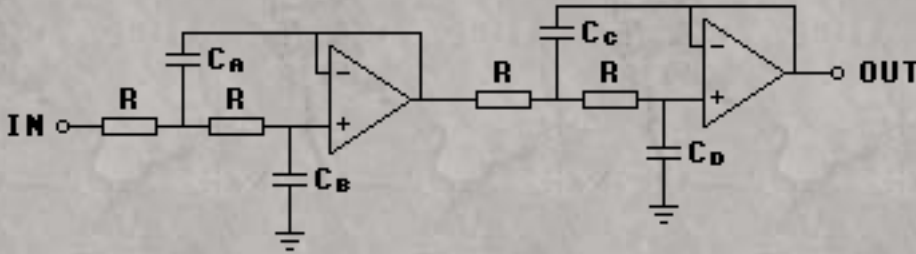
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# Active Filter: Butterworth 24dB Lowpass

## (4th order, 24 dB/octave, Lowpass)



$R=4.7k-10\text{ k}\Omega$

$C_A=1.0824/(2\pi F_c R)$

$C_B=0.9239/(2\pi F_c R)$

$C_C=2.6130/(2\pi F_c R)$

$C_D=0.3827/(2\pi F_c R)$

Units:  $R$  [ $\Omega$ ],  $C_x$  [F],  $F_c$  [Hz]

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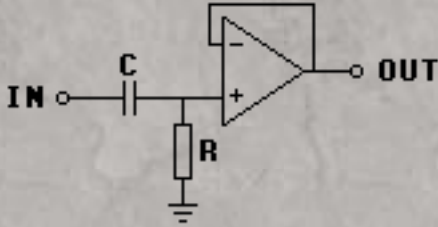
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# Active Filter: Butterworth 6dB Highpass

## (1st order, 6 dB/octave, Highpass)



$C=4.7\text{n-}10\text{nF}$

$R=1.000/(2*\pi*F_c*C)$

Units:  $R$  [Ohm],  $C$  [F],  $F_c$  [Hz]

Contributor: [Joakim Ögren](#)

Source:  
?

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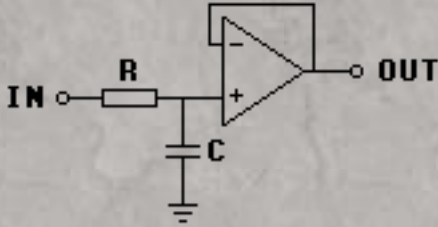
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# Active Filter: Butterworth 6dB Lowpass

## (1st order, 6 dB/octave, Lowpass)



$R=4.7k-10\text{ k}\Omega$

$C=1.000/(2*\pi*F_c*R)$

Units:  $R$  [ $\Omega$ ],  $C$  [F],  $F_c$  [Hz]

Contributor: [Joakim Ögren](#)

Source:  
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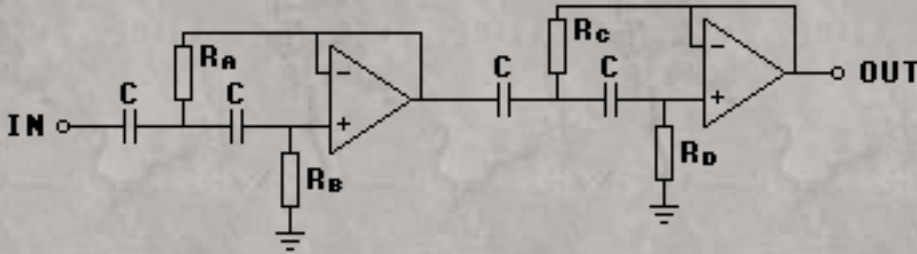
Document last modified: 2001-06-07





# Active Filter: Linkwitz 24dB Highpass

## (4st order, 24 dB/octave, Highpass)



$$C = 4.7\text{n} - 10\text{nF}$$

$$R_a = R_c = 1 / (2 * \sqrt{2} * \pi * F_c * C)$$

$$R_b = R_d = 2R_a$$

Units:  $R_x$  [Ohm],  $C$  [F],  $F_c$  [Hz]

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Source:

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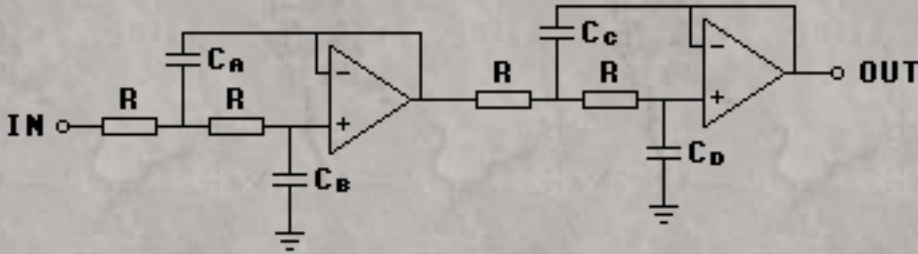
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# Active Filter: Linkwitz 24dB Lowpass

## (4th order, 24 dB/octave, Lowpass)



$R=4.7k-10\text{ k}\Omega$

$C_A=C_C=2 \cdot C_B$

$C_B=C_D=1/(2 \cdot \sqrt{2} \cdot \pi \cdot F_c \cdot R)$

Units:  $R$  [ $\Omega$ ],  $C_x$  [F],  $F_c$  [Hz]

Contributor: [Joakim Ögren](#)

Source:

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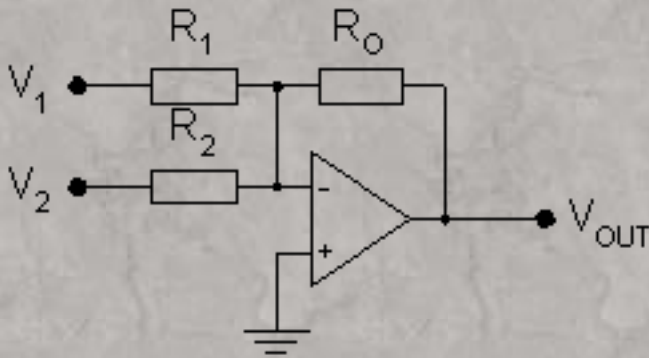
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# Operation Amplifier: Addition

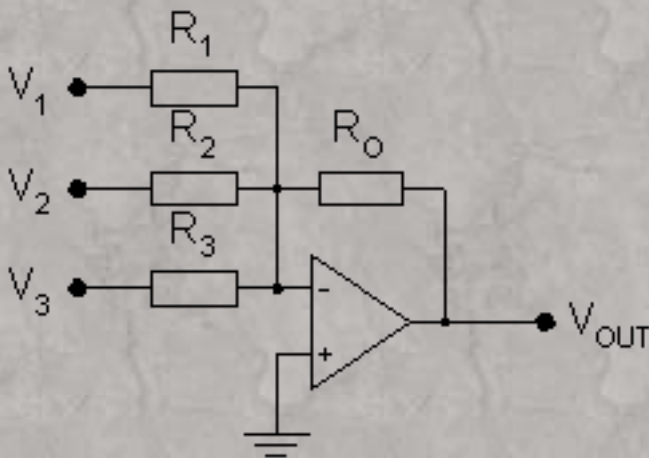


$$V_{OUT} = -(V_1/R_1 + V_2/R_2) * R_O$$

This circuit is used to add several signals to one. By setting all resistors to the same value,  $R_1 = R_2 = R_O$ , you get the following formula:

$$V_{OUT} = -(V_1 + V_2)$$

You can theoretically add how many signals you like. Here's an example with three in-signals:



$$V_{OUT} = -(V_1/R_1 + V_2/R_2 + V_3/R_3) * R_O$$

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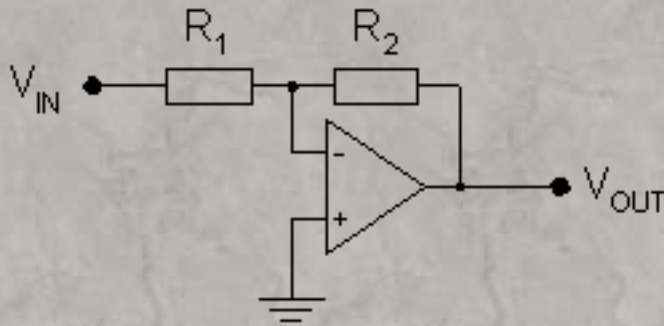
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# Operation Amplifier: Inverting Amplifier



$$V_{OUT} = -(R_2/R_1) * V_{IN}$$

The signal is inverted with this design (notice the minus sign in the formula). But it's very easy to change the gain with the help of  $R_2$ .

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Source:  
?

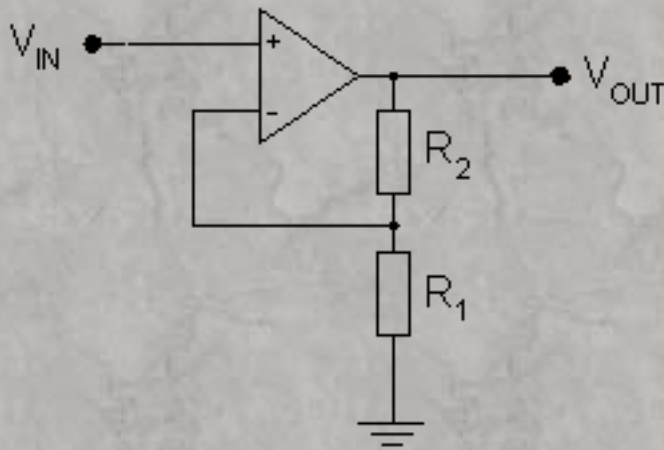
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# Operation Amplifier: Non-inverting Amplifier



$$V_{OUT} = (1 + R_1/R_2) * V_{IN}$$

One positive effect with this design is that the signal isn't inverted. But you can't have less gain than 1 times the in-signal.

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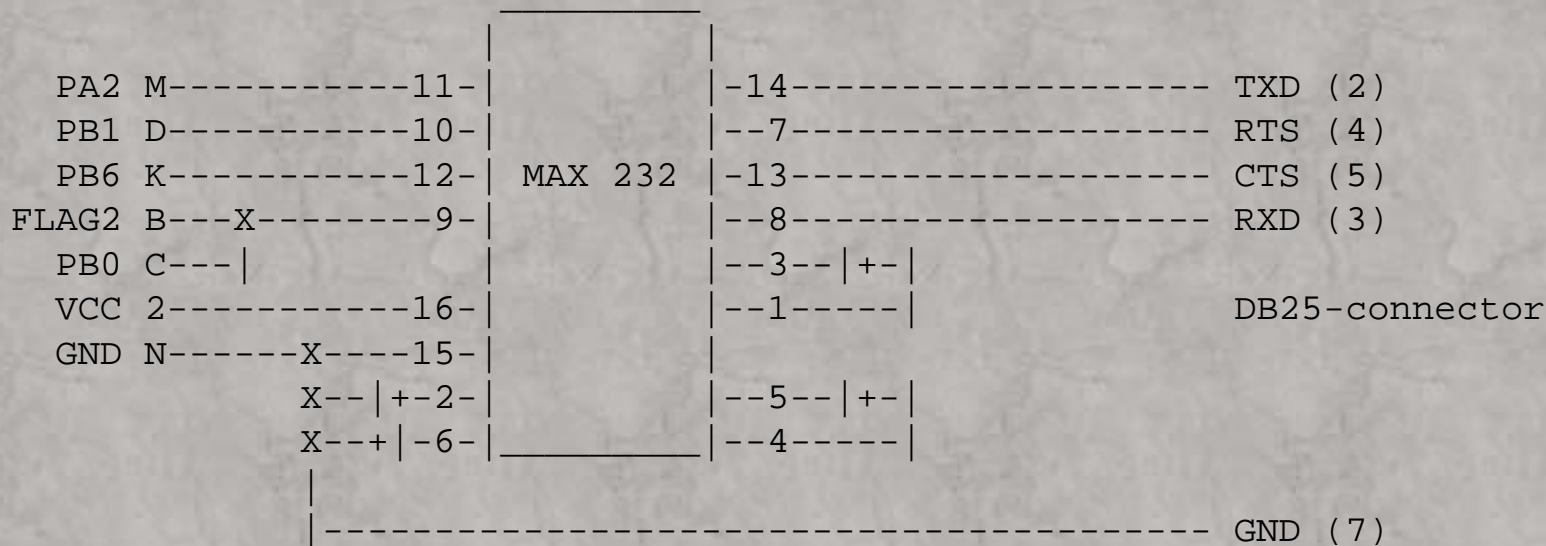
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# C64 to RS232 Interface

Userport C64

C64 RS232



-|+- capacitor 22uF/16V  
- +

Contributor: [Joakim Ögren](#)

Source:

Usenet posting in comp.sys.cbm, C64 -> Serial -> IBM ? by [Andreas Boose](#)

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# CD32 Keyboard to Serial Interface 1

For the signal-translation from the 0-5VDC source to the standard RS232-level (-12VDC / +12VDC) you may choose the MAX232 or an equivalent counterpart (ICL232 ....)

CD32 Keyboard-Port                      level-converter    TTL->RS232                      RS232

```

Pin4 +5V -----Pin16
Pin3 GND -----Pin15-----GND Pin7
Pin2 TxD ----->Pin10  (---|>*-)   Pin7----->RxD Pin3
Pin6 RxD <-----Pin9   (---*<|--)   Pin8<-----Txd Pin2

      C1
      +--)|----Pin1
      |    +
      +-----Pin3
      C2
      +--)|----Pin4
      |    +
      +-----Pin5
      C3
      GND--| (----Pin6
            +      (Polung!)

      C4
      GND--)|----Pin16
            +
      C5
      +--| (----Pin16
      |  +      (Polung!)
      +-----Pin2
  
```

```

+----DSR Pin6
(*) |
+----DCD Pin8
|
+----DTR Pin20
+----RTS Pin4
(*) |
+----CTS Pin5
  
```

(\*) some computers need these handshake connections to proper working

(\*\*)

shielding-----| |-----shielding

connect the shielding of all cables to each other - but only connect it to only ONE interface port connector (i used the keyboard plug).

For the condensers C1..C5 you must get 1 uF electrolyt-condesers.



If your signal-converter is kind of the xxx232A (A-type) you must use 0.1 uF instead (for C1..C5) [source : Maxim Data Book]

Be careful with your explorations. I suggest the serial signals are passed through directly to the PAULA chip - so they are slightly sensitive.

Contributor: [Joakim Ögren](#)

Source:

[CD32 keyboard port info](#) usenet posting by [Klaus Hegemann](#)

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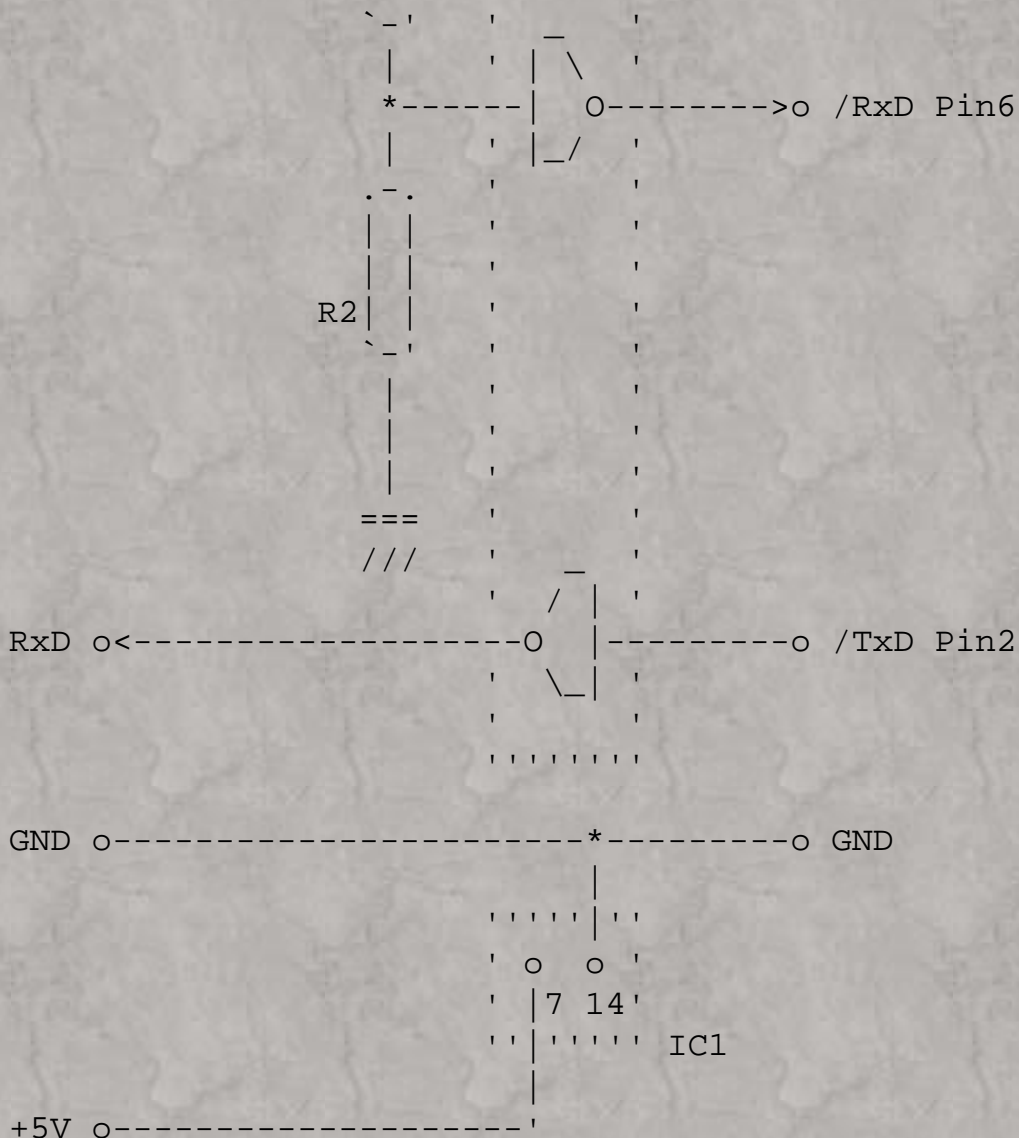
Date: Thu, 20 Oct 1994 11:07:00 +0100  
From: Klaus\_Hegemann@punk.fido.de (Klaus Hegemann)  
Subject: Re: Using Auxiliary Port as Serial Port  
Message-ID: <b1990b05%fidonet@p29.f113.n2452.z2.fidonet.org>  
References: <8df67bba@coyote.dres.dnd.ca>  
Newsgroups: comp.sys.amiga.cd32  
X-Comment-To: sburton@dres.dnd.ca (All)  
Organization: Fido.DE domain gateway (IN e.V.)  
Lines: 91  
X-Gateway: FIDOGATE 3.8.0  
X-FTN-Tearline: CrossPoint v3.02  
X-FTN-Origin: Josef Matula for President (2:2452/113.29)  
X-FTN-Domain: Z242@fidode  
X-FTN-Seen-By: 1000/1 600 601 2000/1 2452/113 3000/1 4900/99 6000/0  
X-FTN-Path: 1000/600 1

```
s> I understand that you can use the auxiliary port (keyboard) as an
s> RS-232 port and that this is what sernet does. But when I look at
s> the pinout, there is only clock and data signals, not ser-in and
s> ser out. What am I missing here?
```

The mess is, that the (serial-) signals carry [negated] TTL-level. As a result, you have to make sure that there is a level-conversion before you connect them to other computers. Without you surely kill your cd32.

If you plan to connect the CD32 with other Amigas then I found out a rather easier/cheaper way to solve that:





the pros. and cons. ([1]this solution ./ . [2]max232-sol. (->FAQ) )

pros.[1]: easy to solder  
 cheap  
 fits within a SUB-D 25 plug  
 does not consume CD32 +5V power ;-)

cons: 'dirty' solution; i.e. circuitry makes use of the 1488/89 tolerances  
 you may only connect Amiga-computers to your cd32 when using THIS  
 [1] circuitry - since they all use the 1488/89 chip set.  
 PCs 'may' work, too. But interface board must contain 1488/89 chip  
 set.  
 I do believe that this will work on all Amigas -I tested it at least  
 on 3 different Amiga-models, however, there is still no guarantee  
 that this will work on yours.

However, I use both interface-types since about 6 months. There has  
 been no problem yet.

s> Also, has anyone made their own connector to the expansion port to

s> pull off the RGB signals? I'd appreciate hearing of your experience.

Yea, does work fine. In use for about 6 months; and still no probs, too. For details refer to the cd32-faq.

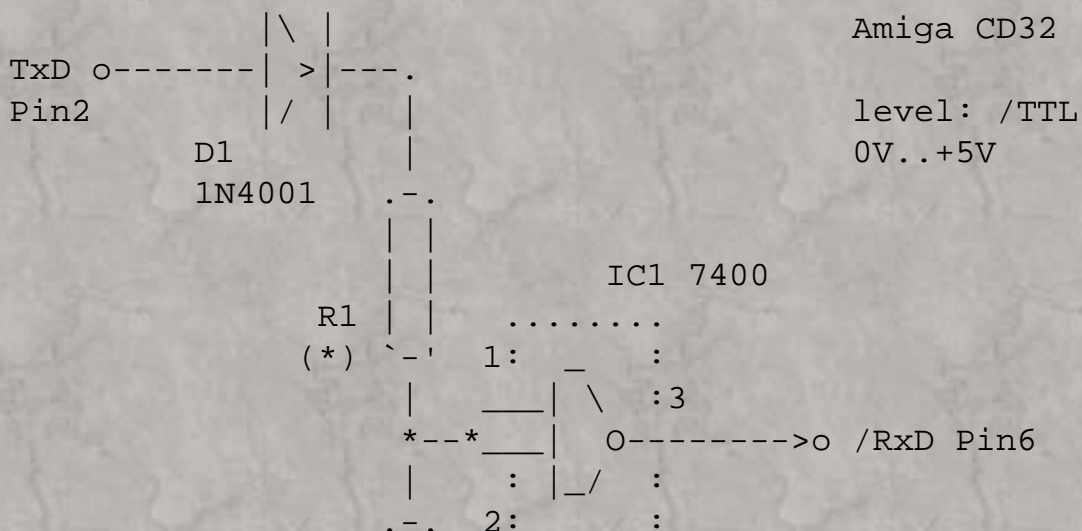
I am not quite sure about the cd32-pin numbers, just take a look in the faq.

bis den bald  
Klaus

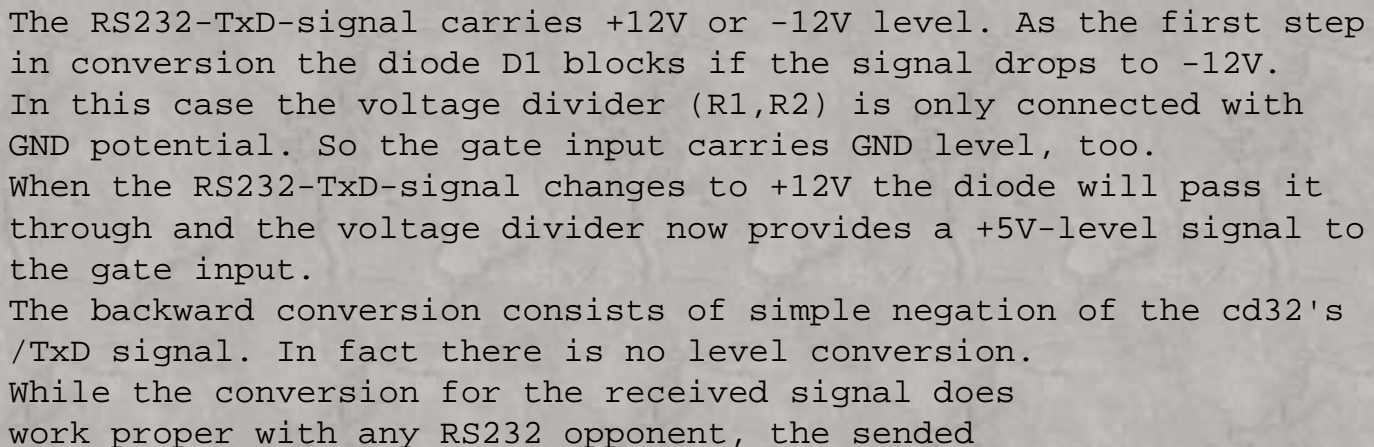
[-----]

Date: Fri, 21 Oct 1994 14:55:00 +0100  
From: Klaus\_Hegemann@punk.fido.de (Klaus Hegemann)  
Subject: Re: [2]Using Auxiliary Port as Serial Port  
Message-ID: <bla112f9%fidonet@p29.f113.n2452.z2.fidonet.org>  
References: <b1990b05%fidonet@p29.f113.n2452.z2.fidonet.org>  
Newsgroups: comp.sys.amiga.cd32  
X-Comment-To: sburton@dres.dnd.ca (All)  
Organization: Fido.DE domain gateway (IN e.V.)  
Lines: 117  
X-Gateway: FIDOGATE 3.8.0  
X-FTN-Tearline: CrossPoint v3.02  
X-FTN-Origin: Josef Matula for President (2:2452/113.29)  
X-FTN-Domain: Z242@fidode  
X-FTN-Seen-By: 1000/1 150 600 601 2000/1 2452/113 3000/1 4900/99 6000/0  
X-FTN-Path: 1000/600 1  
Hi!

'updated info:'  
Amiga 500,2000,1200,...  
  
level: RS232  
-12V..+12V







signal furthermore carries TTL-level.

The opponent hardware tries to regain the TTL-level signal from its 'RS232' input. The conversion unit handles the provided pseudo RS232-type signals correct (as we want it to be:-).

(\*) voltage divider R1-R2:

$$\frac{U}{R1+R2} = \frac{U}{R1+R2} = 12V \quad \frac{U}{R2} = 5V$$

$$\frac{U}{R2} = \frac{U}{R1+R2} \cdot \frac{R1+R2}{R2}$$

$$I = 5 \text{ mA} \Rightarrow R1+R2 = \frac{U}{I} = \frac{12V}{5 \text{ mA}} = 2400 \text{ Ohm}$$

$$\frac{U}{R2} = 5V \Rightarrow R2 = \frac{(R1+R2) \cdot U}{U} = 1000 \text{ Ohm}; R1 = 1400 \text{ Ohm}$$

R1=1500 Ohm

R2=1000 Ohm ==> I=4.8 mA ==> U(R2)=4.8 V .. will be OK

IC1 = 74LS00 (4 NAND gates)

D1 = e.g. 1N4001

have fun !

be careful; I am in no way responsible for any damage that may result.

CU

bis den bald

Klaus klaus@punk.fido.de

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## Information

[ASCII Table](#)

[AWG Table](#)

[SI Prefixes Table](#)

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# ASCII Table

Dec	Hex	Char	Description	Dec	Hex	Char	Dec	Hex	Char	Dec	Hex	Char
0	0	NUL	(null)	32	20		64	40	@	96	60	`
1	1	SOH	(start of heading)	33	21	!	65	41	A	97	61	a
2	2	STX	(start of text)	34	22	"	66	42	B	98	62	b
3	3	ETX	(end of text)	35	23	#	67	43	C	99	63	c
4	4	EOT	(end of transmission)	36	24	\$	68	44	D	100	64	d
5	5	ENQ	(enquiry)	37	25	%	69	45	E	101	65	e
6	6	ACK	(acknowledge)	38	26	&	70	46	F	102	66	f
7	7	BEL	(bell)	39	27	'	71	47	G	103	67	g
8	8	BS	(backspace)	40	28	(	72	48	H	104	68	h
9	9	TAB	(horizontal tab)	41	29	)	73	49	I	105	69	i
10	A	LF	(NL line feed, new line)	42	2A	*	74	4A	J	106	6A	j
11	B	VT	(vertical tab)	43	2B	+	75	4B	K	107	6B	k
12	C	FF	(NP form feed, new page)	44	2C	,	76	4C	L	108	6C	l
13	D	CR	(carriage return)	45	2D	-	77	4D	M	109	6D	m
14	E	SO	(shift out)	46	2E	.	78	4E	N	110	6E	n
15	F	SI	(shift in)	47	2F	/	79	4F	O	111	6F	o
16	10	DLE	(data link escape)	48	30	0	80	50	P	112	70	p
17	11	DC1	(device control 1)	49	31	1	81	51	Q	113	71	q
18	12	DC2	(device control 2)	50	32	2	82	52	R	114	72	r
19	13	DC3	(device control 3)	51	33	3	83	53	S	115	73	s
20	14	DC4	(device control 4)	52	34	4	84	54	T	116	74	t
21	15	NAK	(negative acknowledge)	53	35	5	85	55	U	117	75	u
22	16	SYN	(synchronous idle)	54	36	6	86	56	V	118	76	v
23	17	ETB	(end of trans. block)	55	37	7	87	57	W	119	77	w
24	18	CAN	(cancel)	56	38	8	88	58	X	120	78	x



25	19	EM	(end of medium)	57	39	9	89	59	Y	121	79	y
26	1A	SUB	(substitute)	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	(escape)	59	3B	;	91	5B	[	123	7B	{
28	1C	FS	(file separator)	60	3C	<	92	5C	\	124	7C	
29	1D	GS	(group separator)	61	3D	=	93	5D	]	125	7D	}
30	1E	RS	(record separator)	62	3E	>	94	5E	^	126	7E	~
31	1F	US	(unit separator)	63	3F	?	95	5F	_	127	7F	DEL

## Format control

### BS

Backspace. Indicates movement of the printing mechanism or display cursor backwards in one position.

### HT

Horizontal Tabulation. Indicates movement of the printing mechanism or display cursor forward to the next preassigned 'tab' or stopping position.

### LF

Line Feed. Indicates movement of the printing mechanism or display cursor to the start of the next line (ie one line down).

### VT

Vertical Tabulation. Indicates movement of the printing mechanism or display cursor to the next of a series of preassigned printing lines.

### FF

Form Feed. Indicates movement of the printing mechanism or display cursor to the starting position of the next page, form, or screen.

### CR

**Carriage Return.** Indicates movement of the printing mechanism or display cursor to the starting position (left) of the current line.

# Transmission control

## SOH

**Start of Heading.** Used to indicate the start of a heading which may contain address or routing information.

## STX

**Start of Text.** used to indicate the start of the text and so also indicates the end of the heading.

## ETX

**End of Text.** Used to terminate the text which was started with STX. End of Transmission indicates the end of a transmission which may have included one or more 'texts' with their headings.

## ENQ

**Enquiry.** A request for a response from a remote station. It may be used as a "who are you?" request for a station to identify itself.

## ACK

**Acknowledge.** A character transmitted by a receiving device as an affirmation response to a sender. It is used as a positive response to polling messages.

## NAK

**Negative Acknowledgement.** A character transmitted by a receiving device as a negative response to a sender. It is used as a negative response to polling messages.

## SYN

**Synchronous/Idle.** Used by a synchronous transmission system to achieve synchronisation. When no data is being sent a synchronous transmission system may send SYN characters continuously.

## ETB

End of Transmission Block. Indicates the end of a block of data for communication purposes. It is used for blocking data where the block structure is not necessarily related to the processing format.

## Information separator

### FS

File Separator.

### GS

Group Separator.

### RS

Record Separator.

### US

Unit Separator.

Information separators to be used in an optional manner except that their heirarchy shall be FS (the most inclusive) to US (the least inclusive).

## Miscellaneous

### NUL

Null. No character. Used for filling in time or filling space on tape when there is no data.

### BEL

Bell. Used when there is need to call human attention. It may control alarm or attention devices.

### SO

**Shift Out.** Indicates that the code combinations which follow shall be interpreted as `_outside_` the standard character set until an SI character is reached.

## SI

**Shift In.** Indicates that the code combinations which follow shall be interpreted according to the standard character set.

## DLE

**Data Link Escape.** A character which shall change the meaning of one or more contiguously following characters. It can provide supplementary controls or permits the sending of data characters having any bit combination.

## DC1, DC2, DC3, DC4

**Device Controls.** Characters for the control of ancillary devices or special terminal features.

## CAN

**Cancel.** Indicates that the data which preceeds it in a message or block should be disregarded (usually because an error has been detected).

## EM

**End of Medium.** Indicates the physical end of a card, tape or other medium, or the end of the required or used portion of the medium.

## SUB

**Substitute.** Substituted for a character that is found to be erroneous or invalid.

## ESC

**Escape.** A character intended to provide code extension in that it gives a specified number of contiguously following characters an alternate meaning.

## SP



Space. A nonprinting character used to separate words, or to move the printing mechanism or display cursor forward by one position.

## DEL

Delete. Used to obliterate unwanted characters (for example, on paper tape by punching a hole in \_every\_ bit position).

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*Source:*  
[ASCII table](#) at [The Pin-Out directory](#)

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# AWG Table

AWG=American Wire Gauge standard

Gauge	Diam	Area	R	I at 3A/mm2
AWG	mm	mm2	ohm/km	mA
46	0,04	0,0013	13700	3,8
44	0,05	0,0020	8750	6
42	0,06	0,0028	6070	9
41	0,07	0,0039	4460	12
40	0,08	0,0050	3420	15
39	0,09	0,0064	2700	19
38	0,10	0,0078	2190	24
37	0,11	0,0095	1810	28
	0,12	0,011	1520	33
36	0,13	0,013	1300	40
35	0,14	0,015	1120	45
	0,15	0,018	970	54
34	0,16	0,020	844	60
	0,17	0,023	757	68
33	0,18	0,026	676	75
	0,19	0,028	605	85
32	0,20	0,031	547	93
30	0,25	0,049	351	147
29	0,30	0,071	243	212
27	0,35	0,096	178	288
26	0,40	0,13	137	378
25	0,45	0,16	108	477
24	0,50	0,20	87,5	588

	0,55	0,24	72,3	715
	0,60	0,28	60,7	850
22	0,65	0,33	51,7	1,0 A
	0,70	0,39	44,6	1,16 A
	0,75	0,44	38,9	1,32 A
20	0,80	0,50	34,1	1,51 A
	0,85	0,57	30,2	1,70 A
19	0,90	0,64	26,9	1,91 A
	0,95	0,71	24,3	2,12 A
18	1,00	0,78	21,9	2,36 A
	1,10	0,95	18,1	2,85 A
	1,20	1,1	15,2	3,38 A
16	1,30	1,3	13,0	3,97 A
	1,40	1,5	11,2	4,60 A
	1,50	1,8	9,70	5,30 A
14	1,60	2,0	8,54	6,0 A
	1,70	2,3	7,57	6,7 A
13	1,80	2,6	6,76	7,6 A
	1,90	2,8	6,05	8,5 A
12	2,00	3,1	5,47	9,4 A

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# SI Prefixes Table

Example: 1 TW=1000 GW (W=Watt)

Symbol	Prefix	Factor
Y	Yotta	$10^{24}$
Z	Zetta	$10^{21}$
E	Exa	$10^{18}$
P	peta	$10^{15}$
T	tera	$10^{12}$
G	giga	$10^9$
M	Mega	$10^6$
k	kilo	$10^3$
h	hecto	$10^2$
da	deca	$10^1$
d	deci	$10^{-1}$
c	centi	$10^{-2}$
m	milli	$10^{-3}$
μ u	micro	$10^{-6}$
n	nano	$10^{-9}$
p	pico	$10^{-12}$
f	femto	$10^{-15}$
a	atto	$10^{-18}$
z	zepto	$10^{-21}$
y	yokto	$10^{-24}$

*Note: In the computer world things are a bit different:*



Symbol	Prefix	Factor	Factor
P	peta	$2^{50}$	1125899906842624
T	tera	$2^{40}$	1099511627776
G	giga	$2^{30}$	1073741824
M	Mega	$2^{20}$	1048576
k	kilo	$2^{10}$	1024

There is also the prefixes adopted by IEC in order to cope with the digital world. These are not widely used (yet).

Symbol	Prefix	Factor	Factor
Ei	exbi	$2^{60}$	1152921504606846976
Pi	pebi	$2^{50}$	1125899906842624
Ti	tebi	$2^{40}$	1099511627776
Gi	gibi	$2^{30}$	1073741824
Mi	mebi	$2^{20}$	1048576
Ki	kibi	$2^{10}$	1024

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Source:  
Farnell Components Catalogue

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Here are some links to good sites of technical information on the Internet.

I have a lot of pages I will add as soon as I get the time for it. They are currently in my bookmarks file. Remember that I usually add links to pages covering a specific topic at bottom of the best suited HwB page.

## Misc:

<u>Name</u>	<u>Author</u>	<u>Comment</u>
<a href="#">TheRef</a>	<a href="#">F. Robert Falbo</a>	Harddrives & controllers specifications.
<a href="#">The Tech Page</a>	<a href="#">Blue Planet Corporation</a>	Harddrives & controllers specifications.
<a href="#">Norm's Industrial Electronics</a>	<a href="#">Norman Dyrvik</a>	Misc electronic links.
<a href="#">Circuit Cookbook</a>	<a href="#">Dan Charrois</a>	Various circuits.
<a href="#">Electrical Engineering Circuits Archive</a>	<a href="#">Jerry Russell</a>	Various circuits.
<a href="#">sandpile.org: 80x86</a>	<a href="#">Christian Ludloff</a>	Everything about 80x86 processors & motherboards.
<a href="#">The Computer Information Centre</a>	Many	Contains very much about electronics/computers.
<a href="#">We-Man's Electro Stuff</a>	<a href="#">Stefan Wieman</a>	Misc electronic stuff.
<a href="#">Tomi Engdahl's Electronics Pages</a>	<a href="#">Tomi Engdahl</a>	You will find almost everything here.
<a href="#">PC Mechanic</a>	<a href="#">David Risley</a>	Good info for beginners about how to build PC's.
<a href="#">Armory Electronics Archive</a>	<a href="#">Richard Steven Walz</a>	FTP archive with lots of electronics related files.
<a href="#">ChipDir</a>	<a href="#">Jaap van Ganswijk</a>	Pinouts to Integrated Circuits etc.
<a href="#">GamesX</a>	<a href="#">Lawrence Wright</a>	Pinouts to videogames.
<a href="#">Pin-Outs.com</a>	Pin-Outs.com	Cables, Pinouts and Connectors

# FAQs:

<u>Name</u>	<u>Author</u>	<u>Comment</u>
<a href="#">alt.comp.hardware.homebuilt FAQ</a>	<a href="#">Mark Sokos</a>	Misc information about how to build your own things.
<a href="#">Sci.Electronics.Repair Frequently Asked Question(s)</a>	Various	Lots of links and useful FAQ:s (Repair notes, pinouts and so on)

If you have any more good links of interest, please send us an [e-mail](#).

Feel free to add a link to Hardware Book at Your page. You can use this banner if you would like to:



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The Hardware Book is available in some other formats as well. For the moment only the HTML-version is available for download. Later the PDF and WinHelp versions will be back.

HTTP	Filesize	Date	Description
<a href="#">hwb-010706.zip</a>	1052655	2001-07-06	HTML version, archived with Zip. Open index.html in your HTML-browser.
<a href="#">hwb-010706.tgz</a>	550460	2001-07-06	HTML version, archived with Tar and compressed with GZip. Open index.html in your HTML-browser.
<a href="#">hwb-010706.lha</a>	989952	2001-07-06	HTML version, archived with LhA. Open index.html in your HTML-browser.

You'll also find HwB as a Debian GNU/Linux package in the "non-free" section.

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## New version of The Hardware Book!

The Hardware Book has undergone some major restructuring, refining and making it possible to maintain. Lots of new information has been added and all the web links have been verified.

The index system has been revamped to allow us to make for example equipment specific indexes (like all C=64 hardware on one page). This is not implemented right now, but it is possible now with the new index system.

Since the mirror information was badly outdated, that list has been removed for now. We will start taking contact with the mirrors to make them aware of that The Hardware Book is now actively maintained.

Right now it will only be available for offline reading in HTML format. PDF and others will follow.

We will now actively accept pinouts and other specifications and add them to The Hardware Book which will be released more often now. Like before, please don't send questions asking if we have a specific pinout... If it's not listed in The Hardware Book, it's not likely that we have it.

Lots of people have asked when there will be a new release and why there has been so little activity in The Hardware Book. This is mainly because Joakim Ögren was going to Qatar to work for 2-3 months in the end of 1997, and he is still working there :-).

-- The Hardware Book team as of 2001-06-08.

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Please help us make this reference guide larger. We guess there is much more to add. Don't hesitate to send some strange pinout, circuit or cable.

If you have a strange serial-port on your dish-washer, SEND it to us :-)

If it does not have one you could send me a circuit on how to add a serial-port to it. :-)

*We have already heard from two people that has a serial port on their dish-washers :)*

We are especially searching for the following standards:

- EIB
- SMP16
- SA1000
- JVC bus?
- PC-Engine/TurboGrafix 16 connectors
- Qbus
- MULTIBUS
- MULTIBUS II
- MTM-Bus
- GIO
- FutureBus+
- Nec PC-FX connectors
- Kenwood CD-Player RS232-port (For example DP-M7750).
- IBM PS/2 Motherboard Power connector
- Epson Sample E04974 Diskdrive with Signals+Power in the usual 34 pin connector.
- 40 pin diskdrive connector (not IDE..)
- XTA Interface

Other information of value:

- Filters

If you have any of the above listed please send an e-mail to [the Hardware Book team](mailto:the Hardware Book team).

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What about this? Your free reference guide to electronics.

May be copied and redistributed, partially or whole, as appropriate. If you copy parts of the information, make a reference to the Hardware Book.

The Hardware Book is a compilation of pinouts from different sources. All pages have the same style of presentation. This makes it easier to find information for you. We are not trying to sell anything.

HwB has been developed on spare time and is made available to you for free. This also means that we can't guarantee that the presented information is correct. Use it on you own risk. We can't take the whole credit for HwB. We have since the first release received a great lot of e-mail with suggestions, questions and information. With the help of many contributors HwB has grown. Keep sending the e-mail...

This is the HwB team:



Joakim Ögren  
Creator and editor of HwB.



Tomas Ögren  
Editor of HwB.





Niklas Edmundsson  
Editor of HwB.



Magnus Jonsson  
Editor of HwB.

Could it be even better? Perhaps if You help us. Please send any material you have that might be of interest for this project. Send it to [us](#).

We would especially like to thank the following people:

[Academic Computer Club](#) For hosting the current [Hardware Book Main Site](#)

Karl Asha for hosting HwB in the beginning.

Rob Gill for sending me many nice pinouts etc.

Petr Krc for sending me many nice pinouts etc.

Marco Budde maintainer of the HwB Linux Debian package.



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